Optical and Electrical Testing of Latchup in I/O Interface Circuits

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Abstract

Backside light emission and electrical measurements were used to evaluate the susceptibility to latchup of externally cabled I/O pins for a 0.13 μm technology generation [1,2] test chip, which was designed in a flip-chip package. Case studies of several Inputs/Outputs (I/Os) are shown along with conclusions regarding layout and floorplanning to ensure the robustness to various types of latchup trigger events.

1. Introduction

In this paper we use Emission Microscopy (EMMI) to examine the events leading up to sustained latchup for various I/O pins in an effort to optimize ground rules for electrostatic discharge (ESD) robustness and compact layout. As it has been shown in the literature [3-4], EMMI can be used in order to determine which circuits latched up. Here we show how it is possible to examine different I/O circuits placed in a variety of different environments in order to modify design rules to improve latchup robustness while optimizing placement of circuits adjacent to the I/Os.

While the test procedure and experimental setup will be described and compared to JEDEC78 specifications [5], the major emphasis will be on the analysis of the optical measurements which permit the localization of structures prone to latchup ignition as well as the study of its propagation to neighboring circuitry. In order to achieve such results, a novel technique based on the use of EMMI and a precise control of both pin current and supply current will be discussed. The effect of nearby logic circuitry, *n*-well substrate contact periodicity and temperature on the ignition of latchup will be examined in detail.

2. Latchup background

Latchup is the ignition of the *pnpn* or *npnp* parasitic structure (also know as Silicon Controlled Rectifier (SCR) or thyristor) created in conventional bulk CMOS technologies, as shown in Fig. 1. Such a structure is formed by two *npn* and *pnp* bipolar transistors (one is a vertical or horizontal device, while the other is a lateral device formed in the substrate) closed in a positive feedback loop [6,7]. During normal operating conditions the *pnpn* structure is characterized by very high impedance, and no significant current flows through the structure (connected between V_{DD} and ground). However, carriers injected into the structure, or voltage variations, can turn on one of the two bipolar transistors, thus leading to significant conduction between V_{DD} and ground. During this phase, if the gain of the feedback loop ($\beta_{npn} \times \beta_{pnp}$) becomes greater than one, it can lead to a latchup situation in which the conduction is self-sustained and the external trigger voltage/current is no longer required. The *pnpn* structure will stay on until the supply voltage is turned off. Unless the supply current is appropriately limited, this phenomenon could lead very quickly to the destruction of the chip due to excessive power dissipation.

In prior literature [6-8], it was shown that there are two major categories of latchup events depending on whether the trigger is internal or external to the circuit. The former consists of supply voltage or ground bounces, due to abrupt variation in current consumption, and over voltage spikes due to transmission line reflections. The external causes are generally one of the following: bad supply voltage regulation, radiation effects, such as x-rays and cosmic rays, and electrostatic discharge at the I/O interfaces (cable discharge).

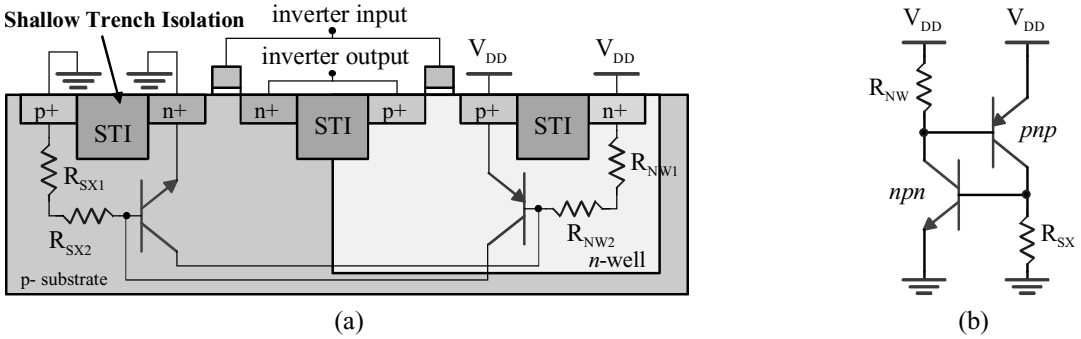


Fig. 1. Parasitic bipolar transistors created in a standard CMOS process are connected to form an SCR structure.

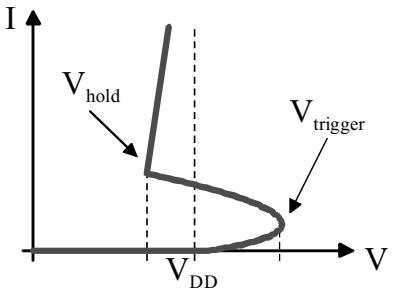


Fig. 2. Overshoot I-V curve of an SCR structure.

In this paper, we will focus our attention on the case of the injection of minority carriers into the *p*- substrate caused by cable discharge because it constitutes the biggest challenge faced when using a bulk *p*-type silicon substrate (1-2 Ω-cm *p*- wafer). If minority carriers are not promptly collected by *n*-well guard rings [6], or if there are not enough substrate contacts to supply the recombination holes, the minority carriers can reach neighboring circuitry, thus triggering latchup events.

2.1. Packaging effects on I/O placement

Since the test chip considered in this paper uses flip-chip packaging, the I/O circuits can be located anywhere within the silicon die area. In addition, I/O circuits can be adjacent to: other I/O circuits, standard or custom-designed circuits, Unused Gate Array (UGA) circuits, decoupling capacitances, *etc*. This situation greatly differs from the perimeter image (used in wire-bond packaging) where the I/O circuits are only located around the perimeter of the chip and active circuitry is only on one side of the I/O. In the latter case, floorplan is straightforward, each I/O is isolated from the others and only the side toward the interior of the chip varies. In the situation examined here, all four sides of the I/O circuit can be different from one I/O to the other, offering us a large variety of environments to test for latchup immunity or susceptibility.

2.2. Internal latchup

As shown in Fig. 1(a), a *pnpn* parasitic structure is created in bulk CMOS process with *p*-type substrate every time an *n*-FET and *p*-FET are placed adjacent to each other. Fig. 1(b) shows the schematic of the *pnpn* circuit. Typical peak beta values observed in present advanced CMOS technologies range from 1 to 5 and from 1 to 3 for the *npn* and the *pnp*, respectively. As a result, the product of the $\beta_{npn}\times\beta_{pnp}$ is typically larger than one, thus leading to a sustained latchup event if V_{DD} is larger than the holding/sustaining voltage of the *pnpn* (see Fig. 2). An ideal *I-V* curve is shown for the case where the *p*+ diffusion exceeds the *n*-well voltage (referred to here as *overshoot* triggering, V_{DD} noise/bounce or *p*-FET hot-hole generation/injection into *n*-well). If the *pnp* in Fig. 1(a) is forward biased, it injects holes into the substrate, then triggering the *npn*. The holding/sustaining voltage and trigger voltage are shown on the I-V in Fig. 2, where the trigger voltage is the amount that the *p*+ voltage needs to exceed the *n*-well potential in order for *pnpn* to turn on, and the holding/sustaining voltage is the amount of voltage required to sustain the latchup event. The opposite case, relative to the overshoot triggering, occurs when the substrate local potential exceeds the *n*+ voltage (referred to here as *undershoot* triggering, ground noise/bounce or *n*-FET hot-electron generation/injection into substrate), the *npn* is forward biased injecting electrons into *n*-well, leading to triggering of the *pnp*.

2.3. External latchup

There are two main sources of external latchup triggering. The first is due to the injection of majority carriers from external sources (on-chip or off-chip). In this case, holes are injected into the *p*-type substrate, thus increasing the local substrate potential, eventually forward biasing junctions (diode built-in voltage exceeded) in the substrate, and potentially leading to the triggering of latchup. An example of cross-section of a circuit showing latchup due to the external injection of majority carries is shown in Fig. 3(a), as well as the schematic (Fig. 3(b)) of the equivalent electrical circuit highlighting the fact that the holes are injected into ground until the voltage rises high enough to turn on the *npn* transistor. The second source of external latchup is caused by the injection of minority carriers from external I/O sources. In this case electrons are injected into the substrate and diffuse until collected by *n*-type diffusions or until they recombine in the *p*-type substrate. The recombination length of electrons in a 1-2 Ω-cm *p*-type substrate is on the order of 20-30 μm. In

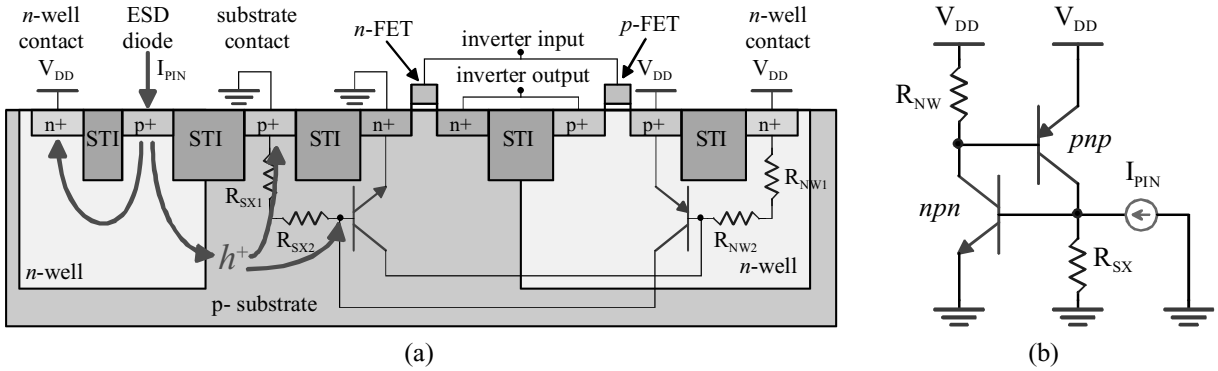


Fig. 3. Cross-section of a circuit showing latchup caused by majority carriers injected from an external source (I_{pin}).

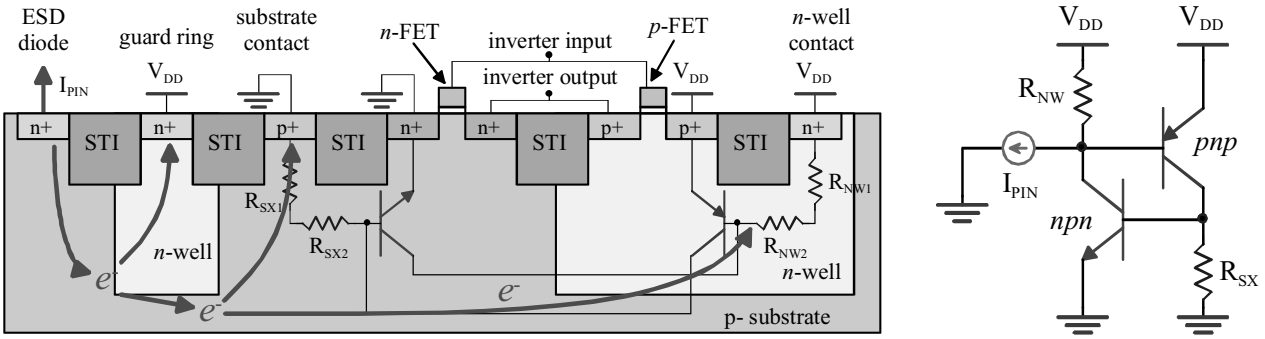


Fig. 4. Some of the minority carriers injected into the silicon substrate (I_{pin}) by the ESD protection diode (left hand side) may escape guard rings and trigger the ignition of a latchup process.

Fig. 4, a cross-section of a circuit and the corresponding schematic of latchup caused by minority carriers are shown.

In order to test the latchup sensitivity of a given circuit in compliance with JEDEC78 [5] specifications, a positive/negative current must be applied to the signal pads connected to I/O circuits. The details of pulse duration (10 µs - 1 s per JEDEC78) and characteristics must be chosen depending upon the circuit specifications and the real-life environment that the testing is trying to emulate.

In the case of positive polarity current injection into an I/O signal pad, any *p*-type diffusion connected to the I/O pad typically gets forward biased (see Fig. 3(a)): usually ESD *p*-type diodes and output driver *p*-FETs. In either case, anytime there exists a *p*-diffusion inside *n*-well connected to an I/O pad, the *p*-diff/*n*-well junction (Fig. 3(a)) becomes the emitter/base junction of a horizontal or vertical *pnp* transistor, while the substrate forms the collector terminal. Therefore, when the *p*-diff/*n*-well junction of the parasitic *pnp* transistor is forward biased, it injects holes into the substrate. If such a current is high enough to raise the local substrate potential above 0.5 V, local *n*-diff/*p*-sub junctions can become forward biased as well, thus leading to the triggering of latchup. The previous analysis points out that the key design variable for inhibition of latchup due to majority carriers is to introduce large substrate contact rings around any *p*-type diffusions inside each *n*-well connected to I/O pads. This ensures a very low substrate resistance, *i.e.* that the current injected into the substrate is effectively collected by substrate contacts before reaching *n*-type diffusions. Such a strategy can easily be implemented during the design of a new circuit and therefore does not constitute a big challenge.

In the case of a negative pin current (current being pulled out of I/O pad), any *n*-type diffusion connected to the I/O pad will become forward biased as shown in Fig. 4(a), thus injecting electrons into the *p*-type substrate. These minority carriers can diffuse more than 500-600 µm for a 1-2 Ω-cm *p*-type wafer and eventually either recombine or get collected by other *n*-type diffusions (*n*-type source/drain junctions or *n*-wells). If the electrons are collected by neighboring *n*-wells in the logic, the local *n*-well potential may decrease enough to allow the diffusion of holes within the *n*-well that is connected to V_{DD}, and latchup may occur.

3. Test procedure

Latchup resistance of I/Os on new ICs is usually verified by means of the JESD/JEDEC78 test procedure [5]. This standard requires that, in a first step, the circuit be put in standby condition and the corresponding quiescence current measured ($I_{DDQ\text{-}pre}$). Then, a current equal to $I_{DDQ\text{-}pre}$ ± 100 mA is applied to the I/O pin under test, and, after the injected current is removed, the total current absorbed by the IC is measured again ($I_{DDQ\text{-}post}$). A latchup event is considered to have occurred if one of the following

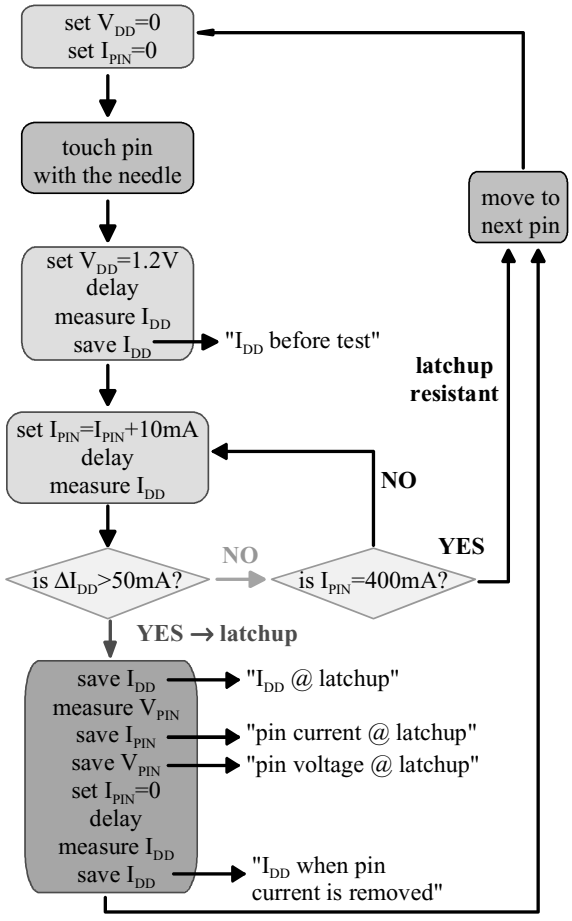


Fig. 5. Diagram of the electrical testing procedure.

two criteria applies:

$$I_{DDQ-post} > 1.4 \times I_{DDQ-pre} \quad (1)$$

or

$$I_{DDQ-post} > I_{DDQ-pre} + 10mA \quad (2)$$

In this work we developed a slightly different version of the JEDEC78 test specifications. We will show that such a test method, when combined with the use of time-integrated acquisitions of the near-infrared (NIR) light emitted by the I/O circuit and any circuitry in its proximity, can be very useful in the localization of incipient latchup occurrences, as well as their dynamic evolution.

The modified procedure schematically depicted in Fig. 5 for a generic I/O pin, is based on the progressive increase of a DC pin current. In order to remove electrostatic charge and avoid unwanted latchup causes, the probe used for injecting current into the I/O pin is initially grounded. Moreover, the IC is not biased until the contacting procedure is complete. The nominal supply voltage is applied to the chip, which is left in a low power standby mode until it reaches a stable operating condition. The test begins by progressively increasing the amount of current pulled from the I/O pin, usually in steps of 10 mA or less. The current absorbed by the chip is monitored simultaneously until a sizable variation ("jump") is detected. When this occurs the pin current is set to zero and the $I_{DDQ\text{-}post}$ of the IC is tested again. Otherwise, the pin current is increased until the maximum limit is achieved and the I/O circuitry is considered to be latchup resistant.

If $I_{DDQ\text{-}post}$ falls into one of the two categories presented above for the JEDEC78 specifications (see conditions (1) and (2)), a latchup event is considered to have occurred. If the $I_{DDQ\text{-}post}$ returns to a value very similar to the one measured before starting the test ($I_{DDQ\text{-}pre}$), a sustained latchup condition was not reached, although a "soft" latchup started to form somewhere in the proximity of the I/O circuitry. Such situations are of interest while trying to understand the dynamics of the formation of conventional latchup that, by definition, is sustained until the chip is damaged or the supply voltage is removed. After a latchup event is detected, the supply voltage is set to zero and the system moves to the next pin to test. Time-integrated images of the NIR light emitted by the I/O circuit and the circuitry in its proximity can be collected during any stage of the test. Using their overlay with the layout of the circuit (emission image over layout) it is possible to identify the areas most prone to latchup, and to follow the dynamic propagation of the latchup current among circuits near the cable I/O.

The whole test program flowchart shown in Fig. 5 is written in Matlab [9]; the instrumentation used in the experiment is controlled by a PC through a GPIB bus. The program loads a setting file containing the list of all I/O pins to test, along with their corresponding name on the test board. Although in the presented experiment we manually contacted each test pin with a needle, the procedure could be fully automated by using a switching matrix. The test results, as well as all collected data, were stored in a separate file that was used for post-test analysis.

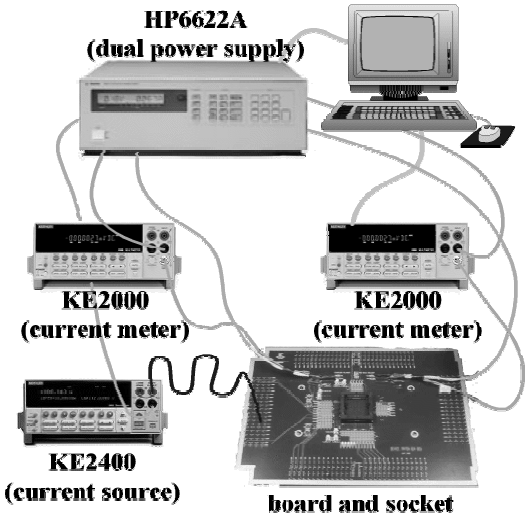


Fig. 6. Schematic of the electrical setup.

3.1. Experimental setup

Fig. 6 presents a schematic of the electrical setup used for the test described in the previous section and used for all DC measurements in this experiment. The chip is packaged on a Temporary Chip Attach (TCA) carrier and mounted on a test board that provides supply voltage and ground, as well as access to the I/O pins. In order to collect the NIR emission from the backside of the chip, the socket must be opened and the silicon substrate thinned down to about 100 μm (or less, depending upon the doping concentration of the substrate) and polished.

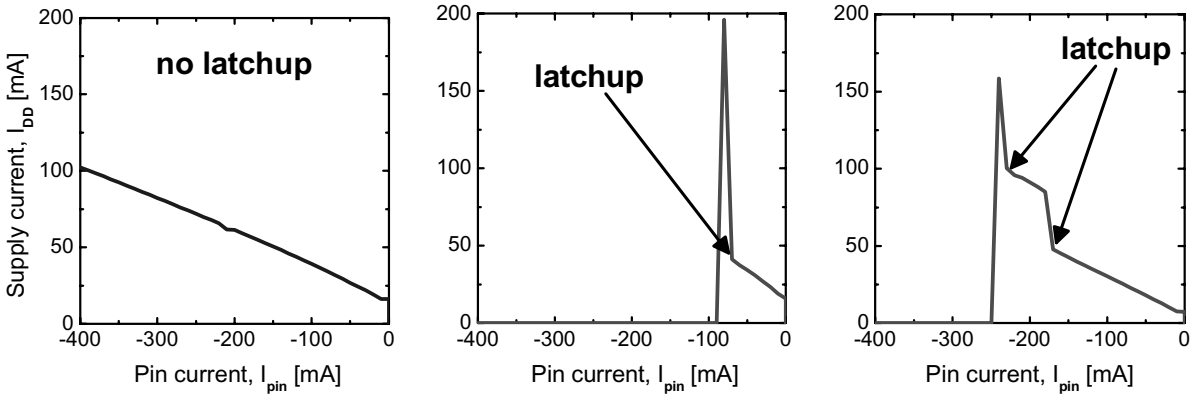
The chip bias voltage is provided by means of a dual output HP6622A power supply [10], capable of supplying two different voltages. The I_{DDQ} current is monitored using two Keithley 2000 multimeters [11], connected in series between the power supply and the board. The pin current is provided by a Keithley 2400 sourcemeter [12], which can be used as a precise current source while monitoring the pin voltage.

The time-integrated images of latchup emission are collected by means of an emission-based microscope using the Hamamatsu C4880-21 NIR back-illuminated Charge-Coupled Device (CCD) camera [13], while a particular bias condition is held constant by the measurement system. The power supply compliance and the pin current can be gradually varied after each light emission acquisition in order to study the dynamic evolution of latch ignition.

3.2. Electrical test results

The I/Os of the IC were tested at the nominal voltage of 1.2 V while applying a maximum pin current of 400 mA, which was chosen to evaluate latchup robustness beyond the usual JEDEC78 requirements. The maximum current step was 10 mA, but it could be reduced in amplitude to allow for precise tracking of the ignition of latchup by means of light emission images.

All I/O circuitries were resistant to latchup when a positive current was injected into the pin. Due to the *p*-doped silicon substrate and the specific layout around the



(a) (b) (c)

Fig. 7. Typical results of the electrical test, for three different I/Os, showing three distinct cases: (a) no latchup detected, (b) single latchup occurrence, (c) multiple latchup conditions.

ESD diodes, only minority electrons injected into the substrate triggered the parasitic *pnpn* structure.

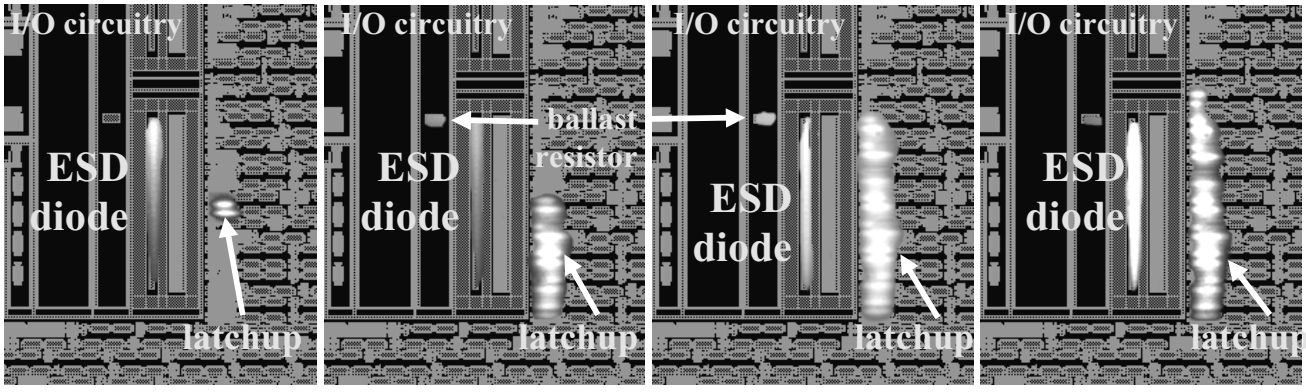
Fig. 7 presents a few examples of electrical test results in the case of negative pin currents, *i.e* current is withdrawn from the pin. Fig. 7(a) shows that the I/O circuitry under test is not prone to latchup and the pin current can be increased in its absolute value to 400 mA without observing abrupt variation of the supply current. A different I/O pin, shown in Fig. 7(b) presents a latchup occurrence for I_{pin} = 70 mA, leading to about a 150 mA "jump" in I_{DD}. Fig. 7(c) represents another I/O pin characterized by two different stable latchup conditions, each occurring for a different value of current extracted from the pin.

4. Optical measurements

After the latchup behavior of all the I/O pins was characterized electrically, a few I/O circuits were chosen for optical inspection by means of light emission. The CCD camera used in the experiments [13] has 1024×1024 pixels, 40 μm × 40 μm each in area, that provide excellent spatial resolution at 100X magnification, for locating latchup emission sources as well as the study of the current diffusion paths in the substrate.

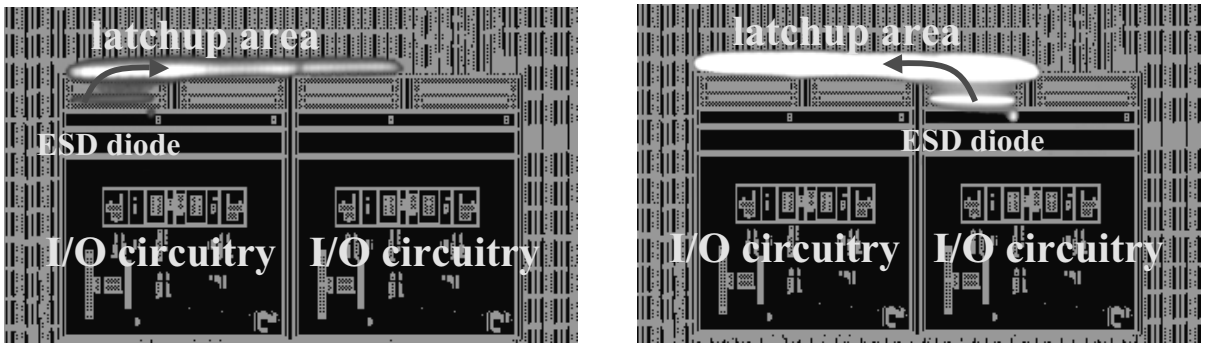
Fig. 8 represents a case study of one I/O circuit: a series of acquisitions was taken at increasing pin current. For each image, a time-integrated acquisition of a few seconds in length was taken of the emission, and then overlaid on the layout of the circuitry in the neighborhood of the cable I/O. During the current injection, the ESD protection diode becomes forward biased, thus emitting a significant amount of light due to electron-hole recombination. Such an emission is very interesting because it can be effectively used to study both the static and dynamic behavior of the ESD structure. The noticeable non-uniformity of the time-integrated emission along the diode provides useful information on the current crowding in the junction, which contributes to limit the efficiency of the diode [3,4]. Picosecond Imaging Circuit Analysis (PICA) [14,15] can also be used to study dynamically the "turning on" of the diode, which has important implications for the limiting signal bandwidth of the I/O [16]. These topics are part of an ongoing study and they will be discussed in a future publication.

Fig. 8(a) shows the emission image corresponding to I_{pin} equal to the critical threshold that ignites the latchup for this specific pin. A bright emission spot appears in the neighboring circuits outside of the I/O circuitry, and some



(a) (b) (c) (d)

Fig. 8. Sequence of time-integrated images of light emission overlaid to the circuit layout. From left to right, the current drawn from the I/O pin is progressively increased, causing the latchup area to grow in size.



(a) (b)

Fig. 9. Latchup emission collected from two different and very sensitive cable I/Os: both pins ignite latchup in the same region, just outside of the I/O circuitry.

faint light is also evident in the area of the ballast resistor inside the I/O circuitry. Since the pin and supply currents are both regulated during the experiment, the latchup can be kept under control in this condition. Moving from left (a) to right (b) in the sequence of images, the pin current becomes more negative. As a consequence, the light emission from the ESD protection diode becomes correspondingly more intense. Concurrently the latchup spreads progressively to cover a larger area of the circuitry surrounding the I/O circuit. Due to a fine regulation of the pin current, Fig. 8(a) shows exactly where the latchup onset occurs, thus permitting localization of the device or structure that is most prone to latchup.

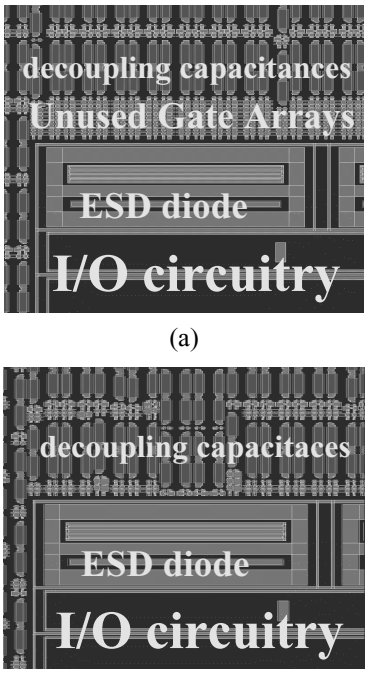
4.1. Primary cause of latchup

In this section we first address the primary cause of latchup ignition. In order to do so, we have looked at different I/Os, starting with those with a low threshold current: Fig. 9 shows the latchup emission related to two of the most sensitive I/O circuits. The light emitted by the ESD diode injecting the current into the substrate identifies the particular pin being stressed: *i.e.* the first on the left hand side for case (a) and the third from the left for case (b). In spite of using two distinct injectors to trigger the latchup, one can note from the images that the latchup always occurs in a very well localized region of the circuit above the I/O circuitry, external to the protection guard ring, thus suggesting that a circuit structure particularly prone to latchup must be present in that area.

To verify such a hypothesis, Fig. 10 shows the layout of the circuitry surrounding two different I/O circuits: (a) one prone to latchup (the same considered in Fig. 9(a)), and (b), one resistant to latchup. Comparing the image in Fig. 10(a) to Fig. 9, one immediately notices that the latchup occurs in an area corresponding to Unused Gate Arrays (UGA).
The UGAs are not employed in logic circuits, but are automatically laid out by the placement tool in the regions not populated by active circuitry around the I/O circuits in order to guarantee good planarity of the circuit and the possibility of logic editing. Decoupling capacitances are usually employed whenever possible, since they also contribute to the overall stability of the chip voltage. However, due to their large size, they cannot uniformly cover the area and therefore the smaller form factor UGA is used to occupy the remaining area. In order to guarantee that such transistors are always turned off, both the source and drain of each device are tied together to the same voltage: ground for the *n*-FETs, and V_{DD} for the *p*-FETs (see Fig. 11). These transistors have twice the number of diffusions biased in the polarity needed to create parasitic bipolar transistors (see Fig. 4), thus making this UGA particularly sensitive to latchup occurrences.

4.2. Latchup in logic circuitry

Although UGA is the primary contributor to the reduction of latchup resistance in the tested I/O circuits, optical acquisitions clearly show that latchup initiated in a UGA



(a)

(b)

Fig. 10. Comparison of the layout of the circuitry surrounding two I/O circuits: (a) prone to latchup and (b) resistant to latchup. The Unused Gate Arrays, shown in Fig. 10(a), are typically the most susceptible to latchup as it was demonstrated by the experimental results in Fig. 9.

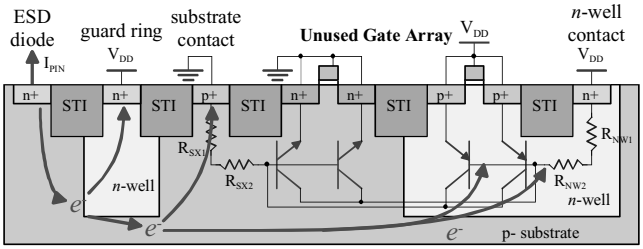
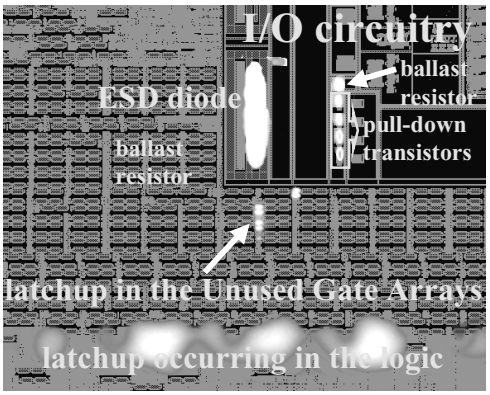


Fig. 11. Unused Gate Arrays (UGA) contain transistors with both source and drain connected to the same potential in order to guarantee that the device is always turned off.

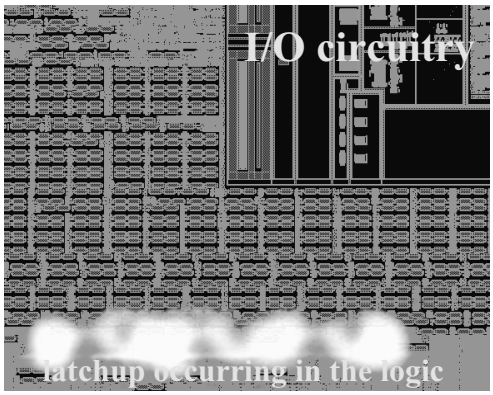
area quickly propagates to regions containing logic circuitry as shown in Fig. 12(a). The UGA acts as a source of injection of minority carriers into the substrate of the chip.

Fig. 12(a) also shows light coming from the 4 pull-down *n*-FETs and the ballast resistor inside the I/O circuitry. Such an emission is related to the negative voltage created at the output node when the current is sunk from the I/O pin. In fact, such a negative drain voltage can cause forward biasing of the drain diffusion or even turn on the transistor, leading to recombination or hot-carrier emission respectively (see schematic in Fig. 13).

Fig. 12(b) leads to another important observation: since in most of the cases the UGA is sparsely distributed, the additional current injection may not be able to easily reach



(a)



(b)

Fig. 12. Since UGA is a secondary source of minority carrier injection, it can trigger latchup in neighboring logic.

a sustainable state (Fig. 9 showed an unusual concentration of UGA). However, once the minority current reaches the logic circuitry, the latchup ignited in this area may stay even after the primary carrier injector (due to the pin current) is removed, and the UGA soft latchup has disappeared.

4.3. Latchup and decoupling capacitances

Fig. 14 shows the case study of a different I/O circuit. When the pin current is raised above the critical threshold, a bright emission area appears in the neighboring circuitry outside the I/O. The latchup region extends to cover the entire part of the circuit limited by a bar of *n*-well substrate (NWSX) contacts above, by decoupling capacitances below, and another I/O to the right of the image. The injected current was not removed during the optical acquisition; therefore the emission from the ESD diode is also visible inside the probed I/O circuit in Fig. 14.

In this section the analysis is focused on the effectiveness of decoupling capacitances in containing latchup, the effect of NWSX contacts are discussed in the next section. Since decoupling capacitances do not contain circuit structures with parasitic bipolar transistors, they are not prone to latchup on their own. However, uncollected minority carriers can diffuse underneath them before recombining, as shown by the faint light emission coming from the region of the decoupling capacitances in Fig. 14. The cross-section of the light intensity is also shown in Fig. 14 and it demonstrates that the carriers can effectively diffuse quite far underneath the decoupling capacitances, dropping in number only in the proximity of the bar of NWSX contacts on the other side. Since the amplitude of such a diffusion tail can be modulated by the intensity of the current injected into the substrate, it would be possible for the latchup to propagate across the line of decoupling capacitances, if enough current were to be injected into the substrate.

In the case of another I/O circuit, shown in Fig. 15, the latchup is seen to actually cross a line of decoupling capacitances thus igniting a latchup event on the other side. It must also be noted in Fig. 15 that the crossing takes place in the only area where a bar of NWSX contacts is not

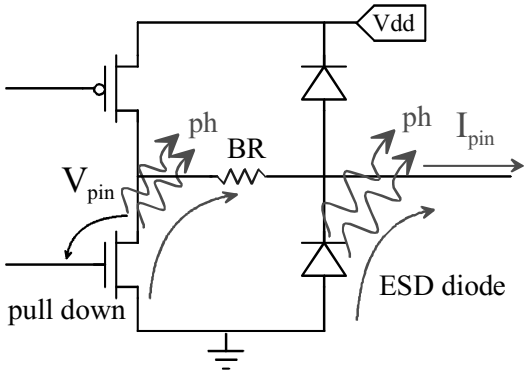


Fig. 13. Schematic of the output buffer showing the ESD protection diodes. High pin current can lead to emission from pull-down transistors and the ballast resistor (BR), aside from that coming from the ESD diode.

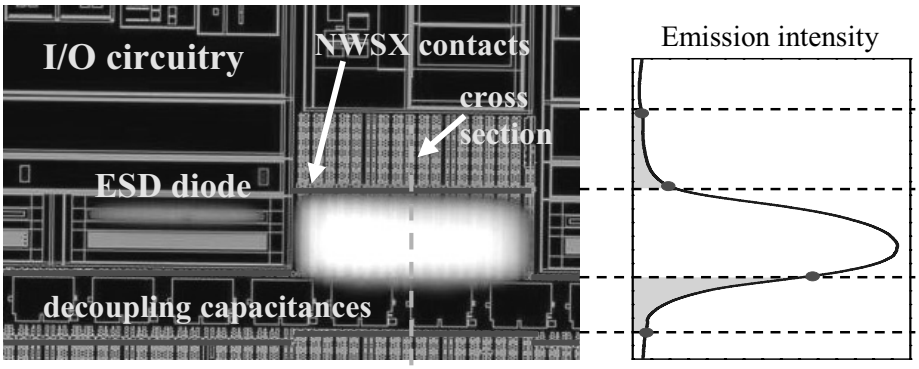


Fig. 14. The latchup area is confined by a bar of NWSX contacts on the top-side and decoupling capacitances on the bottom. The cross-section (along turquoise dashed line) of the emission intensity shows a significant diffusion of minority carriers underneath the decoupling capacitances.

present to act as reinforcement. In fact, the cross-section shown in Fig. 14 also demonstrates that the bar of NWSX contacts below the decoupling capacitances contributes in eliminating (shown by the lack of emission in the area below the decoupling capacitances, as evidenced in the cross-section) the minority carrier concentration, thus allowing for the complete blockage of latchup propagation.

The previous considerations can be used to advise some design practices, including the placing of decoupling capacitance lines between adjacent I/O circuits in order to reduce latchup sensitivity and cross-talk. Although the decoupling capacitances cannot contribute to ignition of the latchup they are not an effective way of stopping the diffusion of minority carriers in the silicon substrate if the recombination distance is not small enough. Other means must be considered where latchup sensitivity is possible, as will be discussed in the next section.

4.4. Importance of NWSX contact periodicity

In the previous section we saw that appropriately placed NWSX contacts are an effective way of stopping the propagation of latchup across an entire circuit (see top NWSX contacts bar in Fig. 14). The primary role of NWSX contacts is the prevention of latchup ignition through the collection of minority carriers injected into the silicon substrate. In addition, the positively biased contacts can be distributed around the I/O circuitry in order to absorb any carriers that go beyond the protection guard ring surrounding the pin. However, if the periodicity of the contacts is too low (the contacts are too sparsely distributed) latchup can take place in unprotected islands where minority carriers may accumulate, as in the case shown in Fig. 14.

Moreover, each NWSX contact has a limited capability of collecting and recombining carriers. In fact, the cross-section of the emission intensity in Fig. 14 shows that there is a significant diffusion tail through the bar of NWSX contacts above the latchup area. If the injected current is increased further, the latchup can effectively propagate to other regions of the circuit as shown in Fig. 16. This explains the possibility of having multiple "jumps" in the chip I_{DDQ} current, seen in preliminary electrical tests and shown in Fig. 7(c), as the pin current is progressively increased. Every "jump" is the result of a different latchup configuration.

4.5. Latchup dependence on I_{DD} compliance

In the previous sections, only the pin current amplitude was used as a parameter for studying latchup sensitivity. However, power supply current compliance, I_{comp}, is another important factor in determining the final state of the latchup. Before a latchup event takes place, the minority carrier concentration in the substrate, responsible for latchup ignition, is controlled only by the pin current injected into the silicon substrate by the ESD protection diode and by the efficiency of the protection guard ring and NWSX contacts in collecting and recombining electrons. Therefore, I_{comp} does not have any effect in the determination of the I_{pin} threshold that leads to latchup.

However, after the parasitic *pnpn* structure is turned on in a conducting state, I_{comp} may contribute by determining the total amount of current flowing from V_{DD} to ground, through the silicon substrate. As already discussed, since such a current is a secondary contribution to the injection of electrons into the substrate, it may aid the latchup to diffuse further, thus determining its configuration (in terms of affected circuitry), extension (in terms of area) and damage to the circuit (soft latchup, permanent destruction).

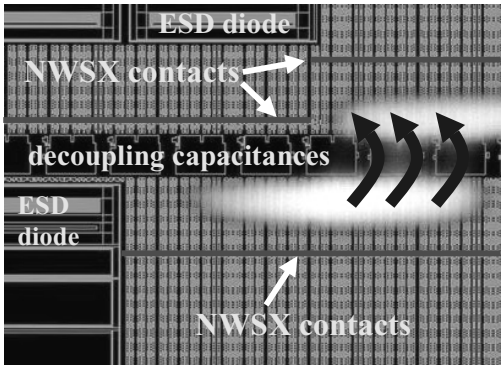


Fig. 15. Minority carriers can cross lines of unprotected decoupling capacitances and trigger a latchup event on the other side.

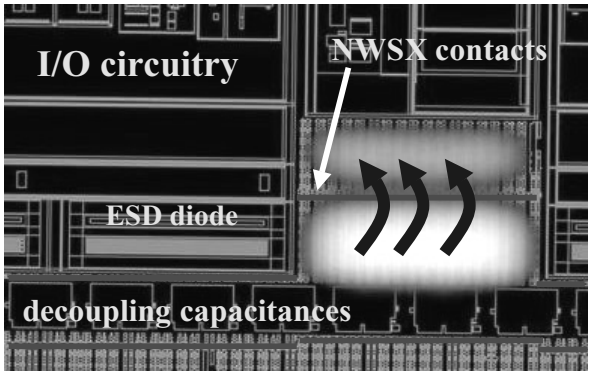


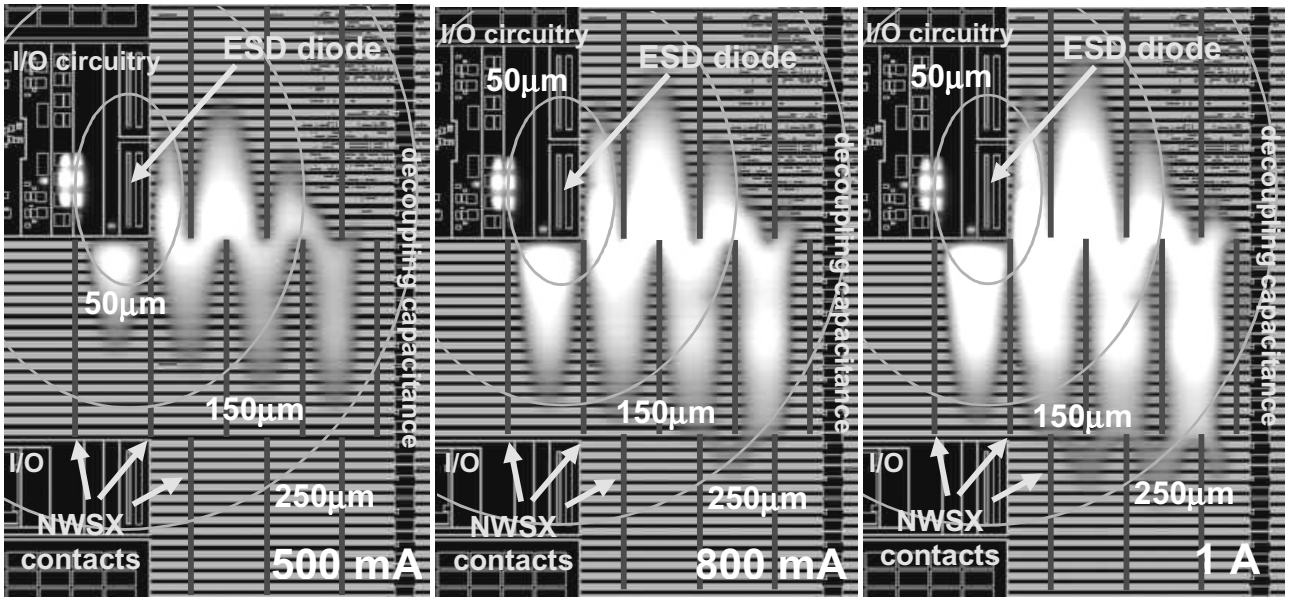
Fig. 16. Due to inadequate NWSX contact periodicity and its simple linear layout, latchup can propagate towards different regions of the circuit as the injection of minority carriers is increased.

Fig. 17 presents a sequence of images taken at a fixed pin current (400 mA) while increasing the power supply compliance, I_{comp}. The images are self-explanatory and show that the extent of the latchup area grows as I_{comp} increases. More specifically, at I_{comp} = 500 mA, the latchup reaches circuitry well over 200 µm away from the original injector (in accordance with the diffusion lengths for the technology), the ESD protection diode on the top left hand side of the images. A range of 200 µm had been considered, through study of prior art, to be the maximum distance from the injector at which latchup effects would take place. It thus defined both a safe distance at which to place logic circuits, and also the size of the "bounding box" to be used to avoid concurrent placement of many injector sources, from different I/O circuits, in the same area. Fig. 17 clearly shows two I/O circuitries within 200 µm of each other: the placement of bars of NWSX contacts is unable to keep the minority carriers away from the second I/O circuit, shown below the one being probed (it could potentially latchup).

Latchup can propagate such distances from the injector of minority carriers for two reasons: low NWSX contact periodicity and high power supply compliance. Due to the inadequate density of NWSX contacts, a high density of minority carriers can build up in the space between two neighboring NWSX contact bars, thus igniting a sustained latchup there. Due to the high compliance current, each one of these latchup areas then becomes an important source of minority carriers in the silicon substrate, leading to the ignition of adjacent regions. Such a diffusion of the carriers among different zones is also made easier by the discontinuity of the vertical bars: they do not overlap each other, from top to bottom. Fig. 17 clearly demonstrates that the carriers can sneak through these apertures and "slalom" around the bars of NWSX contacts. A higher periodicity and a more uniform distribution of NWSX contacts over the entire area around the I/O circuits would be very helpful in preventing the formation and diffusion of latchup.

4.6. Latchup dependence on temperature

Besides pin current and supply voltage level temperature is another important parameter that affects the latchup sensitivity of the chip. Fig. 18 shows a study of latchup sensitivity as a function of the chip temperature. Since the operating temperature of the chip is in general significantly higher than room temperature, the latchup measurements should be performed at the higher temperature for the worst-case scenario. In order to simplify the experimental setup, and to extract an approximation of latchup sensitivity, characterizations can be performed at room temperature and corrected using equations similar to the one presented in Fig. 18.



(a) (b) (c)

Fig. 17. Sequence of latchup images for different values of power supply compliance: (a) 500 mA, (b) 800 mA and (c) 1 A. Lines of equidistance from the injector source are shown at 50, 150 and 250 µm.

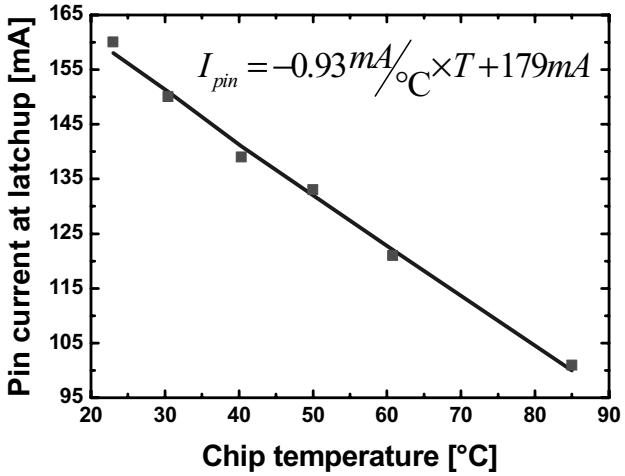


Fig. 18. Latchup susceptibility increases as the operating temperature of the chip is increased: the squares represent measured currents while the line is a fit to the experimental data.

5. Conclusions

By means of this novel adaptation of the JEDEC78 testing procedure, an automated computer controlled latchup test program was developed. Emission microscopy was used to characterize the ignition and diffusion of latchup in a series of I/O pins of a test chip. Many different I/O environments were examined in order to evaluate latchup sensitivity in bulk technology for applications where I/Os can be subject to voltage spikes during operation.

The circuit structures and devices that are most prone to latchup were first localized and then identified. In particular, Unused Gate Arrays (UGAs) placed in the neighborhood of the I/O circuits are shown to be very susceptible to latchup, due to the characteristic bias of their source and drain diffusions. It was also demonstrated that the latchup in the UGA can act as a secondary source of minority carriers, leading to latchup in logic circuitry. A simple solution is to remove any UGA structure from around I/O circuitries and substitute it with NWSX contacts whenever possible.

It was also shown that minority carriers can diffuse underneath lines of decoupling capacitances, if the recombination length of the minority carriers is comparable with the size of the capacitances. Although they are immune to latchup, decoupling capacitances cannot be used alone to slow down its propagation. New NWSX contacts guidelines, leading to a higher periodicity of the contacts as well as a more random or "grid-shaped" placement of the contacts instead of the standard bar structures, were implemented in a new version of the test chip. This new approach prevents the formation of unprotected areas and impedes any diffusion paths. The final result of the optimized layout/floorplan experiments lead to latchup robustness exceeding the ±400 mA DC triggering current: latchup will not occur before metal lines connected to the I/O melt due to excessive current. These results were achieved on a 1-2 Ω-cm *p*-type wafer without the use of *deep* trenches or *deep n*-well.

More work activities are in progress aimed at understanding the dynamic ignition and evolution of ESD and latchup in the time domain by means of the Picosecond Image Circuit Analysis (PICA) technique [16].

6. Acknowledgments

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