Power Amplifiers

Objective

There is not a 'universal' amplifier suitable for all applications. Design in general, and amplifier design in particular, involves tradeoffs between different aspects of amplifier operation, emphasizing performance in some of these aspects at the expense of performance in others. These notes are an <u>introduction</u> to 'power' amplifiers, i.e., amplifiers intended to provide the power necessary for operation of various devices in a controlled manner. A familiar illustration is the translation of electrical energy into dynamic motion of a loudspeaker cone, moving air so as to recreate a pattern of sound pressure previously translated into an electrical signal. A very small broadcast signal is amplified and ultimately a higher-power copy of the signal is used to drive the speaker.

The final (power) stage of amplification has a context different in general from the earlier amplification stages. For example the output load for an <u>interior</u> stage generally is under the control of the circuit designer, whereas the final stage faces a load not entirely under this control and more often than not different from one application to another. This independence is potentially hazardous since, if something goes awry, the power level involved often is sufficient to be physically destructive of output devices. This has not been a major concern in previous discussions of amplifiers because very low power levels were considered

Efficiency is another matter of concern. Small-signal amplifiers are extraordinarily energy inefficient; this is a tradeoff against other performance considerations. The low power levels typically involved mitigate consequences of this inefficiency. That is generally not the case with power amplifiers.

Our evolutionary presentation starts with a straightforward quasi-historical extension of the basic amplifier design considered earlier. Then limitations of the design are examined, and circuit modifications are made specifically to improve performance at higher power levels. Illustrative computations are provided.

Class A Amplifier

A 'Class A' amplifier is one for which all devices remain in the normal active region at all times while amplifying bipolar input signals. Class A power amplifiers basically involve the same basic principles as were considered previously for discussing incremental parameter amplification. The distinction made is that <u>large-signal</u> operation is involved, and because of this a special importance attaches to performance characteristics of less concern for small-signal operation. The principal interest here is in efficiency, although other considerations, e.g., distortion, also can be important.

For incremental-signal amplifiers detailed power calculations are not particularly important. Indeed small-signal amplifiers typically are quite energy inefficient.   One reason for small-signal power amplifier inefficiency, for example, is the need to locate the quiescent point so as to support amplification of bipolar signals. Thus even in the absence of a signal input there is a relatively substantial DC collector power dissipation associated with the quiescent point current and voltage. However because the power level involved is generally quite small efficiency is traded-off for other benefits.

We begin consideration of power amplifiers by considering a familiar circuit in circumstances where collector dissipation becomes significant.

Class A CE Amplifier

To begin the discussion consider the CE circuit configuration drawn below, left. Actually this is not a circuit configuration that is likely to be much used in practice for reasons to emerge. However it is familiar and useful as a model to review power calculations, and to initiate the evolutionary presentation to follow. It is intended to provide a review of principles rather than as an illustration of an important circuit.
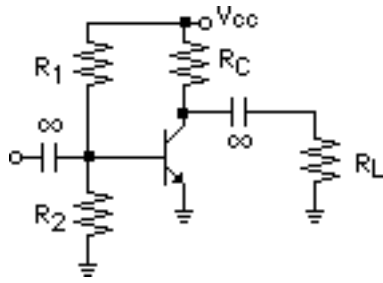
Concern about dissipation and efficiency becomes important when the amplified signal amplitude is large, and this is the context for the following discussion.   For later reference take explicit note that the amplifier load resistor here is R_L, i.e., the _useful_ power expenditure is presumed to occur in R_L. On the other hand R_C is present because of a biasing requirement; it is needed to define the quiescent collector voltage so that there is 'room' for bipolar signal voltage changes at the collector.

Certain simplifications are commonly made in studying analytically the _general_ behavior of this circuit. For example the BJT characteristics are assumed to be adequately represented by a 'flag' model, for which the collector current is ß (assumed constant) times the base current. This neglects entirely the small saturation voltage range of the transistor, with the effect of overstating somewhat the allowable collector voltage swing. Similarly the non-linearity in amplification at very low and very high currents is ignored, i.e., the transistor characteristics are assumed to be parallel lines, equally spaced for equal base current increments, with zero reverse bias leakage current. Here it is the allowable current swing that is somewhat overstated. These assumptions simplify an analysis considerably without major numerical consequences. Ultimately of course a computer numerical analysis incorporating a more detailed nonlinear device model fine-tunes a design derived using broad principles obtained from a study of the simplified model.

The I_C -V_{CE} plane for the CE amplifier collector characteristics is shown in the figure to the left; the (flag) transistor collector characteristics themselves are not drawn explicitly. Because the AC circuit is different from the DC circuit there are two load lines to consider. The DC load line and the DC base bias current establish the quiescent point. The equation describing the DC load line is $V_{CC} - V_{CE} = I_C R_C$. The DC load line and the Q point are as shown in the figure.
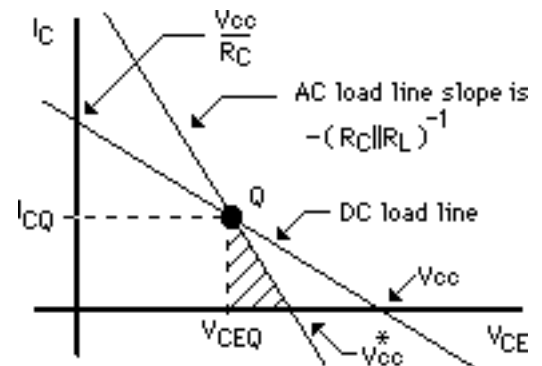
Incidentally note that, primarily as a simplification, emitter stabilization is not used. Generally the use of an emitter resistance would be avoided because to be effective it would also contribute significantly to the standby power dissipation. For modest (millewatt) power levels emitter stabilization possibly might be acceptable, and the inefficiency accepted in exchange for inexpensive simplicity. The analysis following can account for an emitter resistance adequately simply by considering the emitter and collector resistances to be in series; note that the emitter and collector currents will be very nearly equal assuming a reasonably large value for ß.

The AC load line describes the relationship between _changes_ in collector current and _changes_ in collector voltage. Whereas the DC load line has a slope inversely proportional to R_C the greater AC load line-slope is inversely proportional to $R_L\|R_C$. Since considerations of efficiency (more precisely maximum current transfer into the load) generally means $R_L < R_C$ there can be a significant difference in slope. The AC load line also is shown in the figure also; it is defined by its slope and the Q point (through which it passes). Note that the intercepts of the two load lines with the abscissa are labeled V_{CC} and V^*_{CC} respectively.

For maximum symmetrical output voltage and current swing (ignoring saturation and current constraints as noted before) the Q point should lie at the 'middle' of the _AC_ load line, i.e., make $2V_{CEQ} = V^*_{CC}$ and $2I_{CQ} = V^*_{CC}/ (R_C\|R_L)$

The shaded triangle in the figure reveals that $V^*_{CC} -V_{CEQ} = I_{CQ}(R_C\|R_L)$. Hence choose

$$V^*_{CC} = 2V_{CC}\frac{R_L}{2R_L+R_C} = 2V_{CEQ} \quad \text{and} \quad I_{CQ} = 2V_{CC}\frac{R_L+R_C}{(2R_L+R_C)R_C}$$

to locate the Q point as desired.

Note that, as expected (why?), $I_{CQ} \to V_{CC}/(2R_C)$ as $R_L \to$

The DC power provided by the supply is given by the product of the average current (here the Q point current because of the symmetrical variation assumed about the centrally placed Q point) and the DC supply voltage:

$$P_{DC} = V_{CC}I_{CQ} = \frac{V^2_{CC}}{R_C}\frac{R_L+R_C}{2R_L+R_C}$$

Note that $P_{DC} \to V^2_{CC}/(2R_C)$ as $R_L \to$

The average sinusoidal power in R_L (not R_C) is

$$P_{AC} = \frac{1}{2}\frac{V^2_{CEQ}}{R_L} = \frac{V^2_{CC}}{2R_L}\left(\frac{R_L}{2R_L+R_C}\right)^2$$

The instantaneous collector power dissipation is $I_CV_{CE} = I_C[(R_C\|R_L)(I_{CQ} - I_C)+V_{CEQ}]$. Note that the power I_CV_{CE} always is positive, and that the expression is zero for $I_C = 0$ and also for $I_C = I_{CQ}+V_{CEQ}/(R_C\|R_L)$. It follows that the dissipation is a maximum somewhere between these intercepts. That maximum occurs at $I_C = I_{CQ}$ and is $I_{CQ}V_{CEQ}$. This is not unexpected, since the <u>fixed</u> power provided by the supply is dissipated in the resistors and in the collector. Hence increasing the dissipation in the load resistor <u>necessarily</u> reduces the collector dissipation, and so the maximum value of the latter occurs in the absence of an AC signal, i.e., at $I_C = I_{CQ}$. Contrary to the likely first impression the transistor operates cooler with a signal present than without one!
A useful 'figure of merit' for the transistor is

$$\frac{\text{Peak Collector Dissipation}}{P_{AC}} = 2R_L\frac{I_{CQ}}{V_{CEQ}} = \frac{2R_L}{R_C\|R_L} = 2\left(1+\frac{R_L}{R_C}\right) > 2$$

meaning among other things that to survive the transistor selected for use in the Class A amplifier must be capable of dissipating <u>more</u> than twice the power that can be transferred to the load.

Another, perhaps more familiar figure of merit is the conversion efficiency:

$$\text{Efficiency} = \frac{P_{AC}}{P_{DC}} = \frac{1}{2}\frac{1}{\left(2+\frac{R_L}{R_C}\right)\left(1+\frac{R_C}{R_L}\right)}$$

This has a (broad) maximum at $R_C = 2R_L$; the maximum is 8.6%. The efficiency is 6.67% at $R_C/R_L = 2$, and 8.3% at $R_C/R_L = 0.5$.

<u>Note :</u> A special case often used as an illustration makes $R_L \to$, i.e., R_C not only defines the quiescent collector bias voltage but it is assumed also to be the load resistor. In this case the DC and AC load lines are the same. The DC power is $V_{CC}(I_{CQ}/2)/R_C$ and the AC power (in R_C) is 1/4 of this. The efficiency 'rises' to 25%. This increase in efficiency is a consequence of not having to split the AC collector current between R_C and R_L, i.e., the total AC power is 'load' power. Unfortunately putting the load resistor in

the collector is not often feasible. It is worth again asserting that Class A amplifiers of the sort described generally would be used only at low power levels where inefficiency is less of a concern.

Class A CE Amplifier Illustration

What follows is a PSpice analysis of a modified version of the Class A amplifier described above. In that previous description, as a pedagogical simplification, we passed over the important matter of stabilizing the collector current. Using emitter stabilization, for example, adds to the power dissipated and so lowers the efficiency achievable. Another matter noted concerned the division of AC collector current between the load resistor and the collector resistor, reducing the signal transfer into the load.
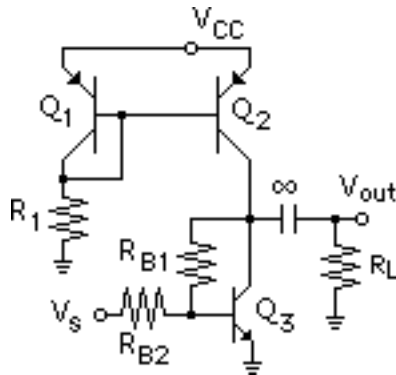
It happens that both limitations can be addressed theoretically simply by replacing the collector resistance by a DC bias current source; the bias current is constant (ideally) by definition, and therefore all the AC collector current flows to the load resistor!

In practice a good approximation to a current source is provided by the Q_1, Q_2 sub-circuit in the amplifier circuit diagram drawn to the right. The diode-connected transistor Q_1 copies its emitter current to a matched Q_2 device to provide the DC bias current for Q_3. Provided V_{CC} is stabile and is large compared to the Q1 diode drop Q2 provides a stabile collector bias current for Q3.

In addition Q3 collector feedback is used to define the quiescent collector voltage.

Roughly (neglecting the Q3 base current) the DC voltage drop across RB1 is approximately $0.7(R_{B1}/R_{B2})$; the resistance ratio is chosen to set the DC collector voltage to about $V_{CC}/2$. Actually, of course, some allowance must be made for a minimum of about one volt for the Q2 collector-emitter voltage so that Q2 is not saturated. A similar allowance is needed for Q3.

The theoretical analysis of this modified configuration is essentially the same as before, except that the slope of the AC load line now is $-R_L^{-1}$; to the extent Q2 acts as a current source R_C is effectively infinite, and the DC load line is vertical. The theoretical maximum efficiency becomes 25%.

```
*Class A CE Illustration          RL    5    0           50
*Current source                   RB1   3    4           330
R1    1    0           100        RB2   4    6           82
Q1    1    1    2    Q2N3906       VS    6    0      SIN(0 1 1K 0 0 0)
Q2    3    1    2    Q2N3906
VCC   2    0    DC    10           .LIB EVAL.LIB
                                   .TRAN      .01U 2M
*CE + load                         .OP
Q3    3    4    0    Q2N3904        .PROBE
CL    3    5         100U           .END
```

Estimates can be made for a number of parameters of interest, and compared to PSPICE computation results.

With V_{CC} = 10 volts the Q1 and Q2 emitter currents could be estimated as (10-0.7)/100 or 93 ma. Note that the actual Q1 emitter junction voltage is somewhat larger than the 0.7 volt approximation because of the high current involved, but because of the exponential diode relationship the estimate still is fairly good. Similarly the Early Effect in Q2, while small, nevertheless is significant because of the high current involved.

It is necessary to assure explicitly the collector voltage assumes the proper value since the 'current source' voltage drop is determined by the circuit. Provided we make the current through R_{B1} large compared to

the Q3 base current R_{B1} and R_{B2} can be considered (roughly) a voltage divider with approximately 0.7 volts across R_{B1}. From this an estimate can be made of resistance values to use to fix the DC collector voltage. First estimate the voltage swing from the DC collector current (equal to the peak AC current allowed); with RL equal 50 and an estimated bias current of 93 ma this is 4.65 volts. However to avoid excessive distortion at low currents and saturation at high currents a smaller peak current swing is required. The resistor values used indicate a collector bias of 3.5 volts for a junction voltage of 0.7 volt. Actually a somewhat higher emitter junction voltage and so higher collector voltage can be anticipated because of the high current. For example a emitter bias of 0.8 volt brings the estimate to 4 volts. Computed values for transistor operating parameters, and for the node voltages, are shown below:

|	Q1 Q2N3906	Q2 Q2N3906	Q3 Q2N3904
IC	-8.93E-02	-1.12E-01	1.01E-01
VBE	-8.52E-01	-8.52E-01	8.16E-01
VCE	-8.52E-01	-5.59E+00	4.41E+00

NODE VOLTAGES
(1) 9.1475   (2) 10.0000   (3) 4.4148   (4) .8161   (5) 0.0000   (6) 0.0000

It is worthwhile to be reminded at this point of the purpose of the simplified model used to make the estimates. That purpose is to obtain in a relatively simple manner 'ballpark' information from which to propose circuit element values sufficient to perform a computer analysis using a more precise circuit model. It is instructive to consider this illustration from a design point of view.

The computed transistor currents are plotted below. The Q1 collector current is constant as expected at 89ma (compared to 93ma estimated). In the simplified model the Q2 collector current would be the same as the Q1 current. However this ignores the Early effect. Because of this effect there is a somewhat higher Q2 DC current (higher collector bias), and the Q2 collector voltage signal variation introduces a small AC current component (about 10 ma peak out of a nominal 110 ma average). The Q3 collector current is essentially that produced by the signal, and virtually all this current transfers to the load.

The estimated peak AC voltage that would be expected is about 93 ma x 50   4.64 volts. For reasons noted before this estimate is on the high side. The AC output for the specified input voltage is 3.3 volts; note that the signal transfer linearity is good. If Q3 is recognized as forming an inverting amplifier, and if it is considered (as a very rough approximation) to be an idealized opamp then from the feedback estimate the gain to be -(330/82) = - 4. Since the single-stage inverter is not likely to have too high a gain the gain with feedback actually would be smaller than estimated. Note that the input voltage magnitude is 1 volt, so that the actual voltage gain is -3.3.

The load power is $(0.5)(3.3)^2/50 = 0.11$ watts. The DC supply current is the average of the sum of the Q1 and Q2 emitter currents, about 200 ma. The source power then is about 2 watts and the amplifier overall efficiency is about 5.5 %.
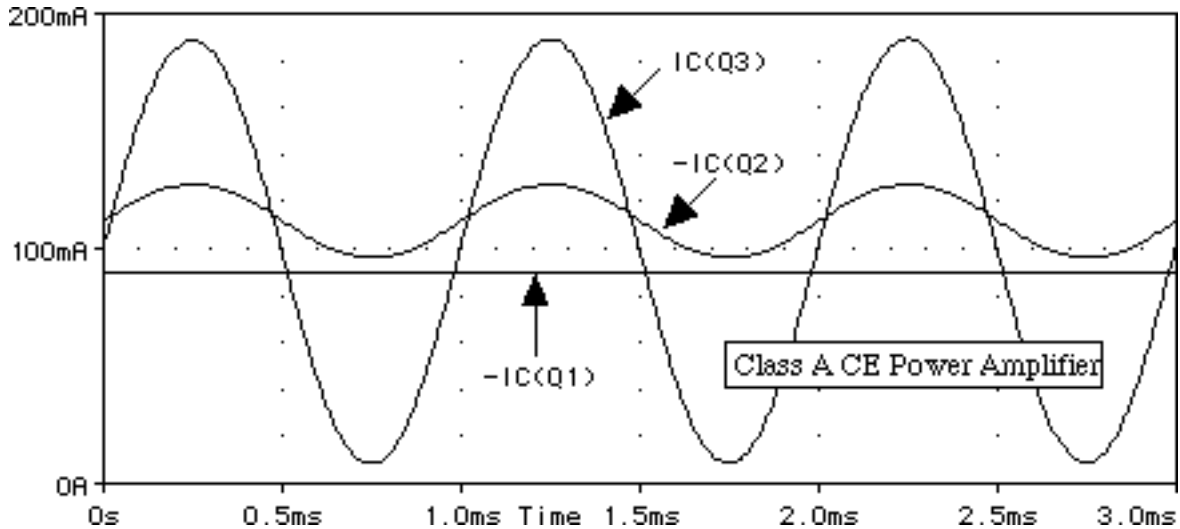
Class A Emitter-Follower Amplifier

An advantageous alternative to the CE configuration is that of an emitter follower, i.e. the CC configuration. This configuration, it will be recalled, provides an enhanced incremental input resistance, thus (ideally) isolating the amplifier input from the output. The amplifier provides nearly unity voltage gain and a current gain of (approx.) ß.

The circuit is conveniently simplified for analysis in a manner similar to that used for the CE analysis, i.e., assume idealized 'flag' model characteristics which neglect the small saturation voltage range and the low-current non-linearity. The 'simplified' load line characteristics are drawn to the right in the figure below.
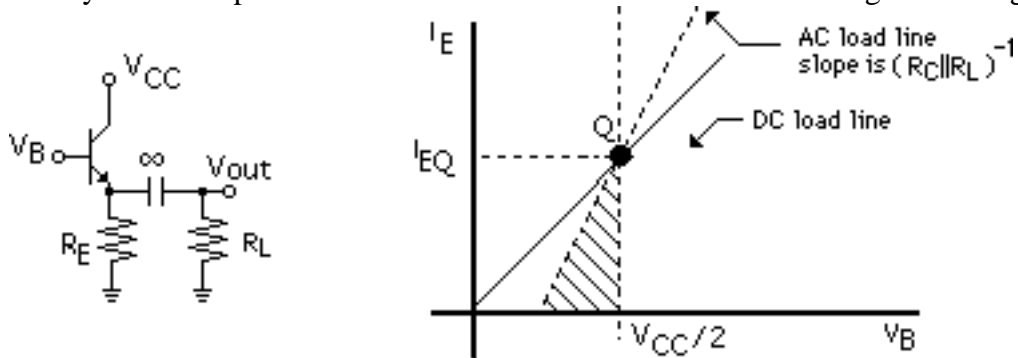
We pass over the analytical details, leaving their derivation for an exercise. They are similar to those for the basic CE configuration, and show a not unexpected poor performance as a power amplifier for reasons similar to those for the CE analysis. Instead we examine a circuit modification similar to that made above to improve performance.

A major inefficiency of the basic CC configuration is associated with the use of R_E to provide an emitter bias that allows symmetrical output voltage swings. Not unlike the CE case it would be desirable if R_E were a short-circuit for DC current (no DC dissipation) but an open-circuit for AC current (entire AC current transferred into R_L). While a resistor itself does not provide this kind of dichotomy a current source can, as in the circuit drawn to the right.
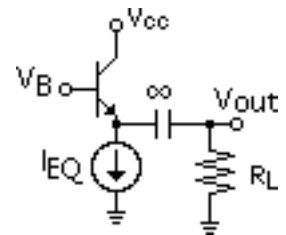
The DC load line (see figure) is horizontal since the emitter current is fixed, and clearly the Q point should be set (ideally) at $V_{CC}/2$ to maximize the allowable output voltage swing. Because the slope of the AC load line is smaller (R_E is effectively infinite) the symmetrical voltage swing possible is increased over what it would be with an emitter resistor. The basic analysis procedure is similar to that presented before; several conclusions are listed, with their verification left as an exercise.
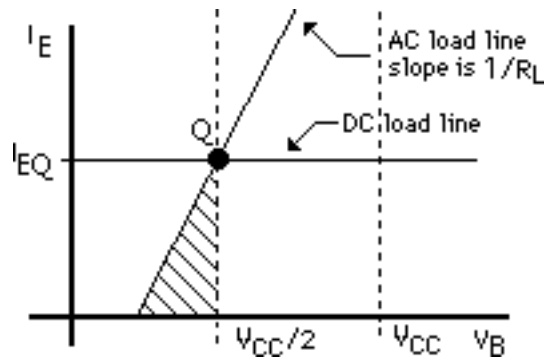
Max <u>AC</u> current magnitude is I_{EQ}.
Max AC voltage (from shaded triangle) is $I_{EQ}R_L$.
Max average load power P_{AC} is
$(I_{EQ})(I_{EQ}R_L)/2 = (I^2_{EQ} R_L)/2$.
$P_{supply} = I_{EQ} V_{CC}$
Incremental voltage $v_{ce} = V_{CC} - v_b = V_{CC} - i_e R_L$ (i_c i_e)
Instantaneous collector power dissipation is $P_{col} = i_e (V_{CC} - i_e R_L)$\
        (Note that $i_e R_L$ $V_{CC}/2$ to avoid saturation)

Maximum P_{col} occurs for $i_e R_L = V_{CC}/2$ and is $V^2_{CC}/(4R_L)$

Efficiency $= P_{AC}/P_{DC} = \{(I^2_{EQ} R_L)/2\}/I_{EQ} V_{CC}$;
Maximum efficiency occurs when $I_{EQ} R_L = V_{CC}/2$, and the maximum is 25%\

Note that the current source also dissipates energy, in the amount ($P_{supply} - P_{AC} - P_{col}$) for which the maximum value (at maximum load power) is equal to the load power! Hence the transistor used must be able to dissipate twice the maximum load power available.

Emitter Follower Illustration

The circuit to be analyzed is drawn to the right. The diode-connected transistor Q1 defines (ideally) a fixed emitter current in Q_1, and to the extent that Q_1 and Q_2 are matched this is the emitter current in Q_2; with ß >> 1 it is also the emitter current for Q_3. (Actually, not quite. The collector voltage change for Q2 is relatively large, and there will be some Q2 Early Effect collector current variation.) The Q_1 and Q_2 arrangement provides effectively a current source to bias Q_3. Circuit parameters are provided in the netlist following. However device and parameter choices are not made capriciously.
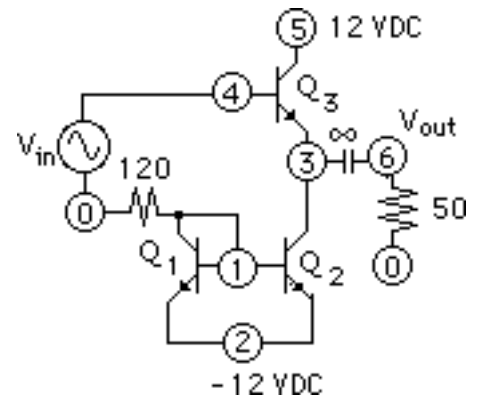

Normally device and parameter selection would be based on the functional specification of the desired amplifier performance. For various parochial reasons of convenience however the transistors used all are specified as 2N3904 NPN devices. This limits transistor dissipation (per manufacturer's device specifications) to roughly 0.5 watt average, and (separately) to a collector current of about 200 ma maximum. Since the collector dissipation will be at least twice the load power the allowed average load power to be permitted is about 0.25 watt.

The load is specified here more or less arbitrarily as 50 . Ordinarily the desired load power would dictate the choice of transistor. Here the transistor dictates the maximum load power. For 0.25 watt dissipation the <u>peak</u> current required would be about 100 ma. With 100 ma the peak AC output voltage magnitude to be anticipated is about 5 volts. The PSpice analysis results follow.

```
*Class A Emitter Follower Illustration
R1          0   1           120             .LIB EVAL.LIB
Q1          1   1   2       Q2N3904         .TRAN      20U  20M 0 20U
Q2          3   1   2       Q2N3904
Q3          5   4   3       Q2N3904         .OP
VIN         4   0   SIN(0 5 1K 0 0 0)       .PROBE
CL          3   6           100U              .END
RL          6   0           50
VCC         5   0   DC      12
VEE         2   0   DC      -12
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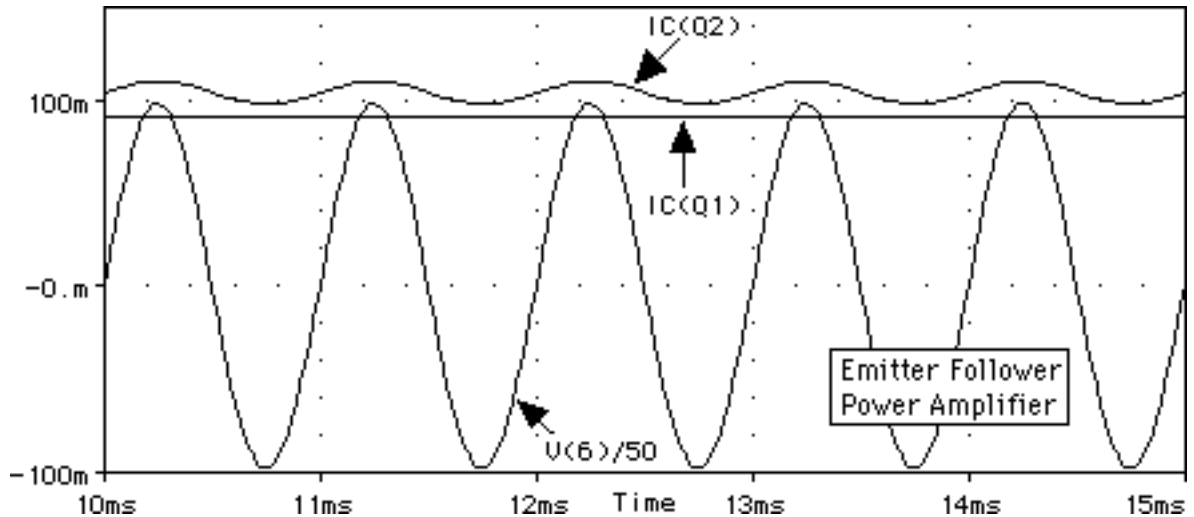

	Q1	Q2	Q3
IB	8.83E-04	8.83E-04	8.49E-04
IC	9.15E-02	1.04E-01	1.03E-01
VBE	8.13E-01	8.13E-01	8.12E-01
VBC	0.00E+00	-1.04E+01	-1.20E+01
VCE	8.13E-01	1.12E+01	1.28E+01

NODE VOLTAGES
(1) -11.1870   (2) -12.0000   (3) -.8119   (4) 0.0000   (5) 12.0000   (6) 0.0000

Incidentally the signal source current is 0.8485E ma. The load current is a nominal 100 ma, reflecting a sizeable current and so power) gain.

Transformer-Coupled Class A Amplifier
In the CE Class A amplifier circuit configuration the collector resistor is selected to allow maximum symmetrical voltage swing about the quiescent operating point. If the resistance is too large there is excessive dissipation by the quiescent current; indeed the low efficiency of the circuit is due primarily to just this dissipation. On the other hand if the resistance is too low the AC collector current division into the load resistor is likely to be degraded. This tradeoff is evident in the expression for the efficiency, which depends both on the ratio RC/RL and also on the inverse ratio RL/RC. In other words it is desirable that concurrently both $R_L > R_C$ and $RC > R_L$! One response to this need is to use a current source, as illustrated before. There is another approach that can be taken, transformer coupling, although it is used comparatively infrequently in current electronic practice. Nevertheless a general appreciation of the subject is instructive, and it is in that spirit that the following terse review is presented.

To repeat, what would be useful is a collector 'resistor' which has a large AC resistance to improve the transfer of AC collector current into the load, but concurrently a small DC resistance to reduce losses in establishing the Q point. The inductor is a AC circuit element with just this general property, if one reads

'inductive reactance' for 'resistance'.   Ideally the DC winding resistance of the inductor is quite low, while the AC reactance can be large (depending on the signal frequency and the inductance).

The circuit diagram below, to the left, illustrates the modification suggested by introducing a 'choke', a relatively large inductance, in the collector. More common however is the closely related transformer-coupled load configuration to the right. The transformer provides ancillary benefits, e.g., the ability to vary the slope of the collector load line for a fixed load resistor by using an appropriate transformer turns ratio. The DC isolation of the load from the collector also can be useful, and of course a transformer allows a step-up or step-down voltage transfer.
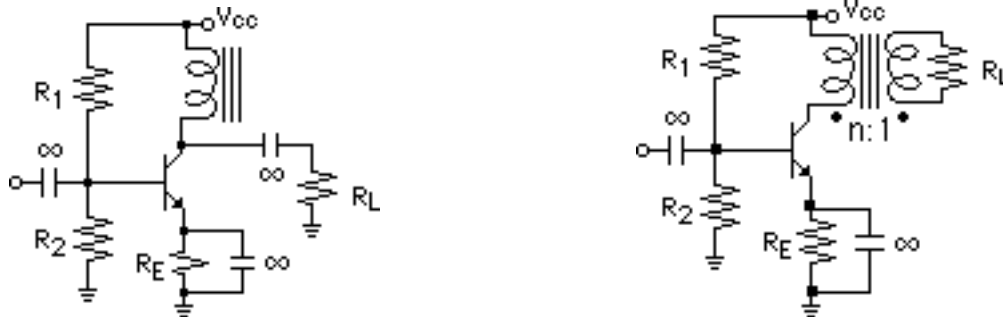
A load-line analysis for the (transformer) circuit is shown in the diagram below. Note carefully the distinction between the 'DC' load line and the 'AC' load line corresponding to the frequency-sensitive collector reactance. The distinction is more easily recognized if it is kept to mind that the load line is the graphical expression of the relationship between the collector current and the collector voltage.

Thus, for example, the DC load line is $V_{CE} = V_{CEQ} = V_{CC}$, i.e., the collector DC voltage is fixed. There is zero DC voltage drop across the (assumed lossless for simplicity) transformer primary.

On the other hand for the AC signal the transformer couples an effective resistance of $n^2 R_L$ into the primary; where n is the turns ratio of the transformer. Hence the AC load line, describing the relationship between changes in collector current and changes in collector voltage, has a slope equal to $-(n^2 R_L)^{-1}$. Since the AC load line passes through the Q point (zero-change point) the load line is located as shown in the figure. The equation for the AC load line is

$$V_{CE} - V_{CEQ} = - n^2 R_L (I_C - I_{CQ})$$
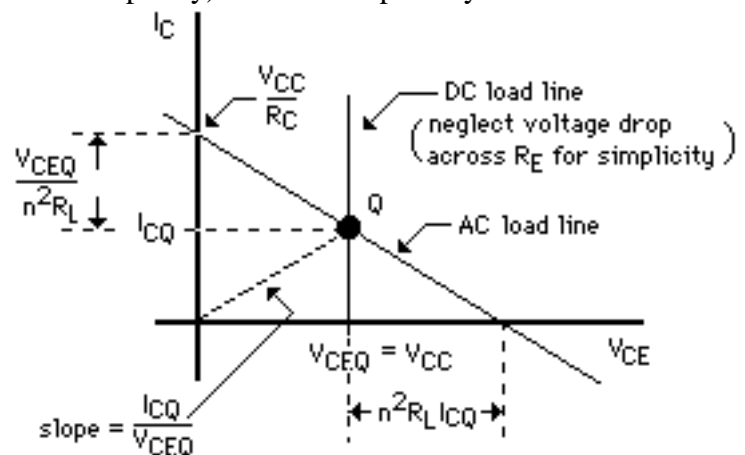
Ordinarily load resistance would be determined by the nature of the application and the turns ratio then would be specified to reflect that resistance into the transformer primary to provide the desired load line slope. For a symmetrical voltage swing (ignoring saturation and low-current nonlinearities) choose the turns ratio n so that

$$V_{CEQ} = n^2 R_L I_{CQ}$$

The DC (supply) power is

$$P_{DC} = V_{CC} I_{CQ} = \frac{V_{CEQ}^2}{n^2 R_L} = \frac{V_{CC}^2}{n^2 R_L}$$

and the AC load power is

$$P_{AC} = \frac{1}{2} \frac{V_{CC}^2}{n^2 R_L}$$

Note that the collector dissipation capability required still is twice the AC load power. If transformer losses are ignored the efficiency is 50 %. The increase in theoretical efficiency is primarily the result of eliminating the dissipation which would be produced by the quiescent current flowing through a collector resistor.

Illustration
An illustrative transformer-coupled power amplifier circuit is drawn to the right.

The output load is an 8 Ω speaker, with a maximum average power of 0.25 watt (nominal) to be provided (limited by the allowable collector dissipation of the 2N3904). This calls for a peak load voltage of 1.4 volts.

A √6:1 turns ratio (nominal) is assumed so that the resistance reflected from the secondary is ≈ 50 Ω. This choice is conditioned by the fact that it makes the intercept of the load line on the abscissa about 12/50 = 240ma. While this is a bit larger than the 200ma maximum current constraint for the 2N3904 avoidance of saturation will limit the current to less than the intercept value.
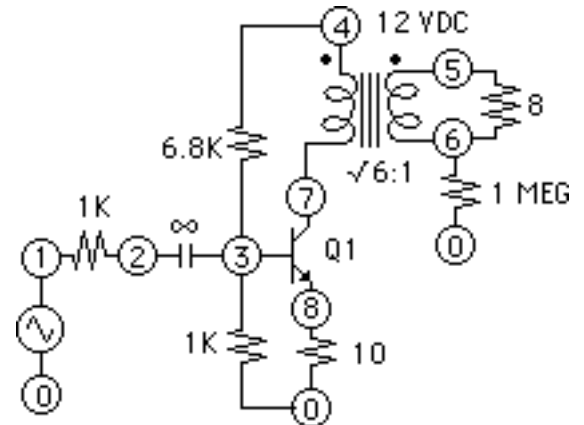
The biasing is designed for a quiescent current of 100 ma nominal. Estimate from a rough PWL calculation the input voltage transfer loss as a factor of 1/3, and a voltage gain ('fixed' by the series-series feedback) to be about 5. For a nominal 5 volt peak AC voltage across the transformer primary (allowing some for the voltage drop across the emitter resistance, and for saturation) the input voltage required is about (3/5) 5, or 3 volts. Note that this is a preliminary estimate that can be refined readily after a trial PSpice computation.

A computer analysis of the design follows; the PSpice netlist is:

```
Transformer Coupled Class A
VS      1   0    SIN(0 1.6 1K 0 0 0)      RL    5    6            8
RS      1   2           1K                RDC   6    0            1MEG
CS      2   3           100U              .LIB EVAL.LIB
VCC     4   0   DC      12                .TRAN    10U  15M 0 10U
Q1      7   3   8       Q2N3904
RE      8   0           10                .OP
RB2     4   3           6.8K              .PROBE
RB1         3   0       1K                .END
LP      4   7           .036
LS      5   6           .001
KPS     LP  LS          .99
```

Note the 1 MEG resistor that is included to satisfy a PSpice requirement for a DC path to ground for all nodes without having a significant numerical effect. Note also the influence of the transformer inductance on the phase shift.

NODE VOLTAGE
(1) 0.0000   (2) 0.0000   (3) 1.9921   (4) 12.0000
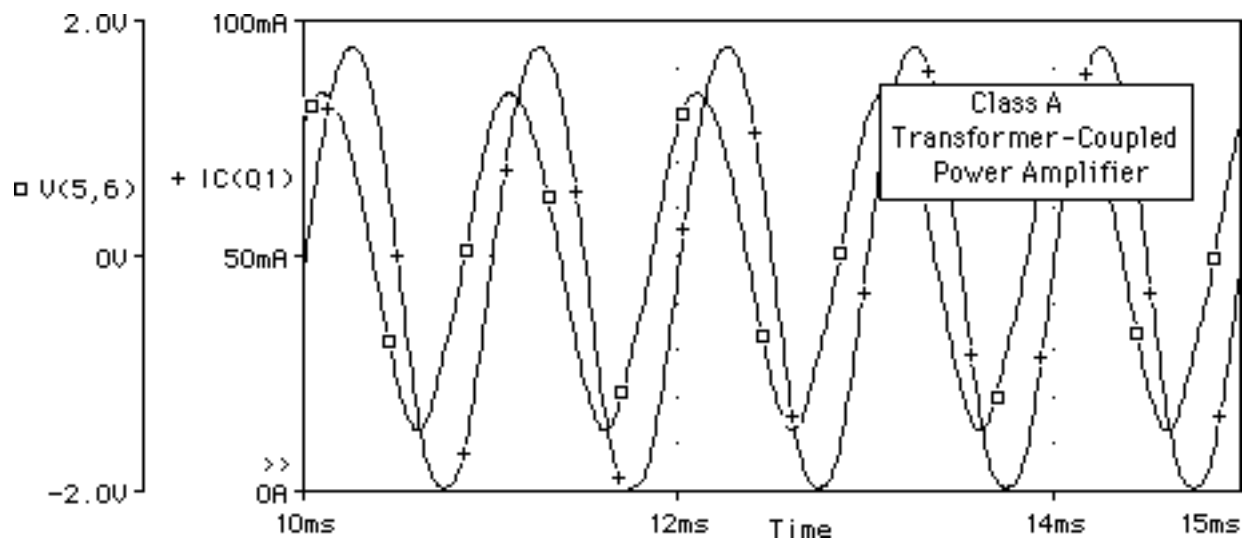(5) 0.0000   (6) 0.0000   (7) 12.0000   (8) 1.1725

| NAME	Q1
MODEL	Q2N3904
IC	1.16E-01
VBE	8.20E-01
VCE	1.08E+01

TOTAL POWER DISSIPATION 1.43 watts

'Push-Pull' Class A Amplifier

The Class A transformer-coupled amplifier is limited in power output capability indirectly because of the quiescent collector current; this current flows through the transformer primary winding and adds a DC magnetic bias to the transformer core magnetic flux. This reduces the core flux change permitted for an AC signal current, in order to avoid magnetic saturation of the transformer core and the consequent nonlinear reduction in core permeability.

The 'push-pull' circuit configuration to the right relieves some of this problem through an application of symmetry. The circuit consists of two otherwise separate Class A amplifiers sharing a common load resistance. Although the output transformer used commonly is constructed as a single unit with a center-tapped primary it operates as two separate primary windings in series, closely coupled magnetically (same magnetic core) to a common secondary. The input transformer also commonly is center-tapped, operating as two transformers with a common primary winding, coupled magnetically to separate secondaries.
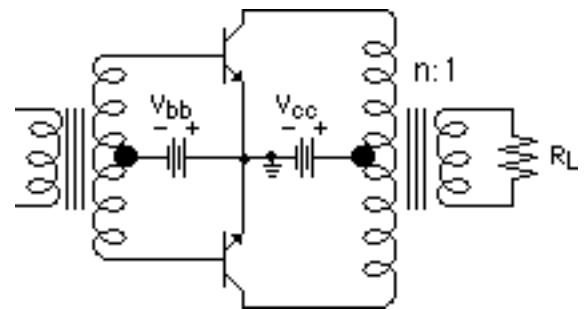
Because of the geometry of the input the two AC signals coupled to the transistor bases are of equal amplitude but are 180° out of phase with each other. The collector currents also are of equal amplitude and 180° out of phase (in the normal range of transistor operation). Hence there is (ideally) no AC collector current flowing through the source connection to the emitter. Insofar as the AC collector current is concerned it flows from one collector to the other!

What is particularly significant about this circuit is that unlike the AC currents the DC collector currents flow from the respective collectors to the center-tap, and then to the emitters. The magnetic effects of the DC collector currents tend to cancel each other since these currents magnetize the transformer core oppositely. However the AC currents couple in phase to the common secondary load.

The design of this circuit is similar to a single Class A amplifier design, except that the resistance seen in each collector circuit is $n^2R_L/2$. The reason for the factor of two is that both AC currents contribute to the magnetic flux linkage and so to the secondary current but only half the primary turns are used by each transistor for the voltage induction.

Since the total secondary power is supplied by two transistors rather than just one as before each one need dissipate (ideally) only half as much as in a single transistor circuit. Note that while this reduces the dissipation requirements for the individual transistors the overall efficiency remains less than 50%.

Transformer-Coupled 'Push-Pull' Class B Amplifier

Push-pull Class A transformer-coupled amplifier efficiency would be improved considerably if the quiescent collector dissipation $I_{CQ}V_{CEQ}$ could somehow be eliminated. This dissipation arises largely because of the biasing needed to enable symmetrical collector current swings. Clearly making either V_{CEQ} or I_{CQ} zero ordinarily does not allow bi-directional transistor operation. However it is possible to operate with $I_{CQ} = 0$ and have a <u>net</u> bipolar operation if two transistors are used, with each amplifying <u>separately</u> alternate polarities of a symmetrical signal.

A circuit to realize this sharing is illustrated to the left; it is similar to the circuit of a Class A push-pull circuit <u>except that there is no emitter junction DC bias.</u> Each transistor therefore is biased at cutoff, i.e., with $I_{CQ} = 0$, and consequently with no DC collector dissipation.   The AC base signals are 180° out of phase as before, so that each transistor is turned on for alternate half-cycles of the input signals.   Although the two collector primary windings both couple to the common secondary they do so on alternate half-cycles.   In this circuit the output effectively uses two transformers operating disjointedly, each with an n/2 turns ratio.   The effective turns ratio then is n/2, so that the load resistance reflected into each collector is $(n^2R_L)/4$.
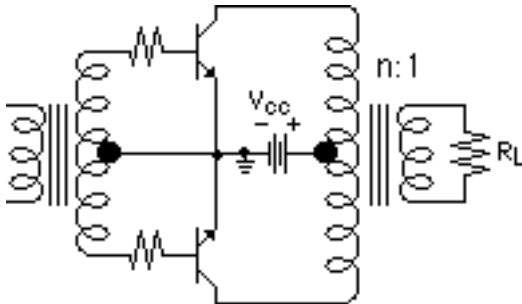
Ignoring saturation and low current effects the peak AC voltage is V_{CC}, and the peak current then is $V_{CC}/(n2R_L/4)$. The average current supplied by each transistor is

$$I_{ave} = \frac{1}{2\pi}\int_0^\pi I_{Cpeak}\sin x \, dx = \frac{1}{\pi}\frac{V_{CC}}{R_L}\left(\frac{2}{n}\right)^2$$

and the combined (total) AC power is

$$P_{AC(total)} = \frac{1}{2}\left[\frac{V_{CC}}{n/2}\right]\left[\frac{V_{CC}}{R_L(n/2)^2}\frac{n}{2}\right] = \frac{1}{2}\frac{V_{CC}^2}{R_L}\left(\frac{2}{n}\right)^2 = \frac{1}{2}\frac{\left[\begin{smallmatrix}\text{secondary}\\\text{peak voltage}\end{smallmatrix}\right]^2}{R_L}$$

secondary peak voltage   primary peak current

The collector dissipation (each device) is

$$\frac{1}{2}\left[2I_{Cave}V_{CC} - \frac{I_{Cave}^2}{2}R_L\left(\frac{n}{2}\right)^2\right]$$

power from DC supply   load dissipation

Differentiate the expression in the brackets to determine that the dissipation is a maximum when

$$I_{ave} = \frac{2}{\pi}\left[\frac{V_{CC}}{R_L(n/2)^2}\right]$$

and the maximum is

$$\left(\frac{V_{CC}}{\pi}\right)^2\frac{1}{R_L(n/2)^2}$$

Note particularly the ratio of the peak collector dissipation to the average power output; the transistors used for a given power output need have an order of magnitude less dissipation capability than before. Note also the improved efficiency

$$\text{Efficiency} = \frac{\text{average AC power output}}{\text{DC power supplied}} = \frac{\frac{1}{2} \frac{V_{CC}^2}{R_L} \left(\frac{2}{\pi}\right)^2}{\frac{2}{\pi} \left[\frac{V_{CC}}{R_L (\pi/2)^2}\right]} = \frac{\pi}{4} = 78.5\%$$

$$\frac{\text{Peak Dissipation (each device)}}{\text{average AC power output}} = \frac{\left(\frac{V_{CC}}{\pi}\right)^2 \left[\frac{1}{R_L (\pi/2)^2}\right]}{\frac{1}{2} \frac{V_{CC}^2}{R_L (\pi/2)^2}} = \frac{2}{\pi^2} = 0.203 \approx \frac{1}{5}$$

Class B Amplifier Illustration

The circuit diagram drawn below supports an illustrative Class B power amplifier illustration. The underlying design philosophy is similar to that used in the last illustration; the circuit may be viewed as two amplifiers operating disjointedly. The operation is similar to that for the Class A amplifier illustration during the active half-cycle. However in Class B operation the load power can be considerably larger than the allowable collector dissipation.

There is one particular 'flaw' inherent in Class B operation, and that involves the biasing of the transistors at cutoff. Since the transistors do not turn on until the emitter junction bias is above the 'knee' of the diode characteristic there is a 'dead zone' around zero crossings of the input signal which is not amplified. This distortion can be significant in some applications and adjustments can be made to mitigate it. The common method for doing this simply is not to use strict Class B biasing, but rather to bias the transistors so that the quiescent point involves small rather than zero DC current. If the transistors are never cut off there is no turn-on problem. This reintroduces some quiescent DC collector dissipation, and is a price for ameliorating the 'cross-over' distortion. Operation in this modified fashion usually is referred to as Class AB operation. However because, as noted before, transformer-coupling is used relatively infrequently in practice, class AB operation will be considered subsequently as part of a discussion of transformerless Class B operation.
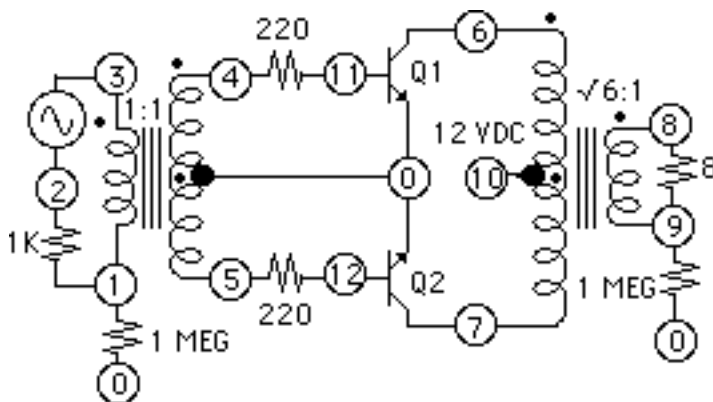
The results of a PSpice analysis follow; examination of the computational details is left as an exercise.

* Class B Xfmr-Coupled Power Amp

VS	3	2	SIN(0 3 1K 0 0 0)		LPC1	6	10	50M
RSL	2	1	1		LPC2	10	7	50M
RS	1	0	1MEG		LSC	8	9	20M
					KSC1	LPC1	LSC	0.99
LPS	3	1	10M		KSC2	LPC2	LSC	0.99
LSS1	4	0	10M		K12	LPC1	LPC2	0.99
LSS2	0	5	10M					
KSS1	LPS	LSS1	0.99		RL	8	9	8
KSS2	LPS	LSS2	0.99		RLDC	9	0	1MEG
KS12	LSS1	LSS2	0.99					
RB1	4	11	220		.LIB EVAL.LIB			
RB2	5	12	220		.TRAN 10U 5M 0 10U			
					.OP			
VCC	10	0	DC	12	.PROBE			
Q1	6	11	0	Q2N3904	.END			
Q2	7	12	0	Q2N3904				
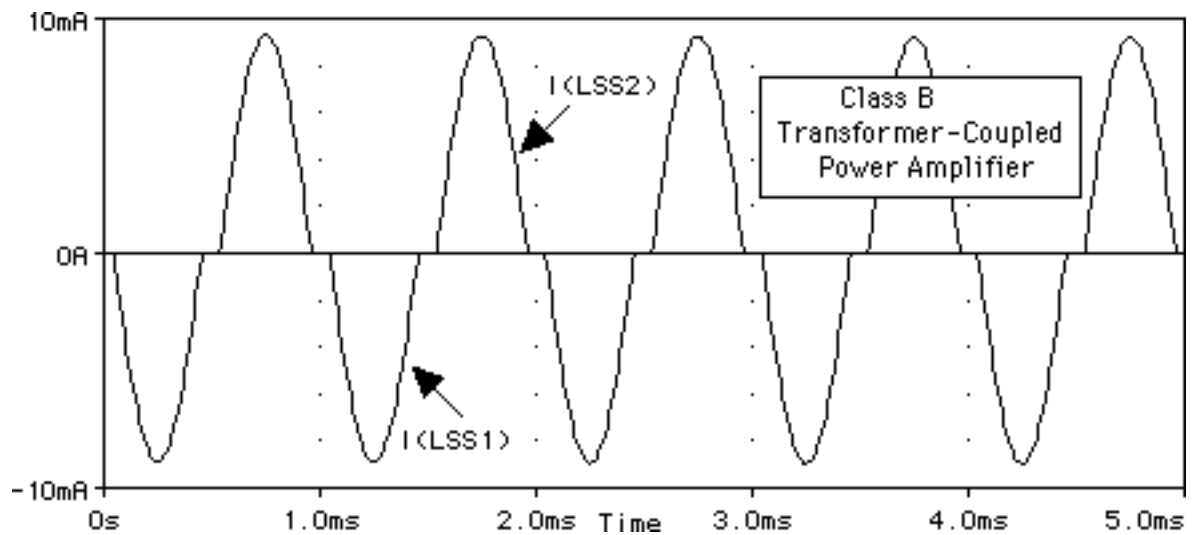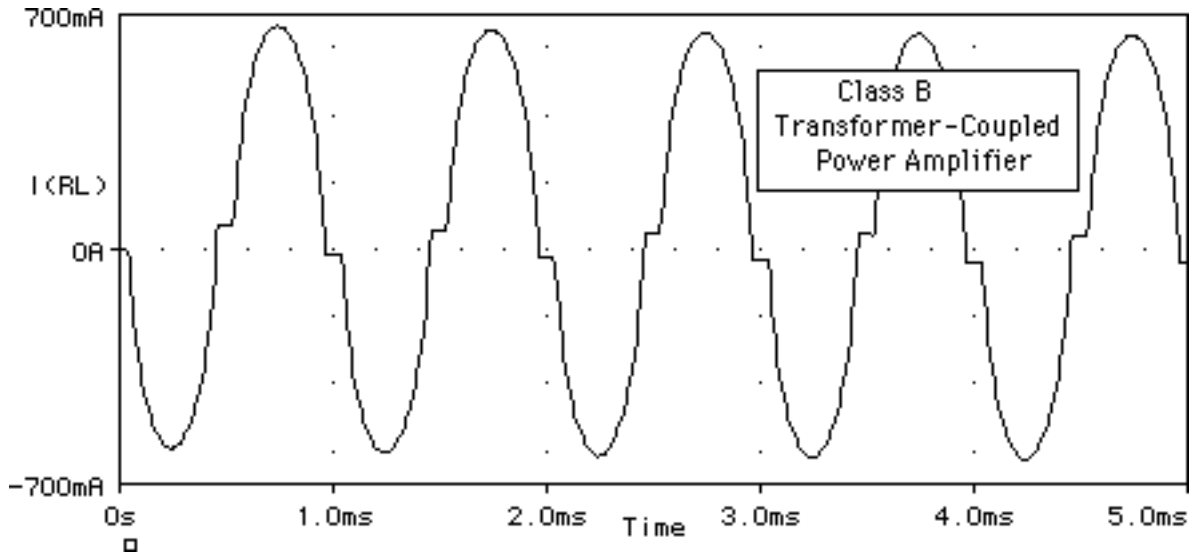
Transformerless 'Push-Pull' Class B Amplifier

Transformers generally are both bulky and heavy, characteristics preferably avoided in general and for small/portable electronic equipment in particular. Methods to combine the contributions of the transistors in a Class B output stage without using a transformer find particular application in integrated circuit devices, where use of a transformer rarely is feasible.
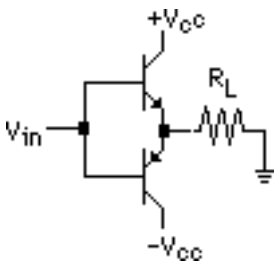
For example the simplified 'complementary symmetry' Class B output amplifier illustrated to the left uses NPN and PNP transistors in such a way that each conducts on alternate half cycles of the input signal. Both transistors operate as emitter followers, with R_L as a shared emitter resistor. During the positive half cycle of the input signal the NPN transistor conducts, providing a current source to 'push' current into the load. For the negative half cycle it is the PNP transistor that conducts, serving as a current sink to 'pull' current from the load. (Class B stage is often referred to colloquially as 'push-pull' operation.)

There is however crossover distortion in the configuration as shown, corresponding to the 'dead zone' around the zero crossing of V_{in}, during which the transistors do not conduct. A circuit modification (below, left) adds resistive biasing to provide Class AB operation. Although the transistors are active biasing is short of enabling significant current flow, i.e., the object still is to avoid excessive quiescent current and the associated collector dissipation.

However for various reasons the use of biasing resistors generally is not desirable in integrated circuit fabrication, and a modified biasing method using diodes (right) often is used. The diodes provide, by virtue of the junction voltage drop, a sort of substitute for bias batteries. The quiescent state of the amplifier is set by adjusting V_{in} (DC level) so that there is no voltage drop across R_L. Assuming matched diodes and emitter junctions for simplicity, a good assumption for integrated circuits, the quiescent current of the transistors then is the same as the diode current I (neglecting the relatively small base currents). Suppose V_{in} is then increased from its quiescent value.
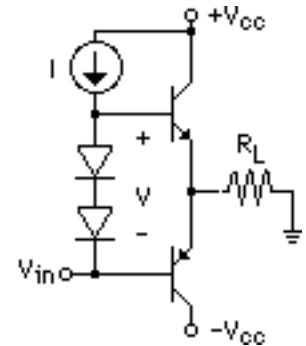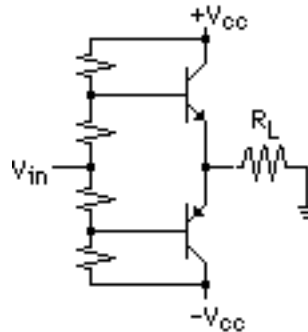
This raises the voltage at the NPN base, and since V (see figure) is substantially constant the base voltage of the PNP transistor also is increased. The effect is to cause the NPN device to carry a larger current, and the PNP device to carry a smaller current; the difference current flows through R_L. Note that the increase of NPN base current to support the larger current comes from I; the diode current is reduced accordingly. This means that I must be at least large enough to provide the base current for the largest NPN emitter current to be drawn.

Conversely, decreasing Vin increases the PNP current while decreasing the NPN current, with the difference current flowing out of RL.
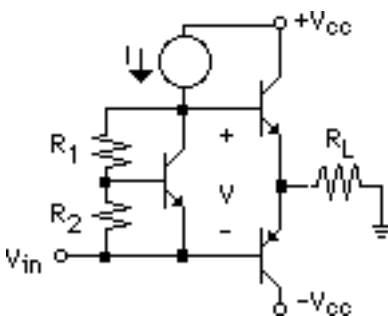
The circuit to the left provides additional flexibility in design, at the expense of reintroducing resistors by replacing the diodes with a transistor and voltage divider. The transistor emitter junction provides a reference voltage of one diode drop across R_2, with the voltage divider action (neglecting the base current) providing a proportional voltage across R_1. Thus the voltage V can be adjusted by the choice of R_1/R_2 resistor ratio.

Class B Voltage Transfer Characteristic

The circuit drawn to the right is used in a PSpice computation to illustrate various aspects of a discrete device complementary symmetry 'push-pull' power amplifier. A 'current source' (about 2 ma) for biasing is provided by the PNP current mirror. The signal voltage source uses a voltage follower as a buffer amplifier to drive the power output stage. The netlist is set up to simplify making three computations; (a) no cross-over correction is used (b) diode correction is used, and (c) a 'VBE multiplier' is used. The icons at the upper right of the figure illustrate substitutions to be made.
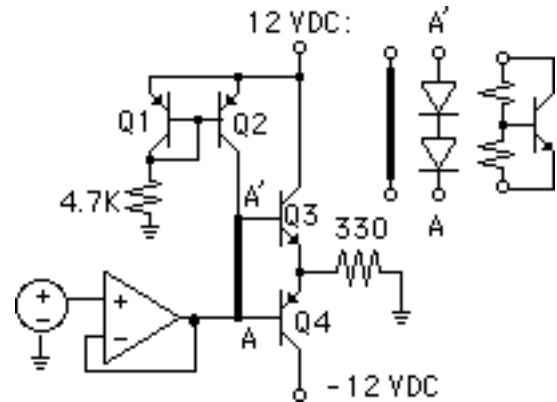
*Class B Push-Pull Power Amplifier

|					
X741	1	2	7 8 2	UA741	;Diode cross-over correction
V+	7	0	DC	12	*D1 5 3 D1N4004
V-	8	0	DC	-12	*D2 3 2 D1N4004
Q1	6	6	7	Q2N3906	
RC1	6	0		4.7K	;BJT cross-over correction
Q2	5	6	7	Q2N3906	*Q5 5 3 2 Q2N3904
Q3	7	5	4	Q2N3904	*RQ1 5 3 10K
Q4	8	2	4	Q2N3906	*RQ2 3 2 4.7K
VS	1	0	DC	1	
RL	4	0		330	.LIB EVAL.LIB
					.DC VS -12 12 .1
; no cross-over correction					.OP
R53	5	3		.1	.PROBE
R32	3	2		.1	.END

The following figure compares the voltage driving the output stage with the load voltage in the absence of cross-over correction. One difference is associated with the emitter junction voltage drop, 0.7 volt. The other is the cross-over 'step' in the output voltage waveform.
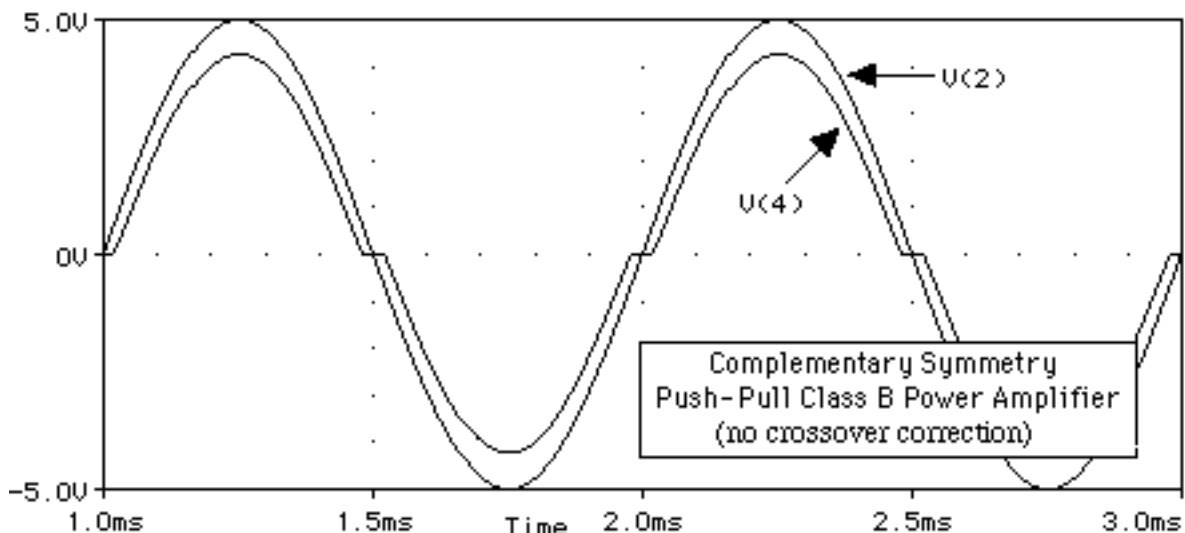

A related comparison is shown in the next figure; the emitter currents of the two output transistors are compared to the load current. Note the expected disjointness of the currents, and their summing (per KCL!) to provide the load current. Incidentally a 180° phase shift is introduced for clarity in making the comparison.
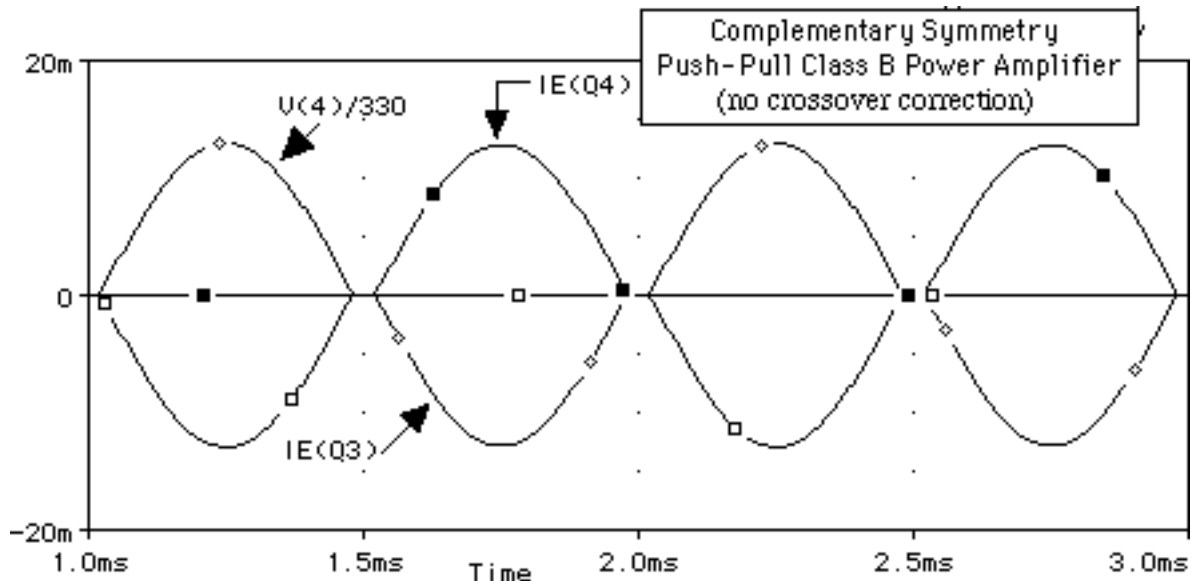
Finally, the following figure compares the voltage transfer characteristics with and without cross-over correction. Note that the <u>vertical</u> displacement of the 'no correction' segments is about two diode drops. Note also the small offset associated with the transistor correction.
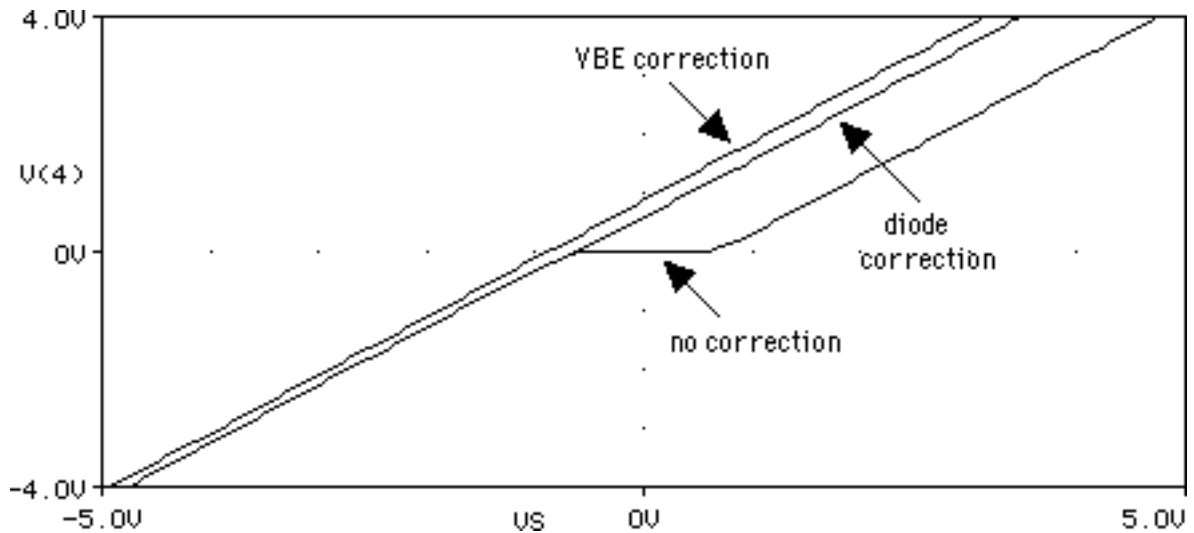
'Feedback' Crossover Correction

There is one other crossover correction method that should be noted, and that involves the use of feedback. In effect the output transistors are used to provide the higher load currents needed, and the amplifier is used to force the load voltage to track the input voltage. To accomplish this the output stage is included in the feedback loop of a voltage follower connection, as indicated by the heavy line in the accompanying figure.
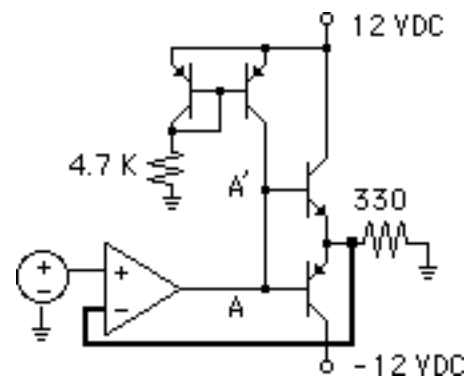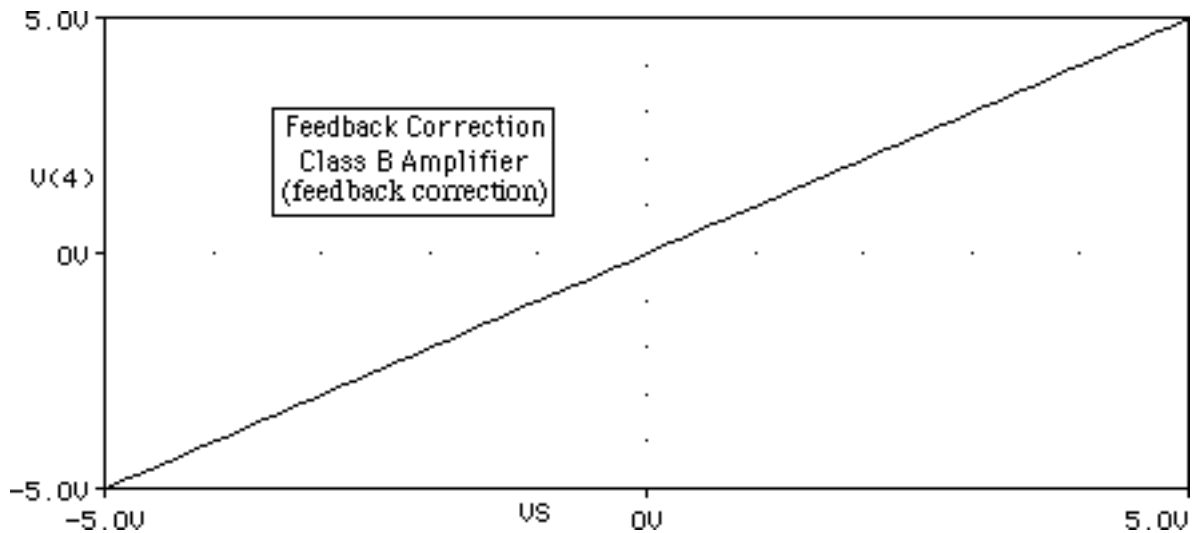
Quasi-Complementary Amplifier

The Class B/AB complementary push-pull power amplifier configurations assumed implicitly that the characteristics of the NPN and PNP devices are matched so that, for example, both half cycles of a sinusoidal input signal were amplified in substantially the same way. High power closely matched discrete complementary devices are in fact available commercially. However for integrated circuits, where both PNP and NPN devices are fabricated in the same substrate, NPN devices generally are preferred, both for device performance characteristics and fabrication simplifications.

One (of several) alternative configurations used for higher powers is the 'quasi-complementary' output stage illustrated to the right. The PNP transistor does not provide a sink for load current directly as before but rather is used to provide a low-power base drive for an NPN device, thus providing a composite PNP-NPN device with the input characteristics of a PNP transistor and the amplification capabilities of an NPN device.
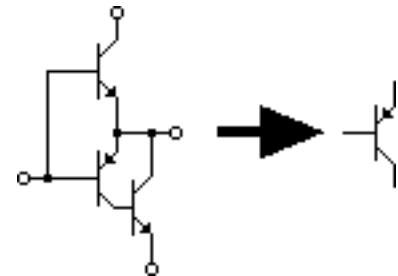
Overload (Short-Circuit) Protection

As noted earlier the output load of a power amplifier often is not entirely under the control of the designer, and accidents happen. If mischance causes the amplifier output to be short-circuited a large current demand may be placed on the output stage; for a power amplifier this can be destructive. Adding short-circuit protection therefore is a prudent necessity.

In general two mechanisms are needed for a protection mechanism; a means for detecting the event guarded against, and a means to prevent damage from the event.

Short-circuit protection shown for positive signals (only) commonly is added to the circuit as illustrated to the right. Detection of excessive current is accomplished by the small resistors R added in the emitter paths; when the voltage drop across these resistors is sufficiently large (approximately 0.5 volt) an overload transistor (only one for NPN current is shown) is turned on. The protection then is implemented by bypassing the NPN base current to the output; the protection transistor essentially acts as a current sink to drain off base current. The effect is equivalent to a rapid reduction in the value of the BJT current amplification factor, so limiting the short-circuit current to a designed safe value.
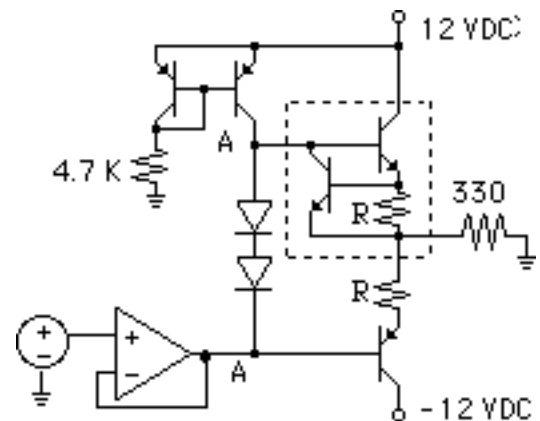
PROBLEMS

1) Design a Class A emitter follower for maximum power to an 8 load, as shown in the figure. Use 2N3904 transistors (maximum collector dissipation is 0.5 watts, maximum collector current is 200ma).
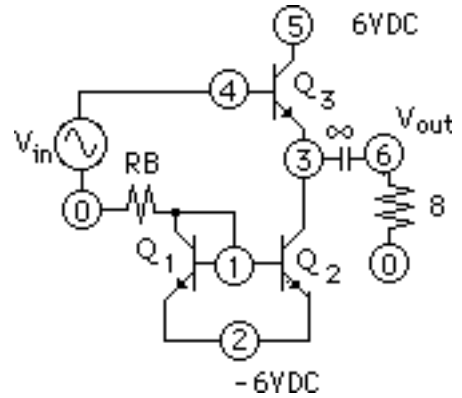
2) Estimate the performance of the Class B amplifier circuit drawn to the right. Compare your estimates against the results of a PSpice computation. Transistors are 2N3904 (NPN) and 2N3906 (PNP) respectively. Suggestion: Use a nominal signal frequency of 1 kHz and amplitude 4 volts.
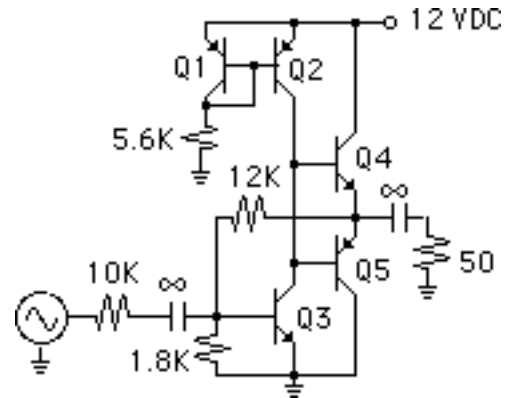
3) Estimate the performance of the Class B amplifier circuit drawn to the right. Compare your estimates against the results of a PSpice computation. Transistors are 2N3904 (NPN) and 2N3906 (PNP) respectively. Suggestion: Use a nominal signal frequency of 1 kHz and amplitude 4 volts.
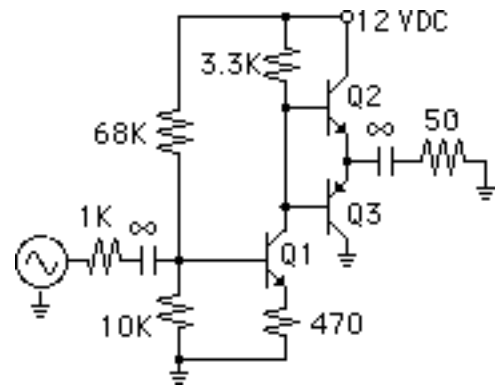
4) Estimate the performance of the Class B amplifier circuit drawn to the right. Compare your estimates against the results of a PSpice computation. Transistors are 2N3904 (NPN) and 2N3906 (PNP) respectively. Approximate the circuit as an inverting amplifier with an 8.2 K shunt-shunt feedback to estimate the voltage gain to be about 8. Suggestion: Use a nominal signal frequency of 1 kHz and amplitude 1volts. How reliable is this circuit, e.g., as a function of temperature.