Chapter 2.   Display Systems

2.1 Introduction

Early computers communicated with the user with either indicator lamps or hard copy printers, but today, the primary output device is the electronic display. This is usually the CRT display, although other technologies are available. The enabling display technology for portable computers and the latest personal digital assistants (PDA) is the liquid crystal display.

2.2 Types of displays

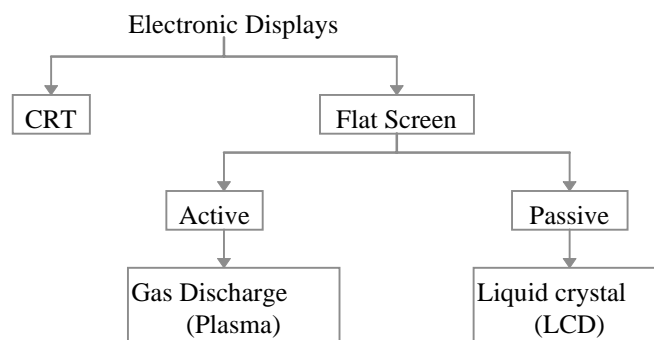Displays can be classified into following 3 main types in term of technology.

Figure 2.2-1 Display technologies.

The CRT display uses the same technology as the television. A vacuum glass tube has at the end of its neck a heated filament. The electrons emitted are attracted towards the face of the screen by the electric field created by the high tension (HT) voltage applied between the cathode and the anode. The beams of electrons pass through the focusing and deflection electrostatic plates or coils along the way. The screen is coated with a thin phosphor layer which emits light when impacted by an electron at that point.

LCDs composed of two plates of glass in close proximity. Each plate has conductive lines evenly spaced, but very close together, on its surface. The two sets of conductive lines on the glass plates are perpendicular to each other so that they form a grid when viewed from the top. On the outside of each glass plate is a polarising filter. The liquid crystal material is in the centre, between the two sets of conductive lines.

There is a mirror on the bottom side of the display. When room light or sunlight hits the display, the light is polarised as it passes through the top polariser. In the parts of the grid with no power applied, the crystals automatically line up in a stair-step type of formation on their side. This alignment causes the now-polarised light to rotate 90 degrees and allows it to pass through the lower, or bottom, polarising layer. There, it hits the mirror and is reflected back along the same path, rotating back through the crystals as it does. This causes the grey or silver colour on the screen. In the parts of the grid where a character is to appear, a current is applied to the appropriate conductive lines on both the top and bottom plates. This causes the crossing point of these two lines to be energised or excited. When this happens, the crystals are pulled perpendicular to the glass plates. The staircase no longer exists at this location, and the light is kept from twisting 90 degrees. Thus, it cannot pass through the lower polarising filter and be reflected back. This screen position, therefore, appears to be black.

Plasma screens are one of the easiest types of displays on which to see characters and graphics. In addition, they are also very reliable. With plasma screens, there are two glass panels on the top and the bottom, like LCDs. The panels are separated slightly and have conductors plated onto the glass in evenly spaced rows. The conductor rows on the bottom plate are rotated 90 degrees from the top plate. The two plates are sealed airtight, and the space between them is filled with a mixture of argon and neon gases. To form a point on the display, one of the upper conductors is energised as well as one of the lower conductors. The point where they cross over each other has approximately 200 volts DC difference. This causes the gas at this point to break down or "ionises" causing it to glow.

2.3 CRT Displays

It is the oldest and most popular display technology

Advantages:

♦   Low cost because of volume of production.

♦   Speed of updating and the retention of image is good.

♦   Colour display is available.

♦   Text and graphics display modes.

Disadvantages:

♦   Large size and weight: Typical CRT displays are at least as deep as they are wide

♦   High voltage and power consumption. Also generate a lot of heat.

♦   CRT displays are glass vacuum tubes, and are therefore relatively fragile.

♦   The microprocessor interface is relatively complex.

2.3.1 CRT FUNDAMENTALS

The CRT display uses the same technology as the television. Figure 2.3-1 shows the basic components of the CRT. The vacuum glass tube has at the end of its neck a heated filament. The electrons emitted are attracted towards the face of the screen by the electric field created by the high tension (HT) voltage applied between the cathode and the anode. For a 12-inch monitor, this voltage is about 1200V. The beam of electrons passes through the focusing and deflection electrostatic plates or coils along the way. The screen is coated with a thin phosphor layer which emits light when impacted by an electron at that point.

The voltage applied to the control grid regulates the intensity of the electron beam. Since the brightness of the screen is dependent on the number of electrons hitting the phosphor, the display brightness is a function of the control voltage applied to the grid. For monochrome displays, the colour of the display is dependent on the type of phosphor used.

The focusing anode, sometimes called an electrostatic lens, forms the emitted electrons into a thin circular beam (along the Z direction), so that the image created on the screen is a sharp well-defined spot. Magnetic focusing coils are common and can produce a narrower beam of electrons, that is, a sharper focus.

The electron beam is aimed at a particular point on the screen by passing it through an electromagnetic field generated by the set of deflection coils in the yoke assembly. Two vertical deflection coils generate a field perpendicular in X direction of the electrons, allowing the electron beam to be scanned vertically. And two horizontal deflection coils do the same in the horizontal direction, thus enabling the beam to be positioned anywhere on the face of the tube. The CRT used in oscilloscopes which require faster, more precise and linear positioning of the beam uses electrostatic deflection plates in the tube rather than deflection coils.
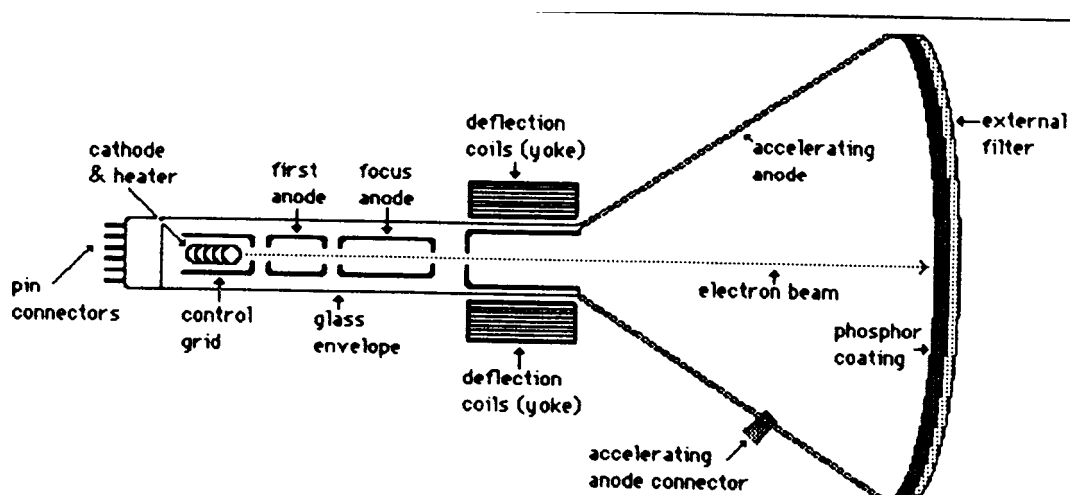

Figure 2.3-1 Basic CRT physical construction

2.3.1.1 Colour display.

To achieve colour, different chemical compounds (excess of 150 types) are used in phosphor manufacturing. Three cathode ray tubes are used. Each gun is directed and masked so that it can only illuminate a single colour phosphor. With the right mixture of the 3 primary colour (RGB) the full colour spectrum can be achieved. Figure 2.3-2 shows a colour mixing chart.
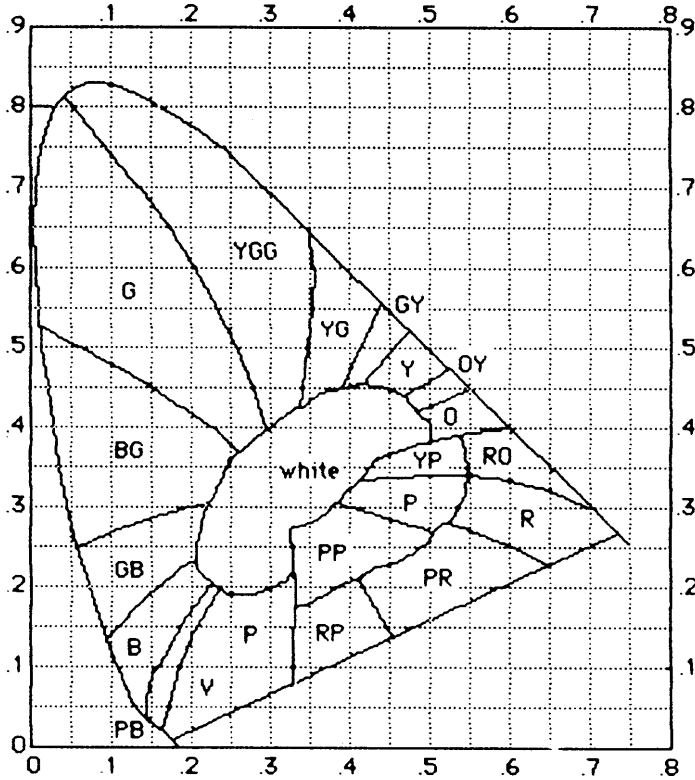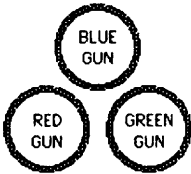
Figure 2.3-2 colour mixing chart

Delta gun configuration

In-line gun configuration
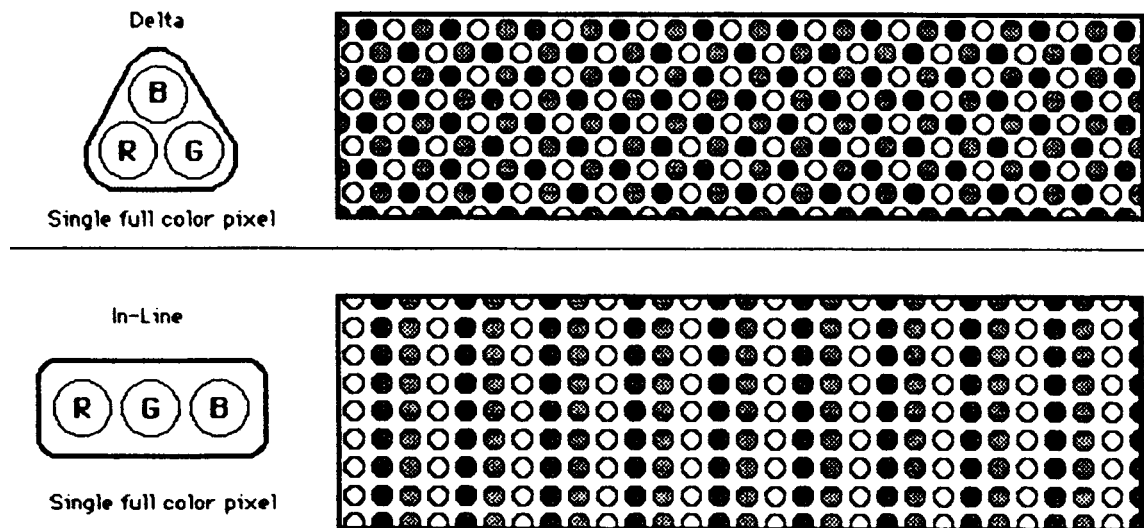
Figure 2.3-3 Configuration of colour CRT gun

Delta

B

R G

Single full color pixel

Figure 2.3-4 Colour CRT phosphor configuration

In-Line

R G B

Single full color pixel

Figure 2.3-4 Colour CRT phosphor configuration

Delta mask pattern

Phosphor pattern

Mask + Phosphor pattern

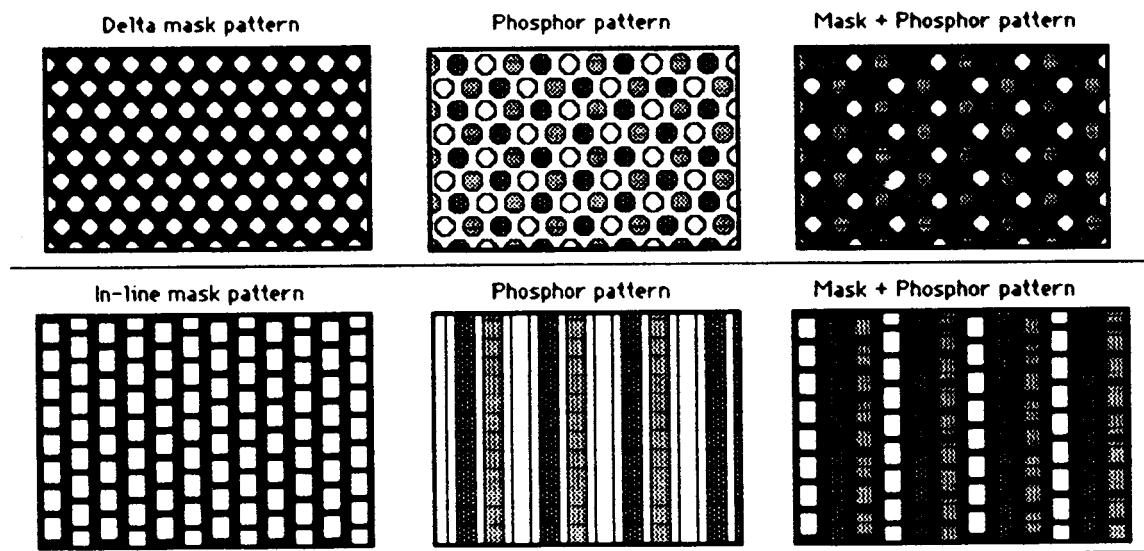In-line mask pattern

Phosphor pattern

Mask + Phosphor pattern

Figure 2.3-5 Colour CRT mask configuration

2.3.2 CRT INTERFACE SIGNALS

The circuit that interfaces the microprocessor buses to the CRT monitor is called the *CRT controller*. The three basic signals that must be provided to the CRT monitor are the video information, horizontal sync, and vertical sync. Each time horizontal sync is asserted, the electron beam retraces to the left edge of the screen. Each time vertical sync is asserted, the beam retraces to the top of the screen. These signals are usually provided by the CRT controller to synchronise the sweep oscillators in the monitor to the video information. For special applications, such as overlaying of computer generated video on television images, the CRT controller may accept the sync signals as inputs and synchronise the computer-generated video to them.

Some CRT monitors use signals called *horizontal drive* and *vertical drive* instead of the sync signals described above. These signals have the same period as sync signals but different pulse widths and polarity.
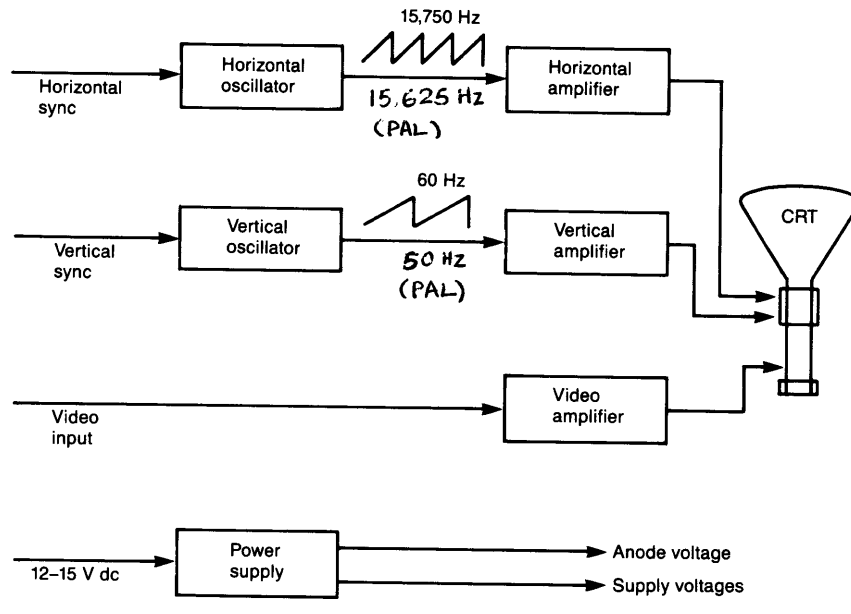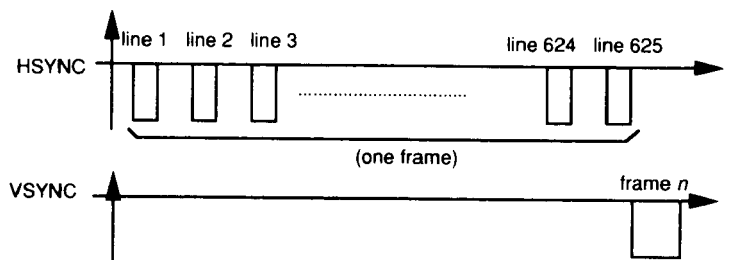
Figure 2.3-6 Major interface signals

Figure 2.3-7 Horizontal and vertical Sync pulses

- Horizontal sync: Retraces beam to the left edge of the screen.

- Horizontal oscillator: Saw-tooth signal that sweeps the beam horizontally across the screen.

- Vertical sync: Causes beam to retrace to the top of the screen.

- Vertical oscillator:Saw-tooth signal applied to the vertical deflection amplifier to move the beam down the screen.

- Video signal: Determines the intensity of the beam that will strike the screen. The signal is amplified and applied as the accelerating voltage in the CRT.

There are two basic methods of displaying an image on the screen:

2.3.2.1 VECTOR GRAPHIC

The vector or stroke method, like the oscilloscope, controls the positioning of the spot on the screen with electric fields (usually, although sometimes magnetic

fields are used,) in the X- and Y- direction to trace out the image. This is suitable for very fine line images. As the persistence is limited and to avoid flicker, the entire image must be retraced more than 30 times per second, which places a limit on the complexity of the image that can be displayed. Sometimes storage display tubes are used.

2.3.2.2 RASTER SCAN

Like the Television, the electron beam traces a standard pattern of horizontal lines. As each line is traced, the brightness of the spot is changed by varying the Z-axis (video) voltage, thus building up the image line-by-line.

Starting from top left, a horizontal line is traced by sweeping the X-voltage. On reaching the right edge, the beam is blanked and quickly returned to the left (horizontal retrace) to trace the next line. The Y-voltage is increased slightly so that the beams begins from a new starting point below the previous line.

After the bottom line is traced, the vertical retrace takes place, blanking the beam and quickly moving it back to the top of the screen even as the horizontal retrace takes place.
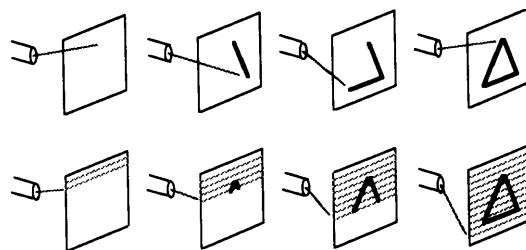

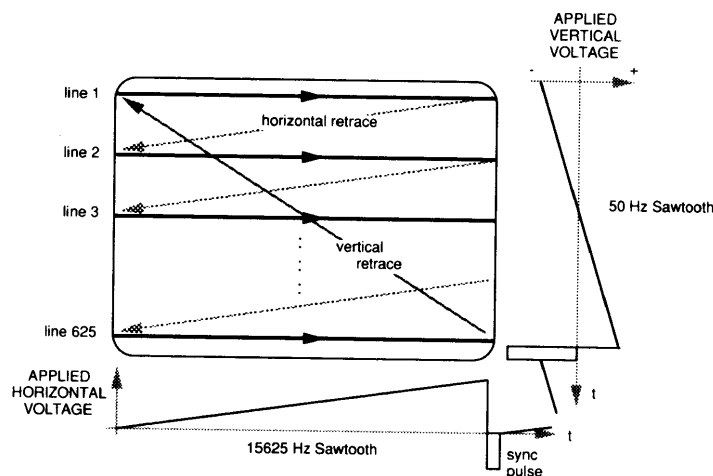Figure 2.3-8 Vector scan vs. raster scan

Figure 2.3-9 Raster scan CRT display

2.3.2.3 Interlaced and Non-interlaced

Instead of tracing all the video signals from top to bottom to form one frame. CRT displays often use interlacing, where the odd number and even number of lines being traced out at alternate frame. See Figure 2.3-10. Interlacing is used because it doubles the effective resolution without increasing the scan rate. However, the refresh rate for each field is reduced to 25 (30) Hz, which is slow enough to cause flicker. This is not noticeable on television displays because both fields (that is, adjacent lines) are usually quite similar. On computer displays, however, the full resolution is often used, and one scan line may be completely different from the adjacent ones, resulting in flicker. Thus, non-interlaced displays are preferred for computer display applications.

The sweep oscillators in the CRT monitor are synchronised to the sync signals from the CRT controller. The sync signals must be within a range that the monitor can accept; the width of this range varies depending on the type of monitor. Most monitors can operate in an interlaced or non-interlaced mode; this is determined by the sync signals. In an interlaced system, every other vertical sync pulse occurs in the middle of a horizontal scan.
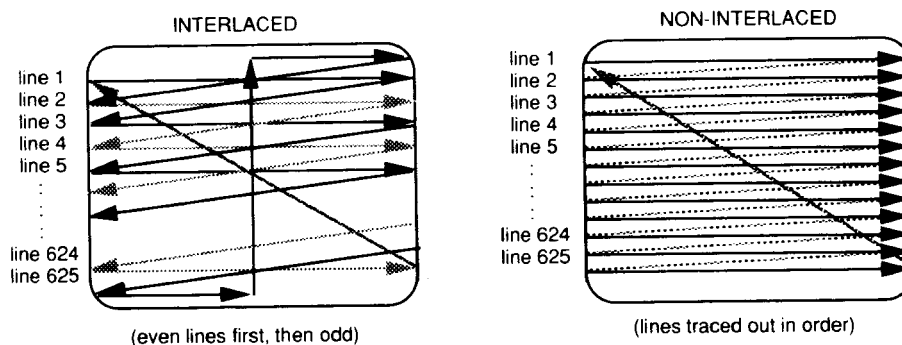

Figure 2.3-10 Raster scan CRT display

For standard broadcast format television in North America, the NTSC standard is used where the horizontal sweep rate is 15,750 Hz, and the vertical sweep rate is 60 Hz. The vertical rate is chosen to match the power line frequency, to avoid any "beating" effects with it. Stray electromagnetic fields which would have a power line frequency would result in waviness in the display by deflection of the beam. The horizontal frequency determines the number of lines per field. A horizontal rate of 15,750 Hz results in 262.5 lines per field. For standard television monitors, the horizontal scan rate must be close to this standard. However, many commercial applications use higher scan rates, such as 18.4 kHz. This provides more lines per field and thus higher resolution. In addition, it raises the scan frequency out of the hearing range of most people, 15,750 Hz is audible to many people, and CRT monitors at this frequency produce an annoying whine. This is not so objectionable with televisions, since the viewer is usually across the room and the television voice channel is generating lots of intentional noise that tends to block out the whine from the scanning. The European Phase Alternating Line standard uses a 625-line raster scan display with a refresh rate of 50 Hz, resulting in a horizontal rate of 15625 Hz.

The fact that the 15625-Hz (15750-Hz) scan rate produces an extra half a line (312.5 or 262.5) is not accidental. It results in *interlacing,* as shown in Figure 3.2.3.1. Each alternate field is offset by one-half the line spacing. This effectively produces a display with twice as many lines, only half of which are scanned each time. Two

fields are required to produce a complete image, which is called a *frame*. This is the technique used by standard broadcast television.

2.3.2.4 Composite Video

Many monitors accept separate video, horizontal, and vertical signals as described previously. For broadcast television and some CRT monitors, these signals are all combined into one *composite* signal. As a first step, the horizontal and vertical sync signals are combined. The horizontal sync pulses are typically 3 to 5 ms wide, while the vertical sync pulses are much longer, typically over 150 ms. Because of the difference in frequency, they are easily separated by low-pass and high-pass filters.

The combined sync signals are then combined with the video information by using different voltage levels. Figure 2.3-11 shows the waveform of a composite video signal for one line. The black, or off, video level is represented by a level of approximately 0 V. The white, or on, video level is represented by the maximum voltage, typically 1 to 2 V. Intermediate voltages can be used for varying intensity levels. The sync signals appear as pulses below the 0 V black level. Figure 2.3-11 shows the composite signal for an entire frame. The vertical sync pulses are distinguished by their length. The number of horizontal sync pulses between each pair of vertical sync pulses determines the number of lines in the field. Typically 20 to 30 percent of each scan line is blanked and thus not available for video information. Similarly, a percentage of the vertical scan time is used for blanking and retrace, so some of the scan lines (approximately 20) are not displayed.

For many computer display applications, there is no reason to use composite video. It makes little sense to add circuitry to the CRT controller to combine several signals, which requires additional circuitry in the CRT monitor to separate them again. CRT monitors that accept composite video are generally more expensive than those requiring separate video and sync signals, since the "sync separator" is an additional cost. There are several standards that apply to CRT monitors, although they are not universally followed. RS-170 specifies the basic interface signals as described previously for television-format displays. For higher-resolution displays, RS-343 defines the interface signals and certain display characteristics.
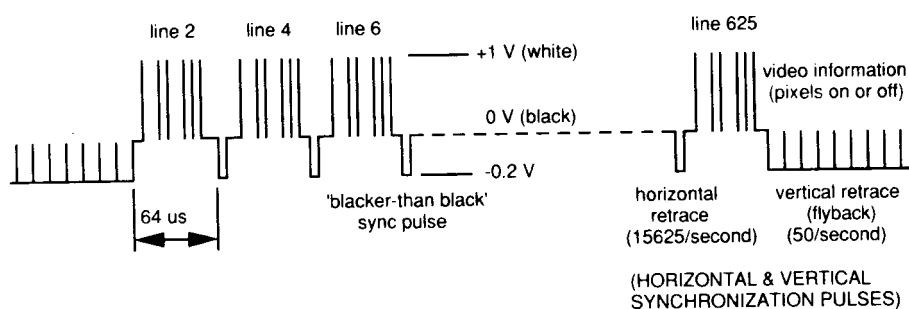

Figure 2.3-11 Composite video signal

2.3.2.5 SIZE AND RESOLUTION

The resolution of a CRT display is a combination of two factors: the number of scan lines and the number of dots that can be displayed on each line. As previously described, the number of scan lines is determined by the horizontal scan rate

(assuming a fixed vertical scan rate). This determines the resolution in the vertical direction. The resolution in the horizontal direction is determined by the rate at which the electron beam can be turned on and off; this is called the *video bandwidth.*

Typical resolutions:

- CGA: 320 X 200

- EGA: 640 x 350

- VGA: 640 x 480

- SVGA: 800 x 600, 1024 x 768, 1280 x 1024 etc.

Screen aspect ratio: 4:3 or 16:9 (Cinemascope)

Dot aspect ratio: The square dot

2.3.2.6 TIMING CONSIDERATIONS

For non-interlaced display with resolution of 640 x 480 dots, refreshed at 70 Hz.

For an actual viewable display of 480 lines we need to allow time for the vertical retrace (flyback). Typically we allow an additional 25-30 lines for this.

Similarly after displaying 640 dots on the line, we allow an additional 25% of the line time for the horizontal retrace (commonly worded as 20% of the line time is used for horizontal retrace). (Total: 800 dots)

Thus every 14.28 ms the screen is refreshed by writing the frame of 510 lines (480 + 30).

Line time is 28 s, i.e. this is the time available for one line to be traced, including the horizontal flyback.

Time for each active line (of 640 dots) is 0.8 of this, 22.4 s.

The dot time is thus 35 ns, giving a dot rate of ~30 MHz.

```
Frequency oscillator:   28.57 MHz ----------------> Dot frequency
                        |     % 800 lines
                        35.71 KHz ----------------> Horizontal Sync
                        |     % 510
                        70.02 Hz -----------------> Vertical Sync
```

2.3.2.7 FREQUENCY RESPONSE OF MONITORS

Worst case display is when dots are alternating on and off, giving a worst case signal of 15 MHz square wave for a 30Mhz display.
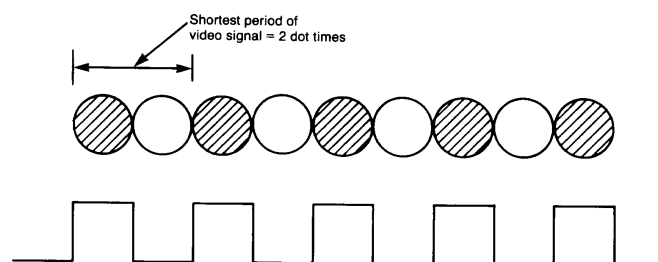
Figure 2.3-12 Frequency response of monitor

However, monitor bandwidth is specified as *sine wave* bandwidth. If a 15 MHz square wave is fed to a monitor with a 15 MHz bandwidth, only the fundamental sine wave will be displayed, resulting in dots with fuzzy edges. To obtain sharper edges on each dot, the monitor must pass the third harmonic of the fundamental frequency. (The Fourier transform of a square wave is an infinite series of odd harmonics.) Thus, the required bandwidth for a high-quality display is 3 x 15 MHz, or 45 MHz. Many applications get by with monitor bandwidths equal to the dot rate (twice the maximum square wave frequency). High resolutions monitor typically has frequency responses in the 100 MHz range.

2.4 TEXT-ORIENTED DISPLAYS

The most flexible CRT displays allow the microprocessor to individually control each dot on the screen. This is called a *bit-mapped* display, since one bit (or several bits) of memory controls each dot on the screen. This is the common approach for graphics displays. Bit-mapped Displays is almost a standard in the latest OS. However, many applications still require Text Display only, Terminals like DEC VT100/220 and the normal mode for the PC monitor.

2.4.1 CHARACTER GENERATION

Dot Matrix representation of Characters on CRT.

Low cost, low resolution 5 x 7 Matrix

Improved 7 x 9 Matrix with 2 dot Descenders

7 x 11 FONT SIZE.

Also requires (say) 2-dot Inter-character Spacing and 3-line Inter-line Spacing

9 X 14 CHARACTER CELL

Figure 2.4-1 shows an 80-character row of data being generated using 5 X 7 matrix and the 35-bit memory for the character R.
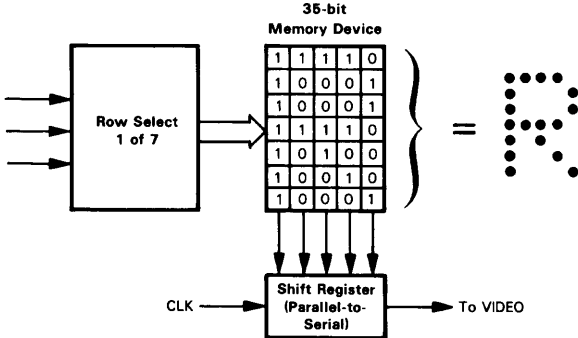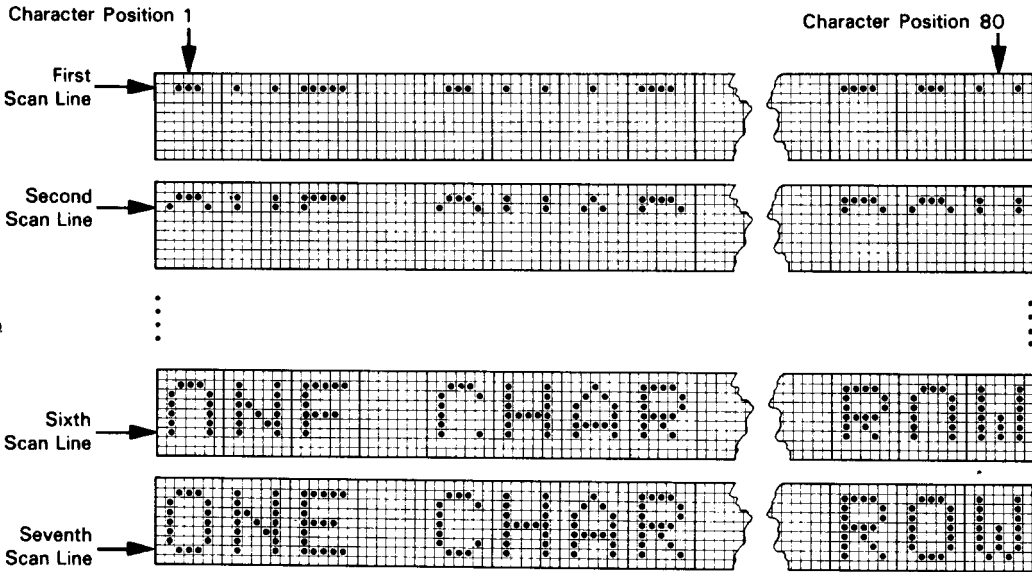
Figure 2.4-1 show a 80-character row of data being generated using 5 X 7 matrix
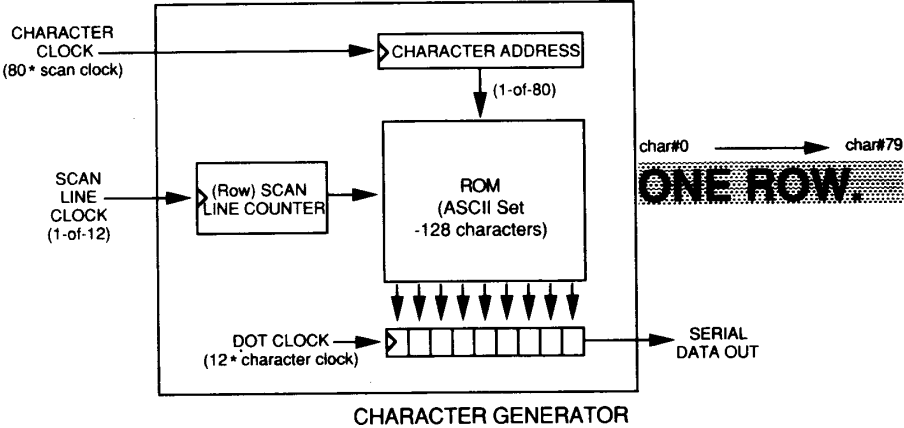

CHARACTER GENERATOR

Figure 2.4-2 Storage of one row of characters

Take the above example with the dot time as 35 ns, giving a Dot Clock of 28.57 MHz. If each character takes up 8 by 10 cell, then the 640 X 480 display is capable of displaying 48 rows of 80 characters. The following are the frequencies:

```
Frequency oscillator:    28.57 MHz ----------------> Dot CLK
                         | % 8 dot per character
                         3.57 MHz  ----------------> Character CLK
                         | % 100 (80 + 20) characters
                         35.71 KHz ----------------> HSYNC
                         | % 10 Lines/Character
                         3.57 KHz -----------------> Data row CLK
                         | % 51 Rows/screen (48+3 retrace)
                         70.02 Hz -----------------> VSYNC
```

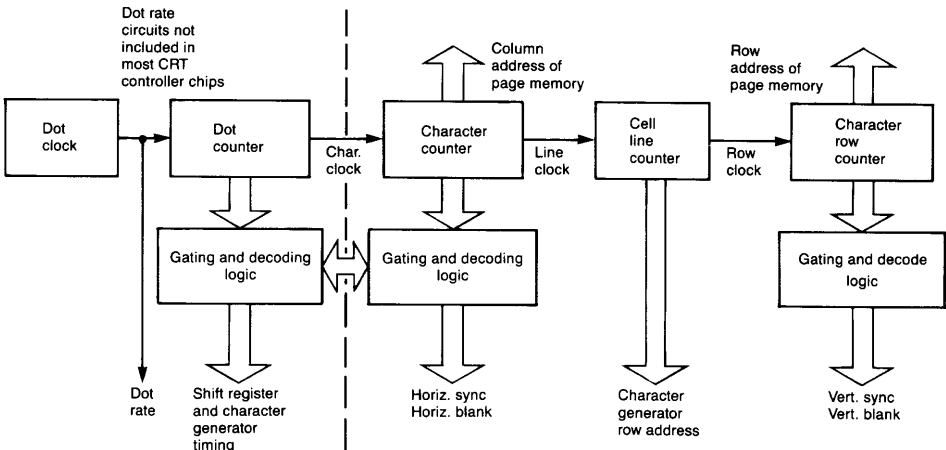

Figure 2.4-3 CRT controller counter chain and associated logic

2.4.2 DISPLAY SIZE

Use 7 x 11 Font Matrix in 9 x 14 Cell

Display with 25 lines x 80 characters

Number of dots per line   80 x 9 = 720

Total lines per frame   25 x 14 = 350

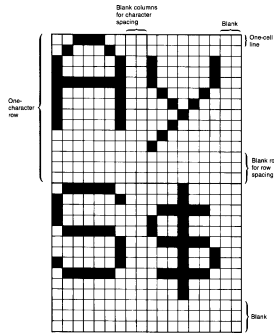Monitor resolution required   720 x 350

This is EGA resolution.

Figure 2.4-4 A 7 X 11 character matrix in a 9 X 14 cell

2.4.3 Screen Memory

Figure 2.5.1 shows a general block diagram of a CRT controller. The CRT display RAM (also called the screen memory) contains one location for each possible character position. The microprocessor writes the characters to be displayed to this memory, and the CRT controller reads them at the appropriate times. Because the microprocessor and the CRT controller both require access to the same memory, memory contention logic is required to determine which of them can access the memory at what time.
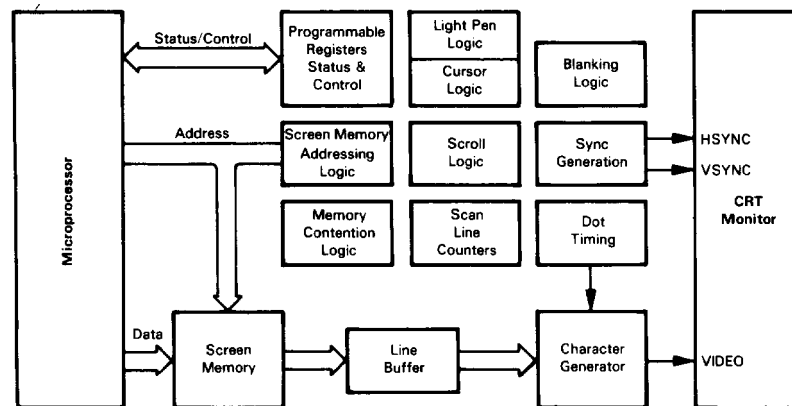

Figure 2.4-5 CRT controller

The CRT controller requires access during the active video time, and if it is denied this access, the image on the screen cannot be maintained. The microprocessor is less demanding of immediate access to the screen memory, but if it has to wait for access often, the system performance can suffer. Three common approaches are frequently adopted to handle memory contention problem

2.4.4 Memory Contention Logics

2.4.4.1 Direct Memory Access

One approach is to use the microprocessor's main memory for the screen memory. A DMA controller transfers data to the CRT controller. The CRT controller typically includes two *row buffers* that store the screen data for two rows of characters. While one row buffer is being displayed, the other is filled by the DMA controller by reading from the screen memory area in the microprocessor's main memory.

2.4.4.2 Interlaced Memory Access

The second technique is to use a 2-phase clock. This allows access by both the microprocessor and the CRT controller 'at any time'. Interlaced Memory Access is often easier to implement with microprocessors such as the 68000 and 6502, since they have symmetrical two-phase clocks that define when the microprocessor needs access to the memory. Since the microprocessor requires access to the memory only during one phase of the clock, the CRT controller can be given access on the opposite phase.

2.4.4.3 Non-Display Time Access

The simplest technique is for the microprocessor to access the screen memory only when the display is normally blanked. The major blanking periods are the horizontal and vertical blanking times, although it is also possible to make use of the blank dots between characters and the blank lines between character rows. This can be implemented with any CRT controller by connecting the blanking signal to an input port bit or an interrupt input. The microprocessor then polls this input bit (or waits for an interrupt) to determine when it can access the screen memory.

Typically horizontal retrace represent approximately 25% of the total horizontal scan time and with the vertical retrace being around 30 lines, this will give about 25% of the time for CPU to access the screen memory. Figure 2.2-1 shows the amount of time available in the total blanking time of a 512 X 512 60 Hz display.
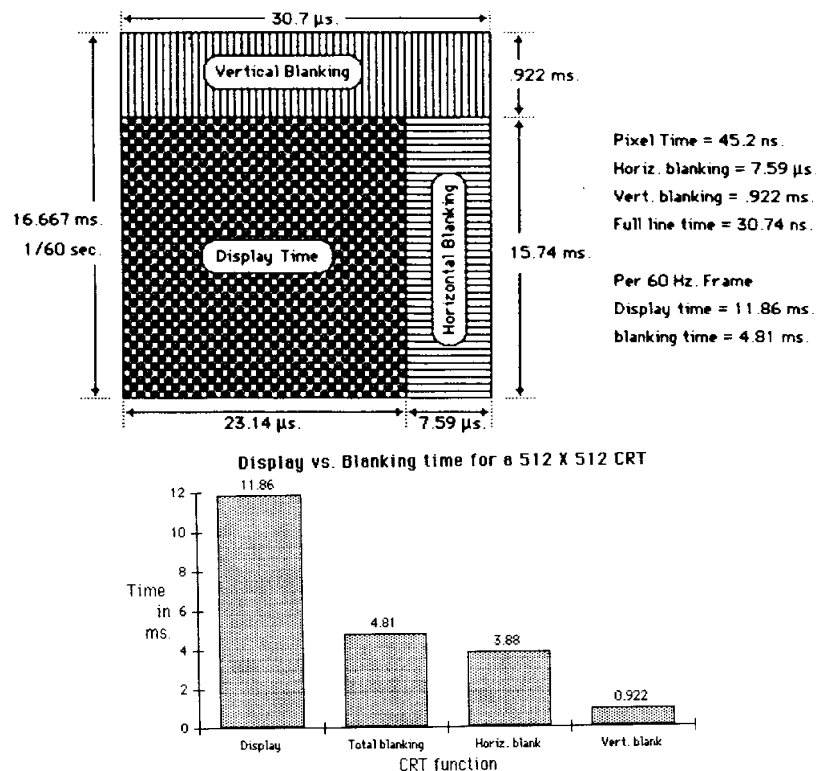

Figure 2.4-6 Display time vs Blanking time.

The disadvantage of the Non-Display Time Access approach is that the microprocessor can spend a significant amount of time waiting for access to the screen memory.

2.4.5 CHARACTER-ORIENTED CONTROLLERS

2.4.5.1 Intel i8275 for Direct Memory Access

i8275 is designed to work with i8257 DMAC in order to handle the block transfer of characters between screen memory and the CPU. The i8275 provide programmable screen and character formats, visual field and character attributes, cursor control, light pen support, dual row buffers and ability to operate in DMA burst mode. Figure 2.4-8 shows a block diagram of the i8275 CRT controller.
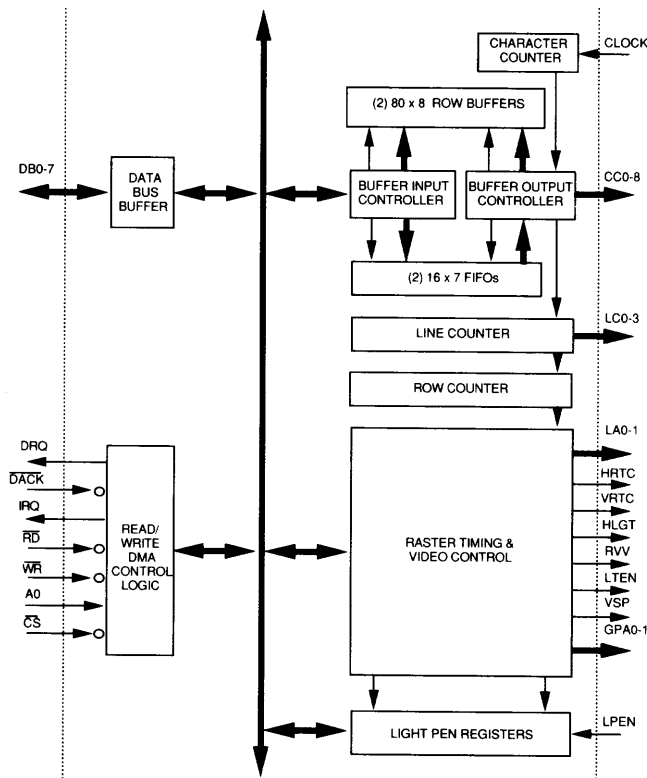
	Pin Name	Description	Type
Microprocessor System Interface Signals	CS A0 RD WR DB0-DB7 IRQ DRQ DACK CCLK V$_{CC}$, GND	Chip Select Register Address Read Control Signal Write Control Signal Data Bus Lines Interrupt Request DMA Request DMA Acknowledge Character Rate Clock Power (+5 V) and Ground	Input Input Input Input Bidirectional, Tristate Output Output Input Input
Character Generator Signals	CC0-CC6 LC0-LC3	Character Code (Inputs to Character Generator) Scan Line Counter	Output Output
CRT Monitor Signals	HRTC VRTC VSP LTEN RVV HGLT LA0, LA1 GPA0, GPA1 LPEN	Horizontal Retrace (HSYNC) Vertical Retrace (VSYNC) Video Suppression (blanking) Light Enable (cursor) Reverse Video Indicator Highlight Indicator Line Attribute Code Signals General Purpose Attribute Code Signals Light Pen Detect Signal	Output Output Output Output Output Output Output Output Input

Figure 2.4-7 i8275 CRT contoller
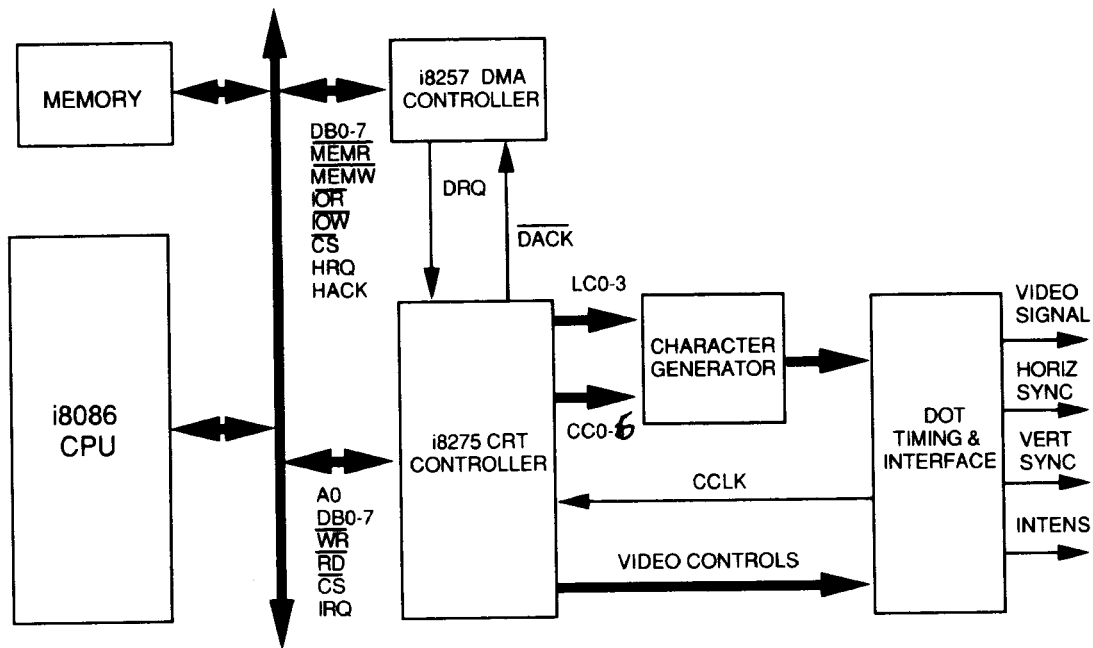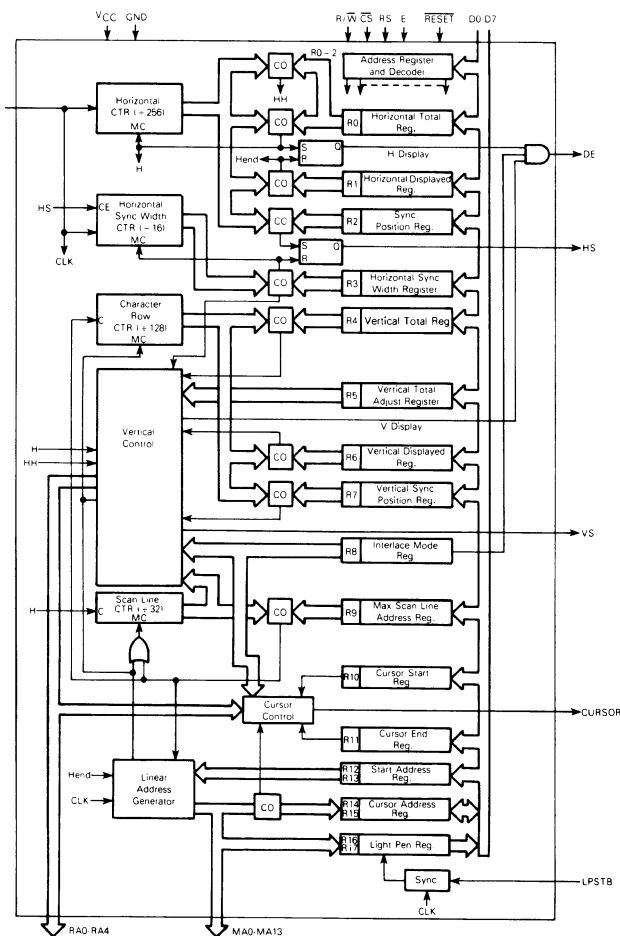
Figure 2.4-8 Interfacing an I8275 CRTC to an I8086 CPU

2.4.5.2 Interlaced Memory Access (Dual-Ported Memory Access)

The 6845 CRT controller was originally developed by Motorola as a 6800-family peripheral chip. While intended primarily for alphanumeric displays, it can be used for graphics displays. Figure 2.4-9 shows a block diagram of the 6845. While it appears complex at first, it is simply a programmable implementation of the counter chain previously described. The clock input is at the character rate. Like most CRT controller chips, this chip is too slow to operate at the dot rate, so the dot timing must be performed externally. The 6845 allows the number of characters per line and many other display parameters to be programmed by the microprocessor. The registers are shown at the right side of the block diagram. Register R0 sets the total number of characters per line (including blanked character positions). The blocks labelled "CO" are comparators, which test the values in the counters against the limits programmed in the registers.

The screen format is determined by the values in the registers. Registers R0 to R3 determine the timing within each line. The DE (display enable) signal is high during active video, it can also be thought of as an active-low blanking signal. The horizontal total register (R0) determines the number of character clocks that make up an entire scan line, including blanking and retrace. The horizontal displayed register (R1) sets the number of actual characters displayed; the difference between R0 and R1 determines the horizontal blanking time. The position of the horizontal sync pulse is independently set by R2, and the width of the sync pulse is set by R3. The unit for all these settings is one character time.

Registers R4 to R7 set the vertical timing in a similar manner. The vertical total register (R4) sets the total number of character rows in the complete raster, including rows that are blanked. Because this register is set in units of one character row (which is typically 9 to 14 scan lines), it will usually not be possible to specify the exact number of scan lines required for the complete raster. The vertical adjust register (RS) sets the number of additional lines needed to make the complete raster. Register R6 sets the total number of character rows displayed, and R7 sets the number of character

rows of delay before the vertical sync pulse is begun. The sync pulse width is fixed at 16 scan lines.

	Pin Name	Description	Type
Microprocessor System Interface	D0-D7 CS RS R/W Φ2 (E) CCLK RESET V_CC, V_SS	Data Bus Chip Select Register Select Read/Write Select System Synchronization Signal Character Rate Clock Reset Power (+5 V) and Ground	Bidirectional, Tristate Input Input Input Input Input Input
Screen Memory and Character Generator Signals	MA0-MA13 (CC0-CC7, CR0-CR5) RA0-RA3 RA4/STB	Screen Memory Address Bus (Linear) Screen Memory Column/Row Addresses Raster (Scan Line) Address Signals Raster Address/Update Address Strobe	Output Output Output Output
CRT Monitor Interface Signals	HSYNC VSYNC DISPEN CURSOR LPSTB	Horizontal Synchronization Vertical Synchronization Display (Video) Enable Cursor Enable Light Pen Strobe	Output Output Output Output Input

Figure 2.4-9 The 6845 CRTC block diagram

The 6845 can produce interlaced or non-interlaced sync signals.

The microprocessor interface to the 6845 is straightforward, but since it is designed for 6800-type microprocessors, some additional logic is needed for Intel-style processors. The 6845 connects directly to an 8-bit data bus. All transfers are timed by the E (enable) signal, which is driven by the Φ2 or E signal in 6800-family systems. Figure 2.4-10 shows a block diagram of a CRTC system and Figure 2.4-11 shows the timing interlacing between the CRTC and CPU
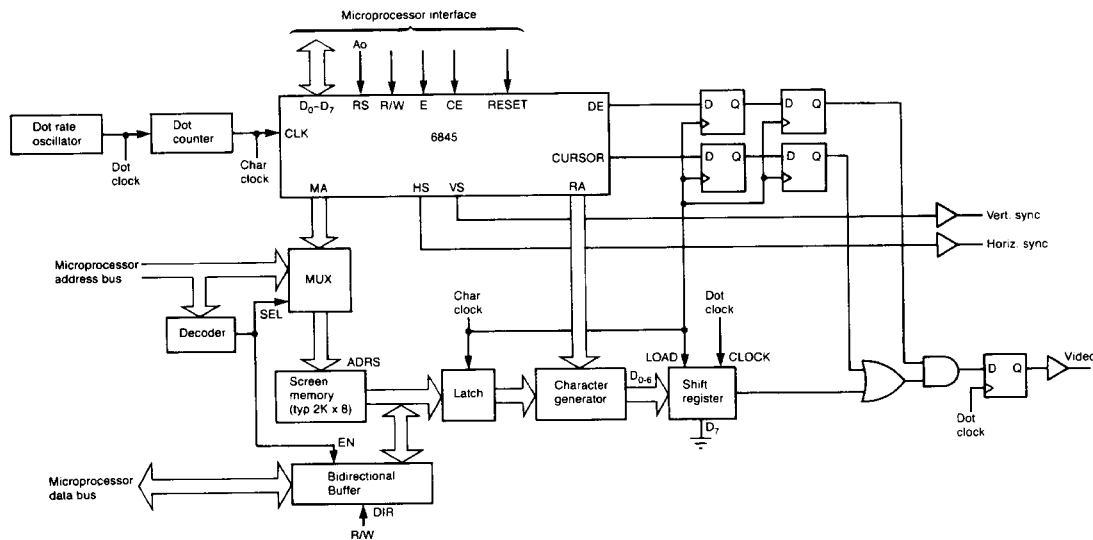

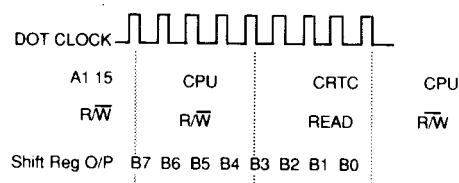Figure 2.4-10 Block diagram of a 6845-based CRTC system

Figure 2.4-11 Timing interlacing

2.5 Graphic CRT Displays

Several techniques are used to generate raster-scan graphics displays.

2.5.1 Graphics Generation Techniques

Graphics capability is obtained by using a *bit-mapped* display, in which there is 1 bit (or more) of screen memory for each possible dot (pixel) on the display. For monochrome displays, only 1 bit/pixel is needed. For colour or grey scale, additional bits are required. For example, using 8 bits/pixel provides 256 different colours or grey levels.

Table 2.5-1 Bit-Mapped Graphics Display Memory Requirement shows, the memory requirements for graphics displays increase rapidly as resolution increases. Note that the terms high-resolution and low-resolution are relative and depend on the application. In a home computer, 640 x 400 may be high-resolution, but to qualify for that designation in a computer-aided design application, 1280 x 1024 is required.

Table 2.5-1 Bit-Mapped Graphics Display Memory Requirement

Resolution	No.of pixels	Memory in bytes for various numbers of bits per pixel		
		1 bit	4 bits	8 bits
240 X 200	48,000	6K	24K	48K
640 X 350	224,000	28K	112K	224K
640 X 480	307,200	38k	152K	304K
1024 X 768	786,432	96K	192K	384K
1280 X 1024	1,310,720	160K	640K	1280K

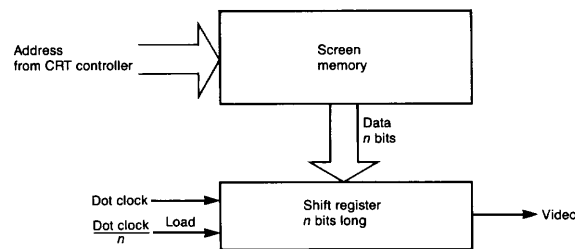Figure 2.5-1 Monochrome graphics video generator shows a Monochrome graphics video generator

Figure 2.5-1 Monochrome graphics video generator

To provide grey levels, more than 1 bit/pixel is required; 8 bits/pixel provides 256 gray levels, enough for virtually any application. The number of bits per pixel is often referred to as the number of *bit planes,* since the memory can be visualized as a number of memory planes, each with 1 bit/pixel. In the actual storing of bit information, there are the bit plane and packed integer format. Figure 2.5-2 shows the video generation circuit for 256 gray levels. Each byte in the screen memory corresponds to a single pixel. All 8 bits are combined by the digital-to-analog converter to produce one of 256 possible video signal levels.
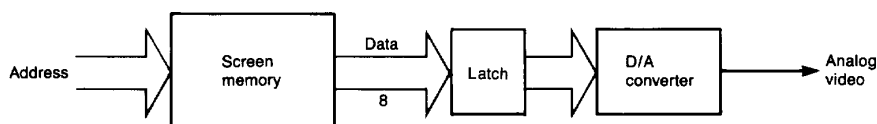

Figure 2.5-2 Graphic video for 256 gray levels.

2.5.2 Color CRT

Color CRT controllers must produce three video signals: red, green, and blue. The simplest implementation uses one bit for each of these signals and allows a total of eight different colors. Figure 2.5-3 shows a block diagram for the video-generation portion of an eight-color CRT controller.
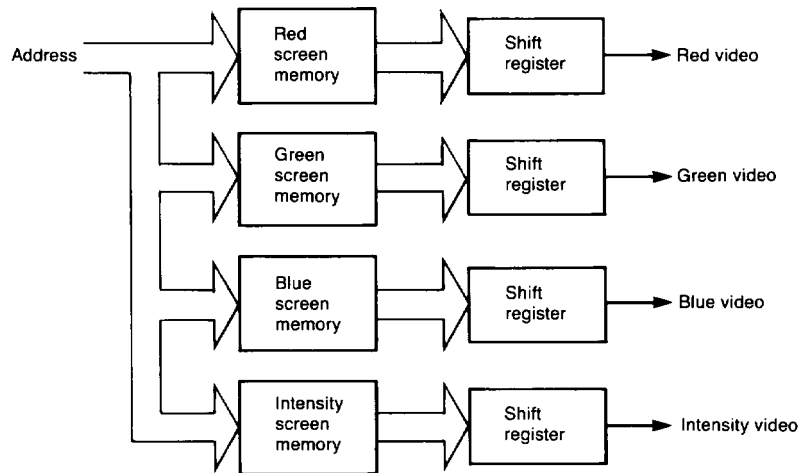

Figure 2.5-3 Video generation for digital RGB + intensity bit.

The eight-colour technique described above is easily extended to 16 colours by adding a fourth bit for luminance, used in CGA. For more colours, analogue RGB monitors are used, and more than one bit per colour is required. There is one memory array and one D/A converter for each colour. If four bits are used for each colour, a total of 2^{12}, or 4096, different colours can be displayed. While 4096 colours are adequate for most applications, more are needed for realistic (true-to-life) colour rendition. High-end systems use as many as 8 bits per colour (24 bits/pixel), for a total of over 16.8 million different hues.
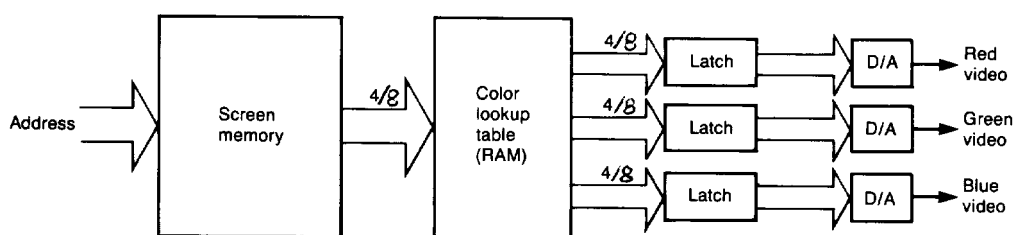

Figure 2.5-4 Analogue RGB video generation with CLUT

2.5.3 Colour Lookup Tables

Although it is desirable to have a large number of hues available, most images use a relatively limited selection. A *colour lookup table* can be used to take advantage of this characteristic to reduce the amount of screen memory required and also the accessing time required for a full frame of graphic. Figure 2.5-3 shows a system using a colour lookup table. The lookup table consists of high-speed RAM that is written by the applications program. (The figure does not show the multiplexers required on the connections to the lookup table RAM to allow access by the microprocessor.) The

lookup table translates a "colour number" from the screen memory to RGB data for the DAC.

A common system uses 8 bits/pixel in the screen memory and provides 8 bits for each colour from the lookup table. This would require a 256 x 24 lookup table and would allow any 256 from a palette of 16.8 million colours to be displayed. The relatively small lookup table greatly reduces the amount of screen memory that would be required for a comparable choice of colours without using a lookup table.

2.5.4 Video RAM

The data in a screen memory must be displayed continuously at the same time as it is being created. The data rate for a video display device is such that the memory used to from the image cannot be easily shared between the display and the processor. A special form of memory, known as the *dual port memory*, allows access by two different circuits at the same time is used. One port, the standard random access memory (RAM) interface, is connected to the computer and the other, a sequential access port, is used by the screen. This special memory device is known *as video random access memory* (*VRAM*) and usually form part of a special interface card called a video adaptor.