A Digital Readout Technique for Capacitive Sensor Applications

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Abstract—**The difference between two capacitors is measured digitally using a charge redistribution technique incorporating a comparator, MOS switches, a successive approximation register (SAR), and a digital-to-analog converter (DAC). The technique is insensitive to comparator offset and parasitic capacitance, and the effect of MOS switch charge injection is measured and canceled. Extensive measurements have been made from test chips fabricated in 3-μm CMOS technology. Detection of percent differences of less than 0.5 percent on 20–100-fF capacitors has been successfully demonstrated.**

I. Introduction

THE measurement of capacitance difference is important for integrated sensors. Silicon structures sensitive to shear, acceleration, and pressure are examples of where a capacitive readout scheme is advantageous [1], [2]. In addition, changes in dielectric permittivity manifest themselves as a change in capacitance [3].

For integrated sensing structures, the readout capacitance can be on the order of tenths of a picofarad which complicates the capacitance detection circuitry. One detection method utilizes an oscillator which drives a capacitive bridge circuit. A change in capacitance relative to a reference capacitance produces an output voltage or shift in frequency which can be detected by an external circuit [4], [5]. For particular readout circuits, parasitic capacitances can cause an error in the measurement.

Recently, the advent of switched-capacitor techniques has led to new and innovative methods of capacitance detection [6], [7]. However, problems appear that are inherent to all switched-capacitor circuits. MOS switch charge injection, clock feedthrough, and circuit noise become major limiting factors in circuit performance.

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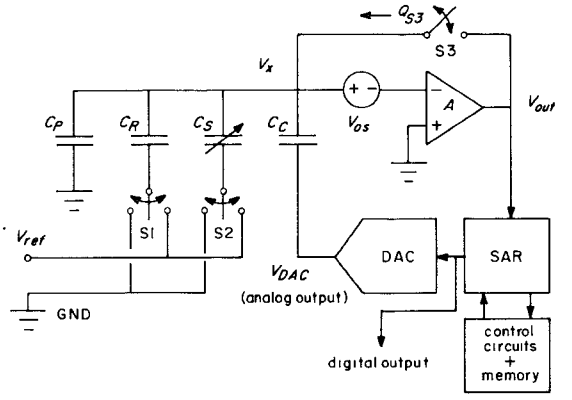

Fig. 1. Measurement system block diagram.

This paper describes a digital technique for measuring capacitance differences. It has its origins in charge redistribution A/D converters, and does not suffer from parasitic capacitance, op-amp offset, or charge injection problems.

II. Theory

In 1979, an algorithm was developed that allowed calculation of ratio errors from a sequence of measurements based on charge redistribution [8]. This technique was implemented to study capacitor mismatch errors that cause linearity errors in charge redistribution A/D converters. MOS switch charge injection, however, was ignored due to the large size of the capacitors. Elimination of charge injection sources is crucial in obtaining higher resolution and smaller errors in these A/D converters. The self-calibration technique allowed higher resolution by eliminating errors caused by component mismatch and charge injection [9]. The technique can be equally applied to measure capacitance differences and random or controlled sources of charge injection. Since in sensor applications the sense capacitors may be much smaller than a picofarad, MOS charge injection causes a large error and must be canceled. The technique can measure errors due to capacitive mismatch, comparator offset, and charge injection and can compensate a system that has these errors. It is ideal for measuring capacitance differences (as in capacitive sensors) and reducing inherent circuit errors.

The basic circuit is shown in Fig. 1. It consists of the sense and reference capacitors C_S and C_R, respectively, the

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coupling capacitor C_C, five MOS switches, a voltage comparator, a digital-to-analog converter (DAC), a successive approximation register (SAR), and a memory register with associated logic capable of signal inversion. The nonidealities of the circuit appear as the offset of the comparator (V_{os}) and its finite gain (A), parasitic capacitance to ground (C_P), and switch charge injection (Q_{S3}). To better understand how these nonidealities are taken into account, an ideal system is first analyzed, then second-order effects are added later. In the assumption of an ideal circuit, $V_{os}=0$, $C_P=0$, $Q_{S3}=0$, $A=\infty$, and DAC quantization error is negligible.

The measurement technique proceeds in two steps. In step 1, switch $S3$ is closed so that V_x is at ground. Switch $S1$ is set to V_{ref} and switch $S2$ is set to ground. The DAC output is also set to ground. The charge at the top node in this configuration is $Q_1=-V_{\text{ref}}C_R$. The comparator is implemented so that when the feedback loop is closed with switch $S3$, V_x is forced to a virtual ground via the DAC. In step 2, $S3$ is opened, then $S1$ is set to ground and $S2$ is set to V_{ref}. The successive approximation search begins after this sequence and continues until the SAR reaches its quantization limit and stops. If the SAR, DAC, and voltage comparator are ideal, then the voltage from the DAC (V_{DAC}) precisely forces the top node voltage (V_x) to zero. The charge at the top node is thus $Q_2=-V_{\text{ref}}C_S-V_{\text{DAC}}C_C$. By charge conservation, $Q_1=Q_2$ and it follows that

$$V_{\text{DAC}}=\frac{V_{\text{ref}}(C_R-C_S)}{C_C}. \tag{1}$$

The output of the DAC produces a voltage proportional to the capacitance difference of C_S and C_R. Appropriate choices of V_{ref} and C_C can be made so that the maximum dynamic range of the DAC can be utilized. The parameter $\Delta C/C$ can be found by multiplying the numerator and denominator by C_R or C_S and rearranging so that

$$\frac{\Delta C}{C}=\left[\frac{V_{\text{DAC}}}{V_{\text{ref}}}\right]\left[\frac{C_C}{C}\right] \tag{2}$$

where ΔC is C_R-C_S and C is a normalizing capacitance, typically either C_R or C_S. Notice that the result is a product of two ratios: a voltage ratio that can be measured easily and a capacitance ratio.

III. Nonidealities

Several errors are introduced when the algorithm is implemented due to component nonidealities. Referring to Fig. 1, the comparator has an offset V_{os} and a finite gain A while the switch $S3$ injects a charge Q_{S3} when opened. A parasitic capacitance to ground C_P exists as well as a DAC quantization error of $\pm\frac{1}{2}$ LSB. It is found that the measurement algorithm can be implemented in either a closed-loop or open-loop topology. They differ only in that the closed-loop topology uses the feedback loop containing switch $S3$ and the open loop does not. The difference between the two is that in closed loop, the voltage V_x is initially the offset of the comparator since it is connected like a voltage follower. Also, it is important to note that if the feedback path due to switch $S3$ is to cause $V_x=V_{os}$, the comparator must operate as a high-gain op amp and cannot be a regenerative latch comparator with only high or low digital outputs.

In open loop when the SAR/DAC feedback loop is initiated, the operation of the comparator can be limited to strictly digital output since it is never directly connected in negative feedback; rather the SAR/DAC generates the appropriate analog signal to the coupling capacitor as feedback. Usually, the comparator can be designed so that it can act as an op amp when the loop is closed [9]. In the open-loop topology, the top node is grounded in the first step so that the feedback loop through $S3$ is never established. Thus the comparator may always have digital outputs. Since the analog signal for measurement of small capacitors is usually small, a monolithic preamplifier can be used to buffer the voltage to an off-chip comparator in this configuration.

A. Quantization Error

The quantization error of the DAC contributes an error to the measurement. Assuming that V_{DAC} is in error by $\pm\frac{1}{2}$ LSB, the amount of error transferred to V_x can be easily shown to be

$$V_x=V_{os}\pm\frac{1}{2}\ \text{LSB}\left[\frac{C_C}{C_P+C_R+C_S+C_C}\right]=V_{os}\pm\delta\left(\frac{1}{2}\ \text{LSB}\right) \tag{3}$$

where δ is the capacitive divider ratio

$$\delta=\left[\frac{C_C}{C_P+C_R+C_S+C_C}\right]=\frac{C_C}{C_{\text{total}}}. \tag{4}$$

This is a simple capacitive divider. Any change in voltage ΔV at V_{DAC} results in a change in voltage $\delta\Delta V$ at V_x. Repeated use of the DAC's voltage output for subsequent measurements will accumulate this error in the worst case; however, averaging can reduce this problem.

B. Charge Injection

Charge injection can also be measured using this technique. Since the charge that $S3$ injects is independent of capacitor difference, it causes an error in the measurement. To correct for it, an additional step is added which will be denoted as the calibration cycle. The capacitive mismatch measurement will be denoted as the measurement cycle. The calibration and measurement cycles inherently eliminate the comparator offset in the closed-loop topology. In the open-loop topology, the offset is measured, then canceled.

The calibration procedure begins by measuring the charge injection. $S1$ is set to V_{ref} and both $S2$ and V_{DAC}

are set to ground. $S3$ is opened and the SAR/DAC is initiated. The calibration voltage at the output of the DAC can be shown to be

$$V_{\mathrm{DAC}_{cal}} = \frac{-Q_{S3}}{C_C} \pm 2\Delta V \tag{5}$$

in the closed-loop topology and

$$V_{\mathrm{DAC}_{cal}} = V_{os}\left[\frac{C_P + C_R + C_S + C_C}{C_C}\right] + \frac{-Q_{S3}}{C_C} \pm 2\Delta V \tag{6}$$

in the open-loop topology. $\pm \Delta V$ is the quantization error of the DAC. Charge injection must be measured since it upsets the charge conservation assumption made in the earlier ideal circuit analysis. If it is taken into account, then charge due to the capacitors can be accurately determined and hence so can the capacitance difference. Once the switch injection voltage is measured, it can be stored in a RAM. When the negative of $V_{\mathrm{DAC}_{cal}}$ is applied to the coupling capacitor, a voltage at V_x is created that cancels out the error voltage generated by the switch injection charge. Alternatively, one can think of the DAC as creating a positive charge on the coupling capacitor that is just large enough to cancel the negative switch injection (assuming an NMOS switch). This is equivalent to analog voltage subtraction at V_x. Subtraction of the digital data is an alternate method of eliminating the charge injection error.

In the measurement cycle, $S3$ is closed, $S1$ is set to V_{ref}, $S2$ to ground, and V_{DAC} to the negative of the voltage measured during the calibration step. This switch sequence is exactly the same as in the ideal analysis except that V_{DAC} is at some voltage other than ground. $S3$ is then opened and the positions of $S1$ and $S2$ are reversed. The SAR/DAC is initialized, and the output of the DAC becomes

$$V_{\mathrm{DAC}_{meas}} = \frac{V_{\mathrm{ref}}(C_R - C_S)}{C_C} \pm 4\Delta V \tag{7}$$

for both open-loop and closed-loop topologies. A disadvantage of the open-loop topology is that a large comparator offset may yield a calibration voltage larger than the DAC maximum voltage and calibration becomes impossible. The closed loop is preferred for this reason. For testing purposes, however, the open-loop topology is easier to implement.

C. Parasitic Capacitance

Parasitic capacitance imposes a constraint on the system. A large C_P reduces the divider ratio δ. If δ becomes too small, V_x becomes pinned by the large C_P and the DAC is not able to adjust V_x. The $\pm \Delta V$ error becomes limited by the capacitive divider ratio and not the quantization error because the minimum amount of control the DAC has is $\delta(\pm \Delta V)$ which may be smaller than the comparator resolution. A smaller C_P increases δ but also increases the kT/C noise so that a trade-off is introduced.

Capacitance mismatch ratio for both topologies is

$$\frac{\Delta C}{C} = \left[\frac{V_{\mathrm{DAC}_{meas}}}{V_{\mathrm{ref}}}\right]\left[\frac{C_C}{C}\right] \pm \left[\frac{4\Delta V}{V_{\mathrm{ref}}}\right]\left[\frac{C_C}{C}\right] \tag{8}$$

where C is either C_R or C_S. It is the same as (2) except for the error term

$$\pm\left[\frac{4\Delta V}{V_{\mathrm{ref}}}\right]\left[\frac{C_C}{C}\right]. \tag{9}$$

This error term determines the minimum resolvable capacitance change for a single measurement. The effect of the parasitic capacitance appears as a constraint on the comparator resolution, as evidenced by (4).

D. Other Nonideal Effects

An MOS switch that is turned off can leak from the reverse-biased p-n junction at the body and source. Normal reverse saturation current from a p-n junction is typically 10 nA/cm^2 in MOS processes at room temperature. If the area of the MOS switch source region is 100 μm^2, the reverse leakage current is approximately 10 fA. If the switch is open for 100 μs, the charge transferred is approximately six electrons. This effect becomes significant only at low clock frequencies and at elevated temperatures. Leakage current introduces an extra charge source in the measurement and can be measured using this technique if the clock frequency is low enough.

Due to the proximity and similarity of the test capacitors used in this work, both the voltage and temperature coefficients of capacitance did not effect the measurement. Since each capacitor experiences similar conditions in the technique, the effects of temperature and voltage coefficient tend to track each other and appear as a common-mode error that cancels in the differential measurement.

The thermal noise generated by an MOS channel causes a variation in injected charge each time $S3$ is opened:

$$(V_n)^2_{\mathrm{rms}} = \frac{kT}{C}. \tag{10}$$

This noise is sampled on the capacitors when the switch is turned off. It can be shown that an MOS channel can be treated as a noiseless open circuit when turned off [10]. Increasing C can reduce this noise, but increases the parasitic capacitance if the sense and reference capacitors are already determined to be small. Complete cancellation is not possible with an individual measurement, but digital averaging can reduce its effect significantly since the noise is random.

IV. Experimental Results

To test the theory of the charge redistribution technique on capacitance difference measurements, a test chip was designed and fabricated by MOSIS using a 3-μm p-well

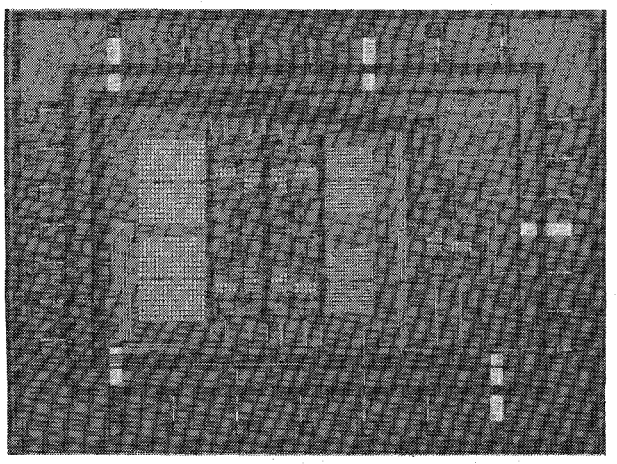

Fig. 2. Die photo of test chip.

TABLE I
TEST CAPACITOR SIZES[1]

C	Area (μm^2)	Capacitance Range (fF)
$C_{R_{large}}$	2132	75–110
$C_{S_{large}}$	2120	74–110
$C_{R_{small}}$	620	22–31
$C_{S_{small}}$	620	22–31
C_{C1}	1696	60–85
C_{C2}	848	30–42
C_{C3}	248	9–12
C_{P1}	31744	1100–1600
C_{P2}	108544	3800–5400

[1]Ranges are given since measurements on absolute capacitance values were never performed. Ranges are calculated from MOSIS vendors specifications.

CMOS technology. Its main purpose was to demonstrate difference measurements of metal/poly capacitors that are comparable in capacitance value to integrated sensing structures. An open-loop topology was implemented. An on-chip isolation amplifier was used to buffer the sensitive node to a comparator off-chip.

Three CMOS runs using MOSIS were made. Fig. 2 shows the die photograph of one of the chips. Five chips per run were obtained. As is shown in Table I, the test capacitors ranged from 20 to 100 fF. MOSIS vendors must meet requirements of metal one-to-poly/diffusion capacitances of 0.035–0.05 fF/μm^2 which indicates an oxide thickness range for the test capacitors of approximately 700–1000 Å. Measurements were also made for each set of sense and reference capacitors to test for any residual polarization [11]. The exact areas and estimated range of capacitance values for all capacitors are shown in Table I. Fig. 3 shows the positions of the circuits on the test chip. Circuits 1 and 3 have the same switch size as do circuits 2 and 4, while circuits 1 and 3 differ in parasitic capacitance as do circuits 2 and 4. Circuit 5 has no intentionally added parasitic capacitance.

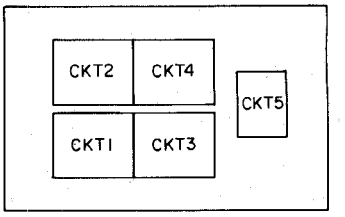

Fig. 3. Positions of circuits on test chip.

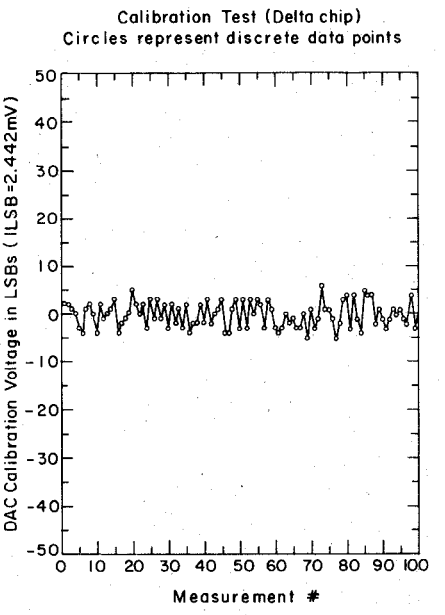

Fig. 4. Cancellation of charge injection and comparator offset.

Shown in Fig. 4 is a graph of calibration voltage output after cancellation. To measure the success of the calibration technique in eliminating charge injection, a calibration test was used. The calibration voltage was measured 100 times, then averaged. The negative of this value was then applied to the coupling capacitor and the calibration cycle was repeated. Cancellation of the charge injection should result in a DAC output voltage near 0 V. The data for all the chips show that on average the DAC calibration voltage is much less than 1 LSB, demonstrating the expected noise reduction from averaging.

The measurement data for one representative test chip are presented in Table II. A large amount of data were obtained since each of the 15 chips contained five separate circuits and each circuit had two sets of sense and reference capacitors. Since in sensor applications extensive averaging may not be possible due to speed considerations, the data represent a reasonable averaging of 16 times. In addition, residual polarization was observed to be negligible. Results compare favorably with previous work on MOS capacitors [11]. Standard deviations are for 16 measurements in time for one chip rather than between differing chips. The deviations of the measurements fall in the range of that expected from (5) and (7). We believe that the discrepancy in standard deviations between the negative and positive measurements is caused by slight asymmetrical noise coupling of the control signals to the test

TABLE II
MEASUREMENT DATA

Parameter	CKT1		CKT3		CKT5	
	C_{large}	C_{small}	C_{large}	C_{small}	C_{large}	C_{small}
Value (fF)	90	26	90	26	90	26
$V_{DAC_{+meas}}$ (V)	0.415	3.66E-3	0.287	7.17E-3	0.258	4.43E-3
Std. dev. (LSB)	3.63	3.38	3.14	2.94	2.56	2.69
$\frac{\Delta C}{C}$ (%)	3.32	0.100	2.30	0.196	2.07	0.121
Std. dev. (%)	0.071	0.23	0.061	0.20	0.050	0.18
$V_{DAC_{-meas}}$ (V)	-0.418	-2.44E-3	-0.287	-8.39E-3	-0.257	9.16E-4
Std. dev. (LSB)	2.28	1.63	3.00	2.33	2.17	1.89
$\frac{\Delta C}{C}$ (%)	-3.34	-6.67E-2	-2.30	-0.230	-2.05	2.51E-2
Std. dev. (%)	0.045	0.11	0.059	0.16	0.042	0.13

1. Test data averaged 16 times.
2. CKT1 has $C_P = 5$ pF, CKT3 has $C_P = 2$ pF, CKT5 has $C_P = 1$ pF
3. +meas denotes a positive measurement where C_R has V_{ref} across it in step 1.
4. -meas denotes a negative measurement where C_S has V_{ref} across it in step 1.

TABLE III
MEASUREMENT SYSTEM PARAMETERS

Switching speed	100 kHz
Sucessive Approximation Register	12-bit
Digitial-to-Analog Converter	12-bit
1 LSB	2.44 mV
Conversion speed	120 μsec
Positive analog supply	5 V
Negative analog supply	-5 V
Reference Voltage V_{ref}	+5.00000 V
Temperature	$\approx$ 25°C
Resolution	$\leq$ 0.05fF

chip. This is currently being corrected. Measurement system characteristics are shown in Table III.

The small capacitors differed by very little, on the order of 0.1–1 percent. This resolution limit was reached by averaging only 16 times. One of the larger capacitors was made approximately 3 percent larger than the other one. As shown in Table II, measurements resolved this difference. Since a large amount of theoretical and experimental work has been done on random MOS capacitor mismatches [12], [13], this paper did not attempt to seek correlations to previous work. From the data in Table II, standard deviations indicate that the resolution of a single measurement is close to 1000–1500 electrons, corresponding to nearly 0.05 fF in this study. Averaging can significantly increase the resolution but at a cost of increased time.

Two different switching sequences were used in this work to measure capacitance differences and residual polarization. Several alternate sequences will yield $V_x \propto \Delta C$. Table IV shows some of these sequences if the only available switching voltages are $\pm V_{\text{ref}}$ and ground. V_{R1} and V_{S1} are the voltages applied to the bottom plates of the reference and sense capacitors in step 1, respectively, while V_{R2} and V_{S2} are the voltages applied in step 2. Sequences 8–10 yield the same result as given by (7) while 9 and 10 yield (7) multiplied by two. The many possible switching sequences make it possible for the sensor designer to choose the appropriate sequence that best suits the particular application. For example, sequences 6 and 7 have 0 V across both capacitors in step 2 so that any change in either capacitor during the measurement cycle will not introduce an error. This may be important if both capacitors change during a sensing operation.

TABLE IV
ALTERNATE SWITCHING SEQUENCES

Sequence number	V_{R1}	V_{S1}	V_{R2}	V_{S2}
1	0	V_{ref}	V_{ref}	0
2	0	0	V_{ref}	$-V_{ref}$
3	0	0	$-V_{ref}$	V_{ref}
4	0	$-V_{ref}$	$-V_{ref}$	0
5	V_{ref}	0	0	V_{ref}
6	V_{ref}	$-V_{ref}$	0	0
7	$-V_{ref}$	V_{ref}	0	0
8	$-V_{ref}$	0	0	$-V_{ref}$
9	V_{ref}	$-V_{ref}$	$-V_{ref}$	V_{ref}
10	$-V_{ref}$	V_{ref}	V_{ref}	$-V_{ref}$

V. CONCLUSIONS

This paper demonstrates a technique that can measure capacitance differences with a resolution of 0.05 fF on capacitors in the 20–100-fF range in the presence of parasitic capacitances nearly 100 times larger. It is shown that nonideal effects such as charge injection, parasitic capacitance, and voltage and temperature coefficients are either negligible or can be calibrated. Junction leakage, threshold-voltage hysteresis, and capacitor hysteresis are shown to be negligible. Digital averaging can increase resolution but increases measurement time.

The charge redistribution technique measures capacitance differences and can be applied directly to sensor design. The technique is simple, requiring three capacitors, a voltage comparator, a successive approximation register, and a digital-to-analog converter. It provides extremely high resolution and an inherently digital readout. Its simplicity and compatibility with digital signal processing make it ideally suited for readout in sensor systems requiring a capacitance difference measurement.

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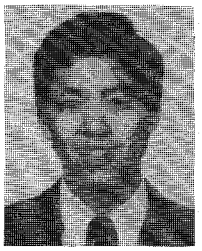

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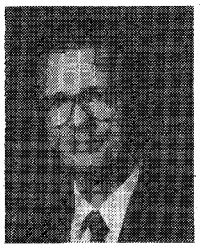

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