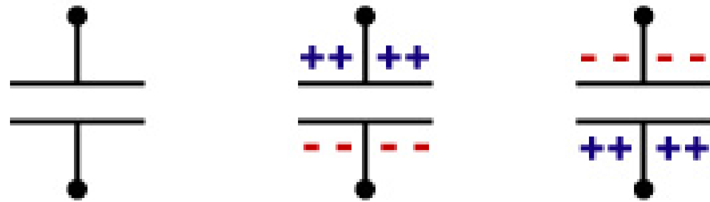
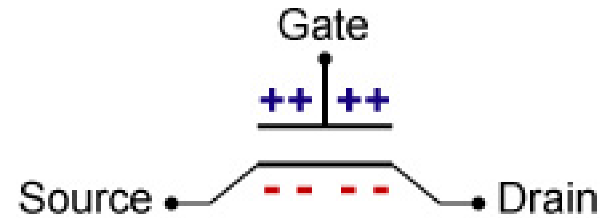
JFETs AND MESFETs

Introduction

Field effect = Induction of an electronic charge due to an electric field

Example: Planar capacitor





Why would an FET made of a planar capacitor with two metal plates, as shown above, not work well?

Why do FETs made of semiconductors work well?

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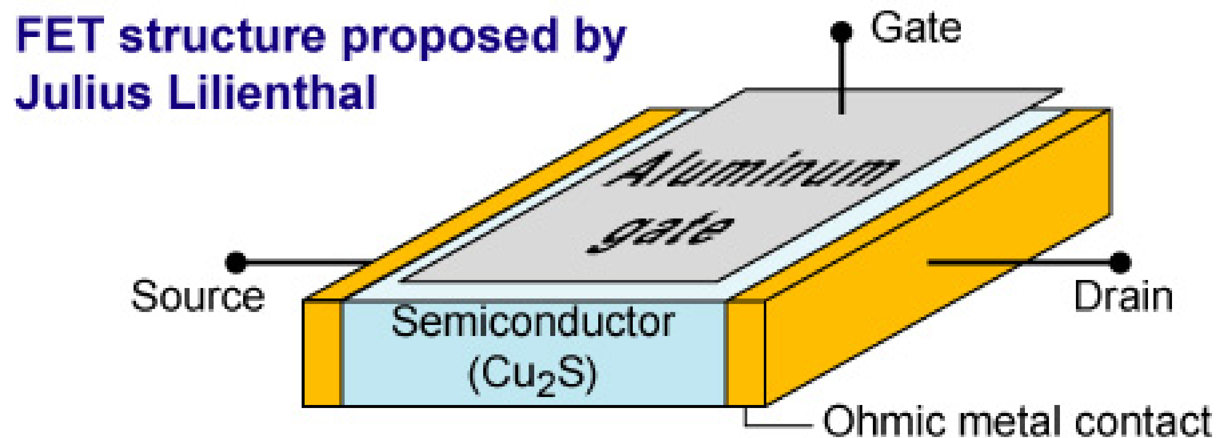
History of FET

As early as 1925, an FET was proposed by Julius Edgar Lilienfeld. A US patent was issued in 1930 (Lilienfeld, 1930, U. S. Patent 1,745,175).



In the early 1930s, Oskar Heil described an FET structure similar to the modern junction field-effect transistor (Heil, 1935, British Patent 439,457).

Neither Lilienfeld nor Heil were able to construct a working device.

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Other milestones in transistor development:

1925	FET proposal by Lilienfeld
1930	Junction FET proposal by Heil
1947	Point-contact transistor by Brattain and Bardeen of Bell Laboratories
1949	Bipolar junction transistor by Brattain, Bardeen, and Shockley of Bell Laboratories
1958	First Integrated Circuit by Jack Kilby of Texas Instruments
1959	Silicon planar process: Procedure resembles integrated circuits of today by Robert Noyce of Fairchild
1960s	PMOS process
1970s	NMOS process
1980s	CMOS
1990s	CMOS, BiCMOS

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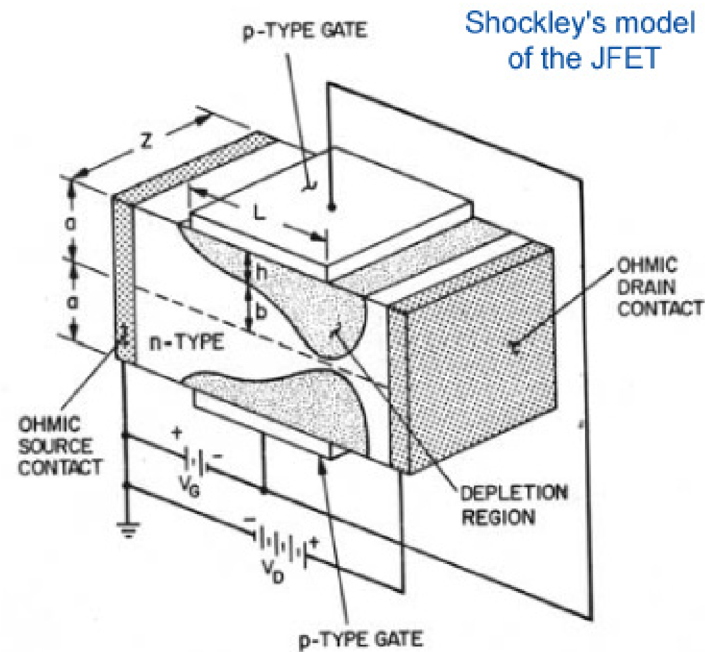
Shockley’s model of a junction FET:



… beautiful illustration of concept of JFET

… is the device proposed by Shockley **practical**?

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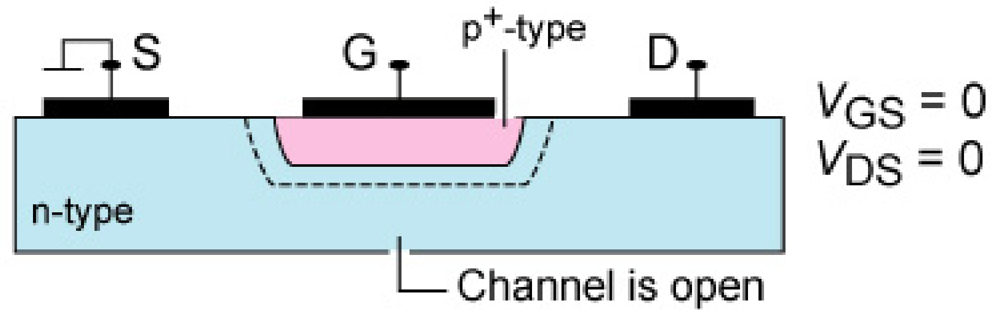
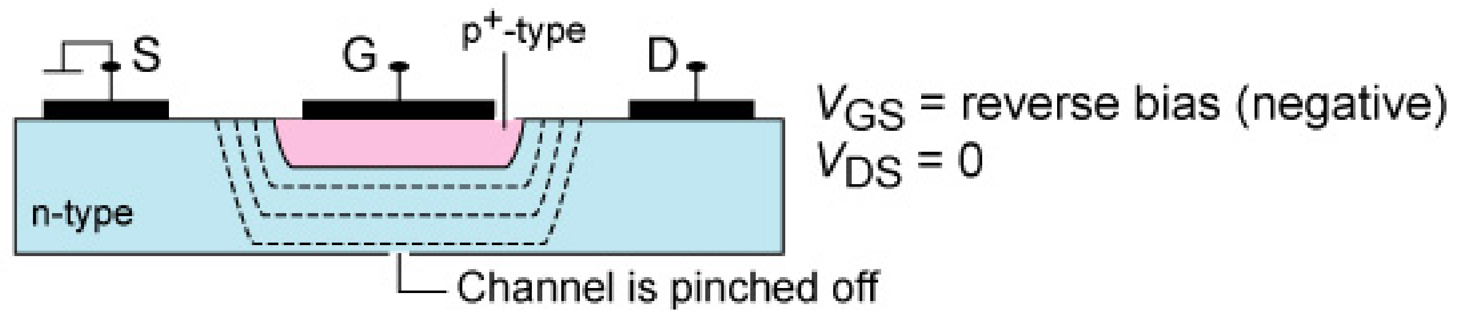
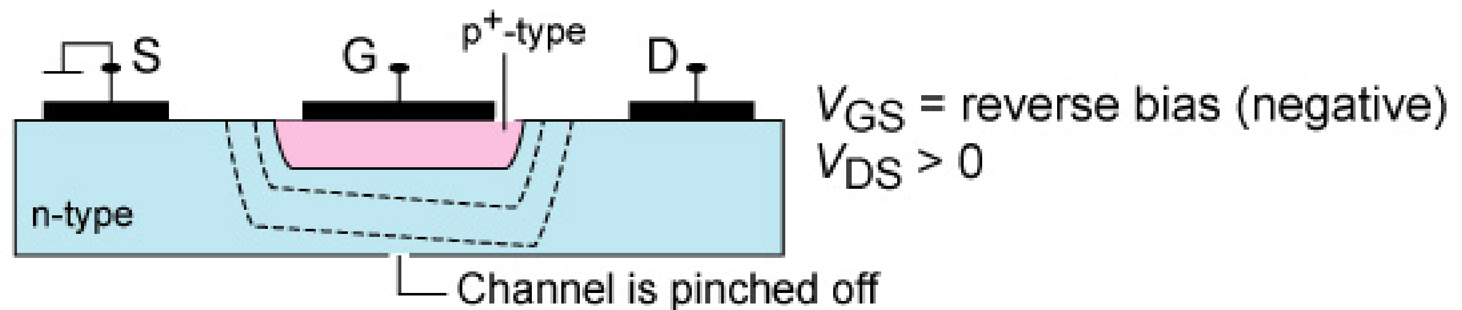
JFET = PN junction FET

JFET







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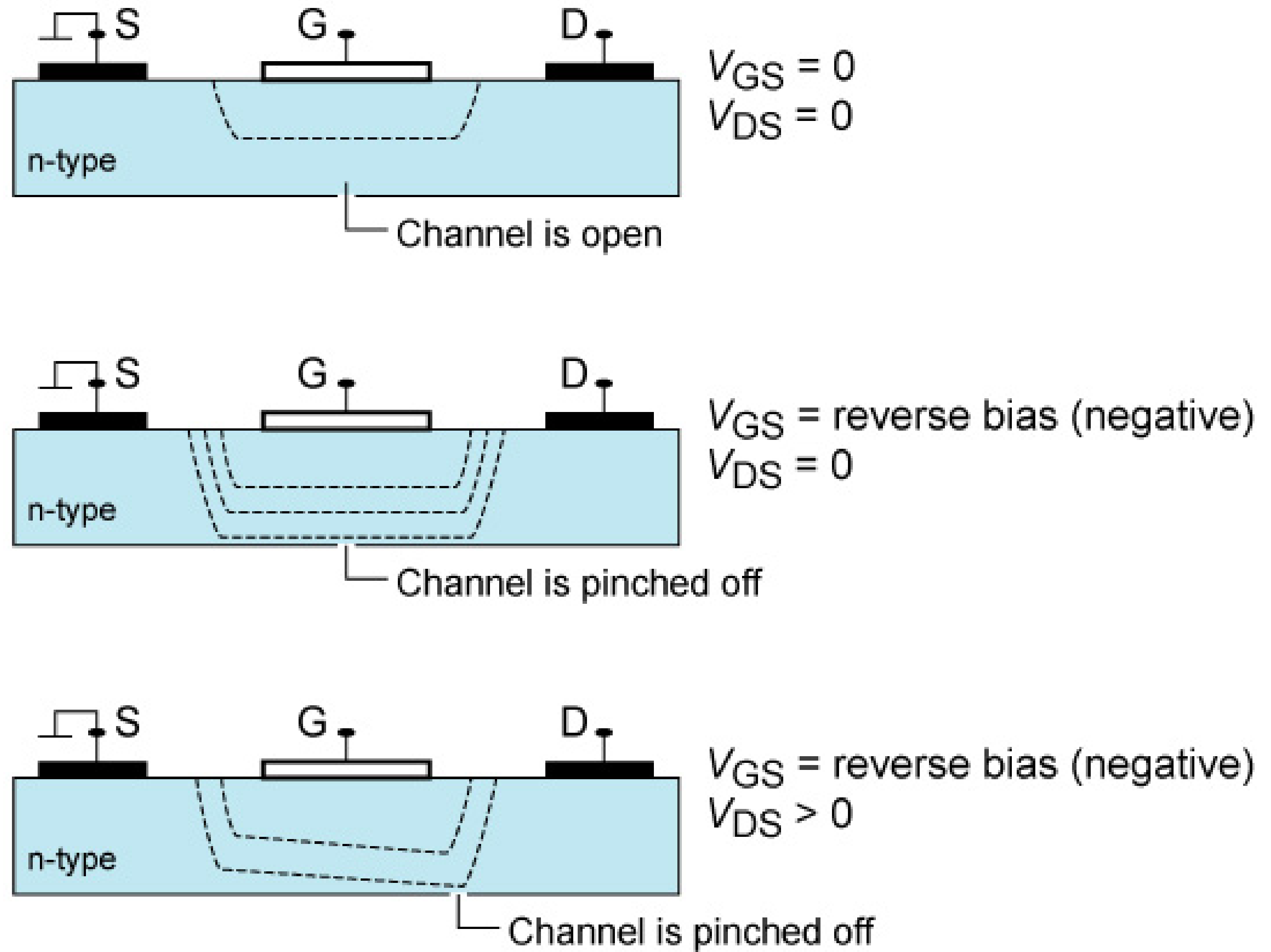
MESFET = Metal-semiconductor FET = Schottky gate FET



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JFET and MESFET follow similar principles

Similarity:

A MESFET can be thought of as a p^+n junction FET with $p^+ \rightarrow \infty$

Differences:

1. JEFT has a higher gate barrier. This is an advantage for low-gap materials (*e. g*. GaInAs). As a result, JFETs have a low gate leakage current

2. MESFET has ohmic contacts only to n-type material. Advantage: Ease of fabrication.

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All discrete JFETs and MESFETs have an n-type channel due to higher electron mobility as compared to hole mobility.

Gate current ≈ 0 for JFET and MESFET ➔ FETs are voltage-controlled devices

Comparison: FET vs. BJT

FET:
Input power = $V_{GS} I_G$ $\quad (I_G = \text{const} \approx 0) \quad (1)$

BJT:
Input power = $V_{EB} I_B$ $\quad (V_{EB} = \text{const} \approx 0.7 \text{ V for Si}) \quad (2)$

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Note: 99 % of all ICs are made of FETs.

MESFET and JFET applications:

High frequency devices, cellular phones, satellite receivers, radar, microwave devices

GaAs is primary material for MESFETs

GaAs has high electron mobility (8000 cm^2 / Vs)

Generally, if f > 2 GHz ➔ GaAs transistors are usually used

f < 2 GHz ➔ Si transistors are usually used

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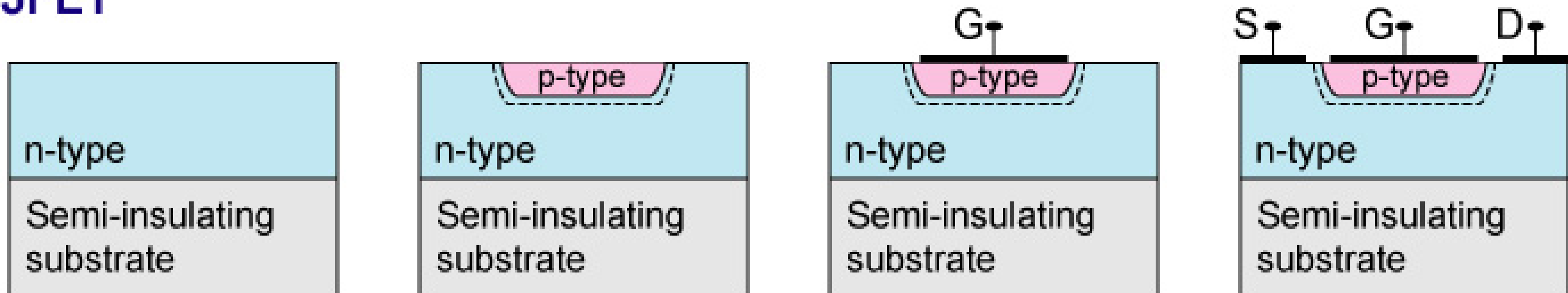
Fabrication

(1) JFET



Typical contact materials for a GaAs JFET:

AuGe for S and D (annealed)

AuZn for G (annealed)

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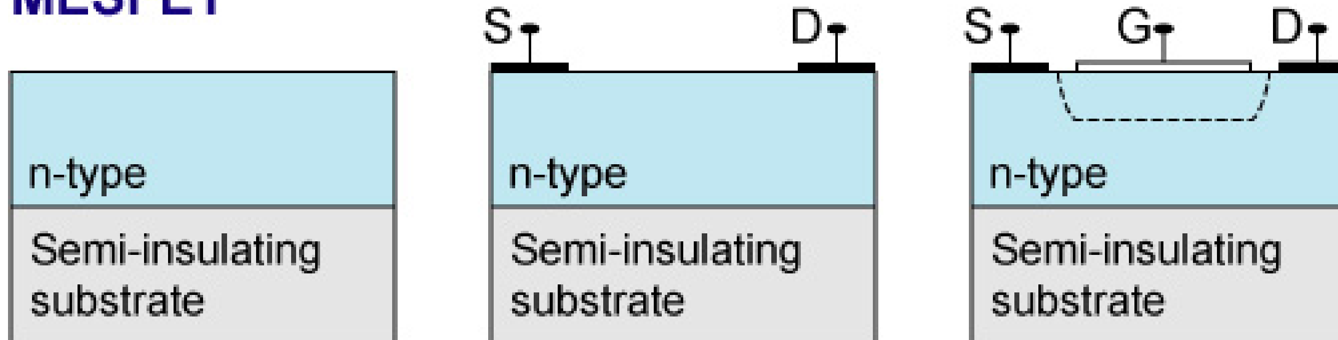
(2) MESFET



Typical contact materials for a GaAs MESFET

Au Ge for S and D (annealed)

Ti for G (not annealed)

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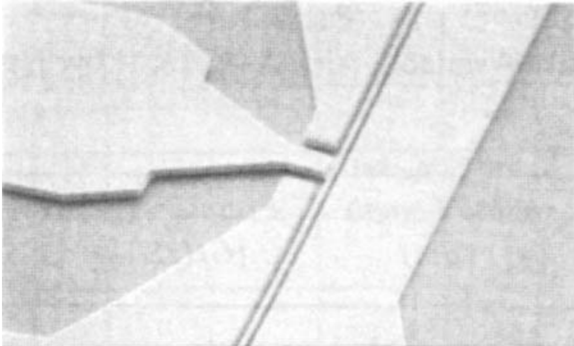
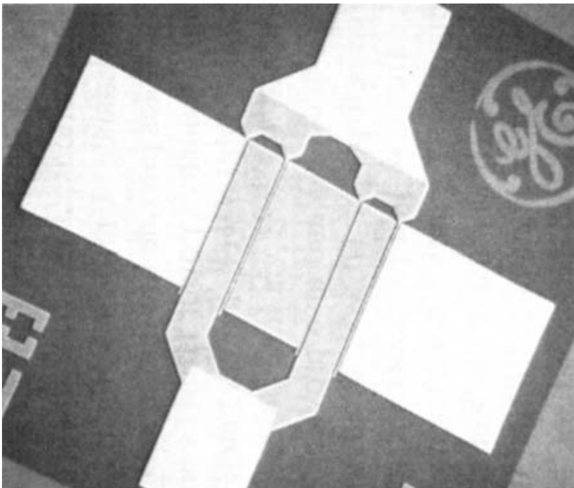
Top view of MESFET using scanning electron microscopy (SEM)



T-gate GaAs MESFET



(after GE Corporation)

High-current transistor: Wide gate

How many gates do the transistors, shown in the pictures, have?

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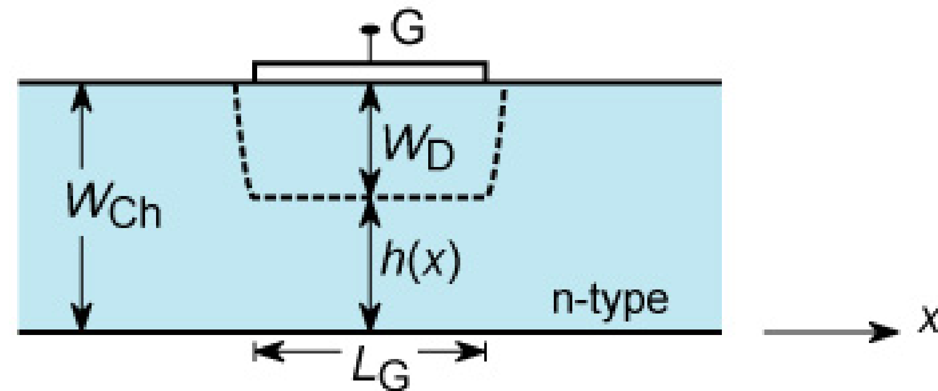
JFET / MESFET operation

Ohmic regime or linear regime

V_{DS} is assumed to be small

$| V_{GS} | > | V_{DS} |$



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Depletion layer thickness

$$W_D = \sqrt{\frac{2\varepsilon}{e\,N_D}\left(\Phi_B - V_{GS}\right)} \approx \sqrt{\frac{2\varepsilon}{e\,N_D}\left(-V_{GS}\right)} \qquad (3)$$

Channel height $h(x)$

Pinch off condition $h(x) = 0$ or $W_D = W_{ch}$

Pinch-off voltage

$$V_{PO} = \frac{e\,N_D}{2\,\varepsilon}\,W_{ch}{}^2 \qquad (4)$$

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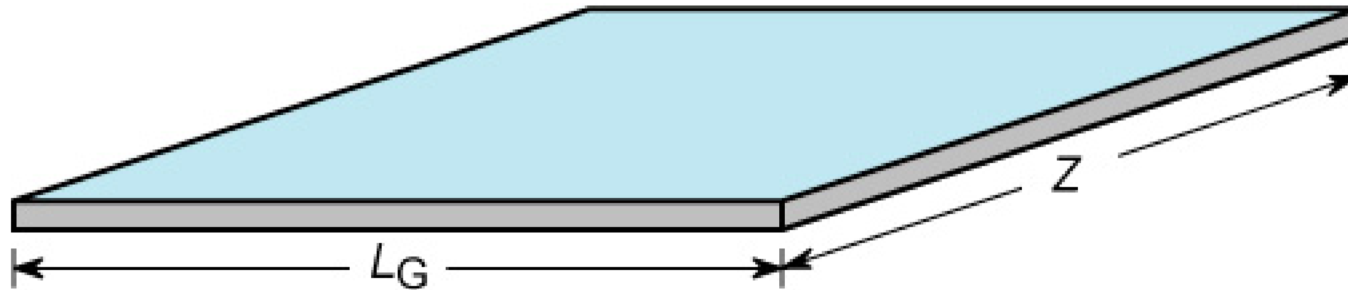
Next we calculate the resistance of the conductive channel.



Gate length = L_G

Gate width = Z

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Resistance of channel

$$R = \rho \frac{L_G}{A} = \rho \frac{L_G}{Z\, h(x)} = \frac{1}{e n \mu} \frac{L_G}{Z\left(W_{ch} - W_D\right)}$$

$$R = \frac{1}{e n \mu} \frac{L_G}{Z\left(W_{ch} - \sqrt{\frac{2\varepsilon}{e N_D}\left(-V_{GS}\right)}\right)} \qquad (5)$$

Resistance can be controlled by gate voltage

At $V_{GS} = - V_{PO}$ ➔ $R \rightarrow \infty$

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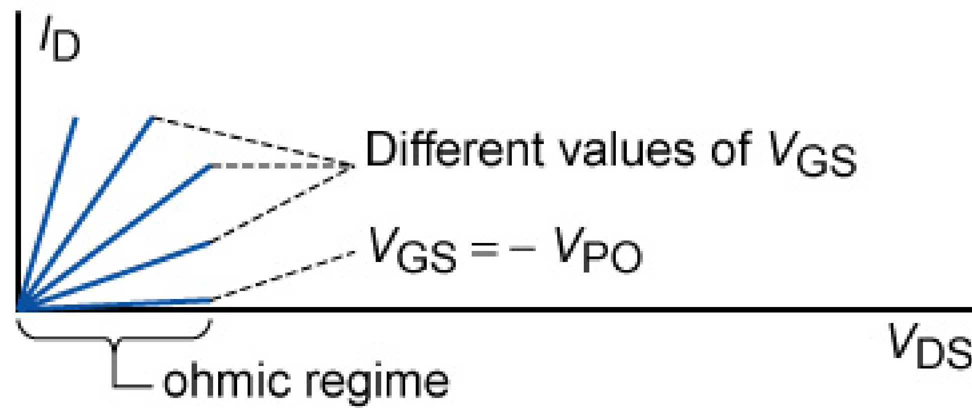

In the **ohmic regime**, the FET behaves like a variable resistor controlled by the gate voltage.

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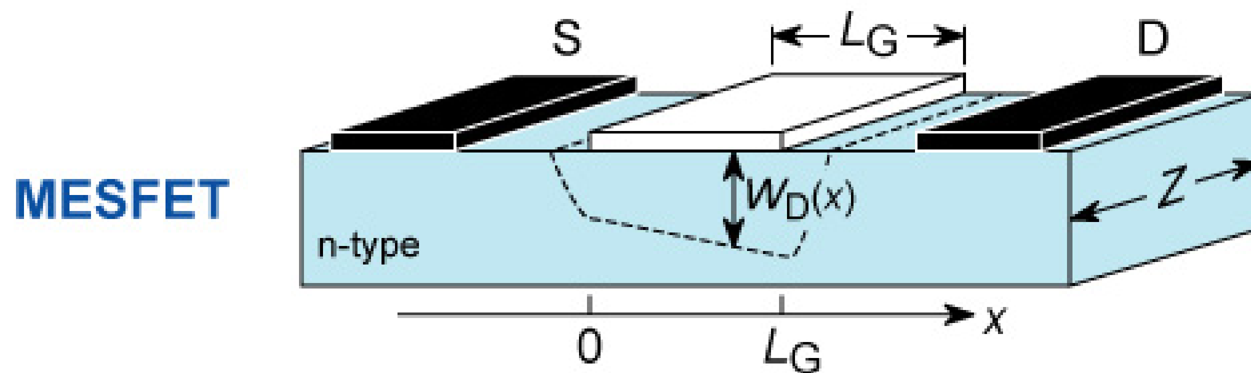
Gradual channel approximation

This model was developed by William Shockley



Depletion width

$$W_D(x) = \sqrt{\frac{2\varepsilon}{e N_D}\left(-V_{G\,x}\right)} = \sqrt{\frac{2\varepsilon}{e N_D}\left[V(x) - V_{GS}\right]} \qquad (6)$$

$V(x)$ = Voltage in the channel along the x direction

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$$\int_0^{L_G} V(x)\,dx = V_{DS} \tag{7}$$

Drain current I_D is the same for all values of x. These are fewer carriers at the drain end of the channel than at the source end. Carriers must drift faster at the drain end since I_D = const.

Electron velocity in channel

$$v = -\mu\,\mathcal{E}(x) = \mu \frac{dV(x)}{dx} \tag{8}$$

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Gradual channel model means:

Gradual change of W_D(x)

Gradual change of $V(x)$

Gradual chance of $v(x)$

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Drain current

$$I_D = -e\,n\,v\,h(x)\,Z \qquad (9)$$

Using

(1) $h(x) = W_{ch} - W_D(x)$,

(2) Eq. (6) for $W_D(x)$,

(3) Eq. (8) for v,

one obtains

$$I_D = -e\,n\,\mu\,\frac{dV(x)}{dx}\left(W_{ch} - \sqrt{\frac{2\varepsilon}{e\,N_D}\left(V(x) - V_{GS}\right)}\right) Z \qquad (10)$$

Using Eq. (4) to eliminate $2\varepsilon / \left(eN_D\right)$, one obtains

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$$-I_D \, dx = e n \mu Z W_{ch} \left[1 - \left(\frac{V(x) - V_{GS}}{V_{PO}} \right)^{1/2} \right] dV(x) \tag{11}$$

… differential equation

… left-hand side: dx

… right-hand side: $V(x)$ and d$V(x)$

… integration of both sides of equation

(LHS) x from 0 to L_G

(RHS) $V(x)$ from 0 to V_{DS}

yields:

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$$-I_{\mathrm{D}} = en\mu \frac{W_{\mathrm{ch}} Z}{L_{\mathrm{G}}} V_{\mathrm{PO}} \left[\frac{V_{\mathrm{DS}}}{V_{\mathrm{PO}}} + \frac{2}{3} \left(-\frac{V_{\mathrm{GS}}}{V_{\mathrm{PO}}} \right)^{\frac{3}{2}} - \frac{2}{3} \left(\frac{V_{\mathrm{DS}} - V_{\mathrm{GS}}}{V_{\mathrm{PO}}} \right)^{\frac{3}{2}} \right] \qquad (12)$$

- **Exercise**: Show that Eq. (12) is derived from Eq. (11) by integration.
- Note that current I_{D} is negative since it flows in negative x direction. Electrons drift from S to D. Current flows from D to S.
- For very small values of V_{DS}, the second and third term in the bracket cancel. Then, it is $I_{\mathrm{D}} \propto V_{\mathrm{DS}}$. This is again the ohmic regime.
- For larger values of V_{DS}, the slope of I_{D} - vs. - V_{DS} becomes smaller.
- At some point, for even larger values of V_{DS}, pinch-off of the channel will occur at the drain end of the channel.

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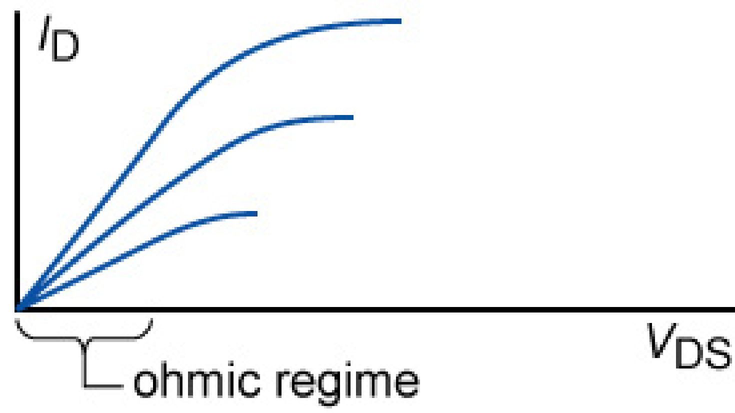

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Gate-to-channel voltage $x = 0$: $V_{Gx}(x=0) = -V_{GS}$

Gate-to-channel voltage at x: $V_{Gx}(x) = V(x) - V_{GS}$

Gate-to-channel voltage at $x = L_G$: $V_{Gx}(x=L_G) = V_{DS} - V_{GS}$

Pinch-off at the drain end of the channel:

$$V_{Gx}(x=L_G) = V_{PO} = V_{DS} - V_{GS} \qquad (13)$$

At pinch-off, $I_D = I_{D,\,sat}$ = saturation current

$I_{D,\,sat}$ is independent of V_{DS}

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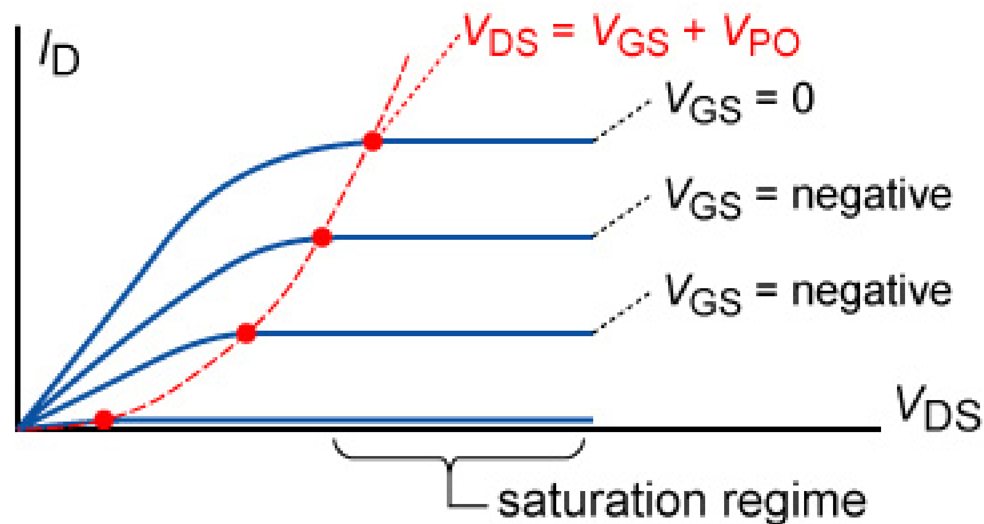
Elimination of V_{DS} from Eq. (12) by using Eq. (13) yields:

$$I_{D,\,sat} = e n \mu \frac{W_{ch} Z}{L_G} V_{PO} \left[\frac{V_{PO} + V_{GS}}{V_{PO}} + \frac{2}{3} \left(- \frac{V_{GS}}{V_{PO}} \right)^{3/2} - \frac{2}{3} \right]$$

$$I_{D,\,sat} = e n \mu \frac{W_{ch} Z}{L_G} V_{PO} \left[\frac{V_{GS}}{V_{PO}} + \frac{2}{3} \left(- \frac{V_{GS}}{V_{PO}} \right)^{3/2} + \frac{1}{3} \right] \quad (14)$$



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Amplification of an FET

Amplification = g_m = dI_D / dV_{GS}

The dimension of the amplification:

Dimension {amplification} = Ω^{-1} = Dimension {conductance}

Amplification = Transconductance

$$g_m = \frac{dI_{D,\,sat}}{dV_{GS}} = en\mu \frac{W_{ch} Z}{L_G} \left[1 - \left(- \frac{V_{GS}}{V_{PO}} \right)^{1/2} \right] \qquad (15)$$

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Inspection of the equation reveals:

… highest transconductance at $V_{GS} = 0$

… for high transconductance design:

- ➔ High mobility μ
- ➔ High concentration n
- ➔ Short gate length L_G

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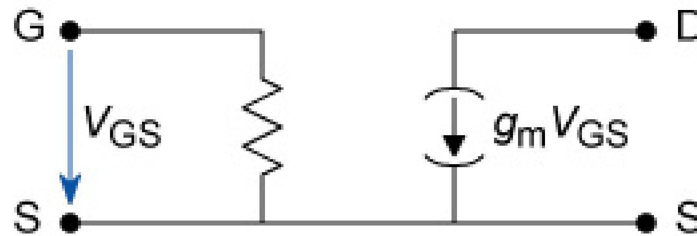
Equivalent circuit (in saturation regime)



- This is the simplest possible equivalent circuit diagram
- Input resistance is very high (frequently assumed to be ∞)
- FET = voltage-controlled current source

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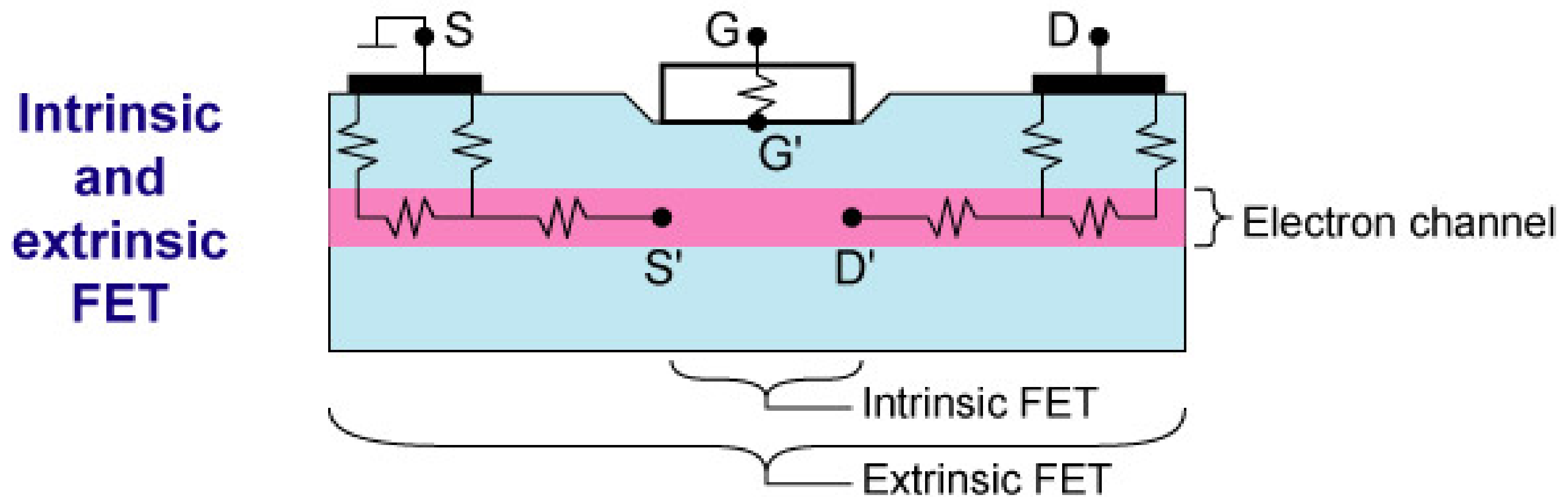
Intrinsic and extrinsic FET



- Extrinsic FET (real FET) has terminals S, G, and D.
- Intrinsic FET has terminals S', G', and D'.
- Intrinsic FET = inner FET = ideal FET
- Intrinsic FET + Parasitics = Extrinsic FET

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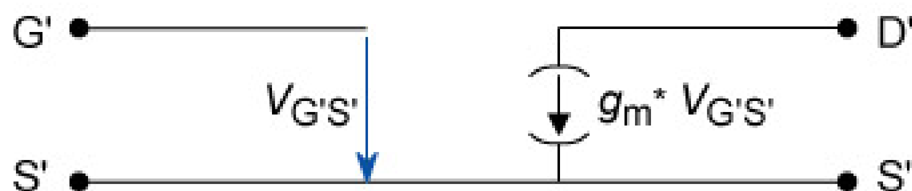
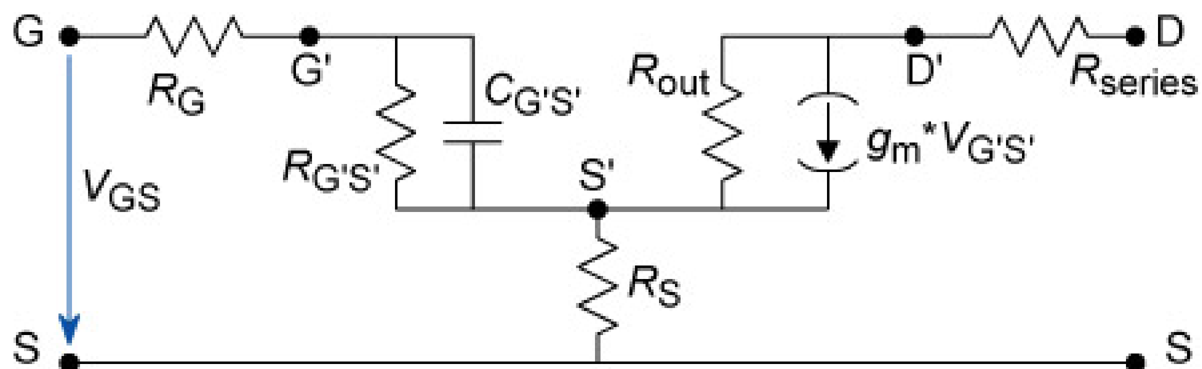
Equivalent circuit of intrinsic and extrinsic FET:

Intrinsic FET



Extrinsic FET



- R_G is very small because the gate is a metal
- $R_{G'S'}$ is very large because of the gate insulator
- R_{out} represents a possible current path through the substrate. R_{out} is very large

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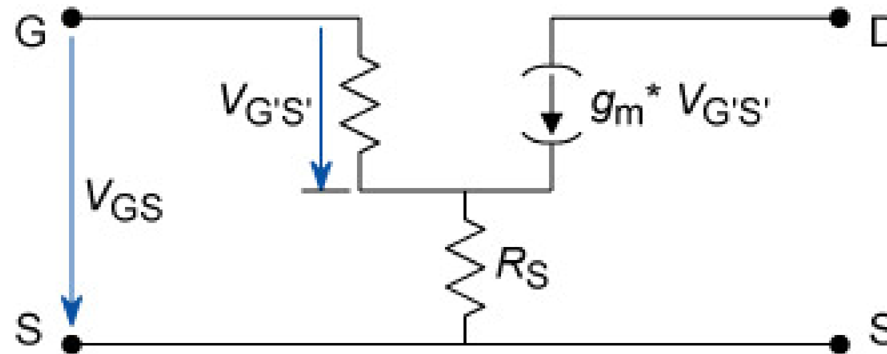
Extrinsic and intrinsic transconductance



- R_S = source resistance
- Voltage drop across source resistance = $R_S\ g_m^*\ V_{GS}^*$
- Intrinsic transconductance: $$g_m^* = \frac{dI_D}{dV_{G'S'}}$$
- Extrinsic transconductance: $$g_m = \frac{dI_D}{dV_{GS}}$$

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Exercise:

Calculate the transconductance (g_m) of a transistor as a function of g_m^* for a transistor with $R_G = 0$, $R_{S'G'} = \infty$, and $R_{out} = \infty$.

Solution:

$$g_m = \left(\frac{1}{g_m^*} + R_S \right)^{-1}$$

It follows from this equation that the source resistance decreases the transconductance. It also follows from this equation that the source resistance must be minimized in order to maximize the extrinsic (external) transconductance of the FET.

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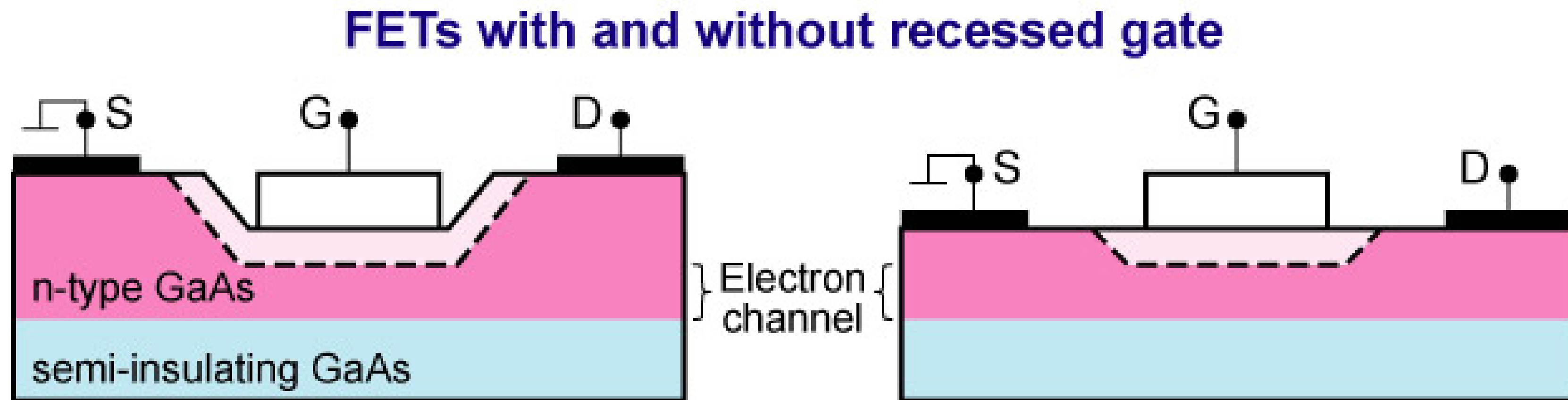
Recessed gate FET structures



- Left-hand-side figure: Recessed gate FET structure
- Right-hand-side figure: Planar FET structure
- Recessed gate helps to reduce access resistances to intrinsic FET
- Recessed gate structure reduces difference between extrinsic and intrinsic FET
- Additional etching step required

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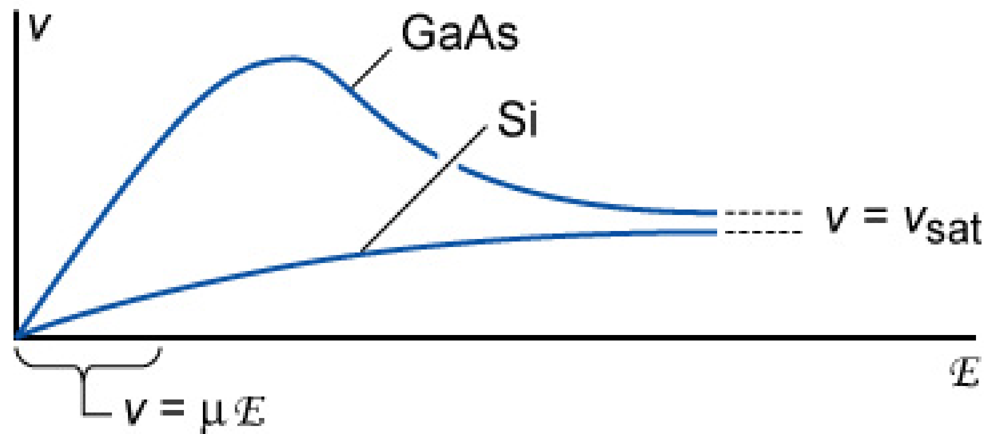
Drift velocity in short-channel FETs

Gradual channel approximation breaks down in FETs with a very short gate length.

Velocity - versus - field characteristic:



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For short gate lengths:

$\mathcal{E}$ is very high ($\mathcal{E}$ along the channel)

$$v = v_{sat} \qquad (v \neq \mu \mathcal{E})$$

Gradual channel model is not valid for very short gate lengths

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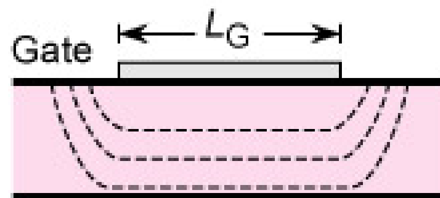
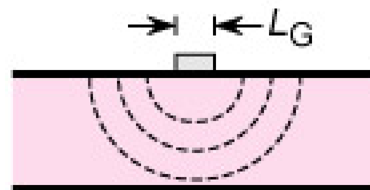
Short-channel effects

At short channel lengths, the planar-capacitor geometry is lost.





Short-channel effects:

Threshold-voltage shift

Lack of pinch-off

Increased leakage current

Increase of output conductance

Why is there a lack of pinch-off at short gate lengths?

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Mitigation of short-channel effects: Scaling of “vertical” dimensions!

Channel depth must be decreased.

➔ Doping concentration must be increased

➔ Fields increase

➔ Gate voltage must be decreased

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Appendix: Fabrication Steps of a GaAs MESFET

Mesa definition (Device isolation)

1. Cleaning of wafer (optional)
2. Deposit and spin photoresist (5000 rpm, 30 s)
3. Pre-bake photoresist (90 °C, 20 min.)
4. Expose with mesa mask (10 sec)
5. Post-bake (120 °C, 20 min.)
6. Measure thickness of photoresist
7. Etch sample. Typical solution is H_3PO_4 + H_2O_2 + H_2O. Typical mesa height is 2500 Å
8. Measure mesa height with surface profilometer
9. Repeat Steps 7 and 8 until desired mesa height is reached
10. Dissolve photoresist in acetone
11. Clean wafer in methanol

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Ohmic contact definition

1. Cleaning of wafer (optional)
2. Deposit and spin photoresist (5000 rpm, 30 s)
3. Pre-bake photoresist (90 °C, 20 min.)
4. Expose with ohmic contact mask (10 sec)
5. Post-bake (120 °C, 20 min.)
6. Deposit ohmic contacts by thermal evaporation. A typical metal layer sequence: AuGe (1000 Å) + Ni (200 Å) + Au (1000 Å)
7. Lift-off of unwanted ohmic contact metal by dissolving the photoresist in acetone. Use ultrasonic bath if necessary
8. Clean wafer in methanol
9. Anneal contact. Typical temperature and time are 410 °C for 25 s
10. Measure drain-source current-voltage characteristic and contact resistance

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Gate recess etching and gate deposition

1. Cleaning of wafer (optional)
2. Deposit and spin photoresist (5000 rpm, 30 s)
3. Pre-bake photoresist (90 °C, 20 min.)
4. Expose with gate mask (10 sec)
5. Post-bake (120 °C, 20 min.)
6. Etch gate recess using strongly diluted $H_3PO_4 + H_2O_2 + H_2O$
7. Measure current between source and drain
8. Repeat Steps 6 and 7 until desired source-drain current is reached
9. Deposit gate metal. Typical metallization: Ti (500 Å) + Au (1000 Å)
10. Lift-off of unwanted gate metal by dissolving the photoresist in acetone. Use ultrasonic bath if necessary
11. Clean wafer in methanol
12. Measure gate-source current-voltage characteristic and leakage current

On-wafer measurement of device characteristics
Scribing and cleaving
Packaging
Testing of packaged devices

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