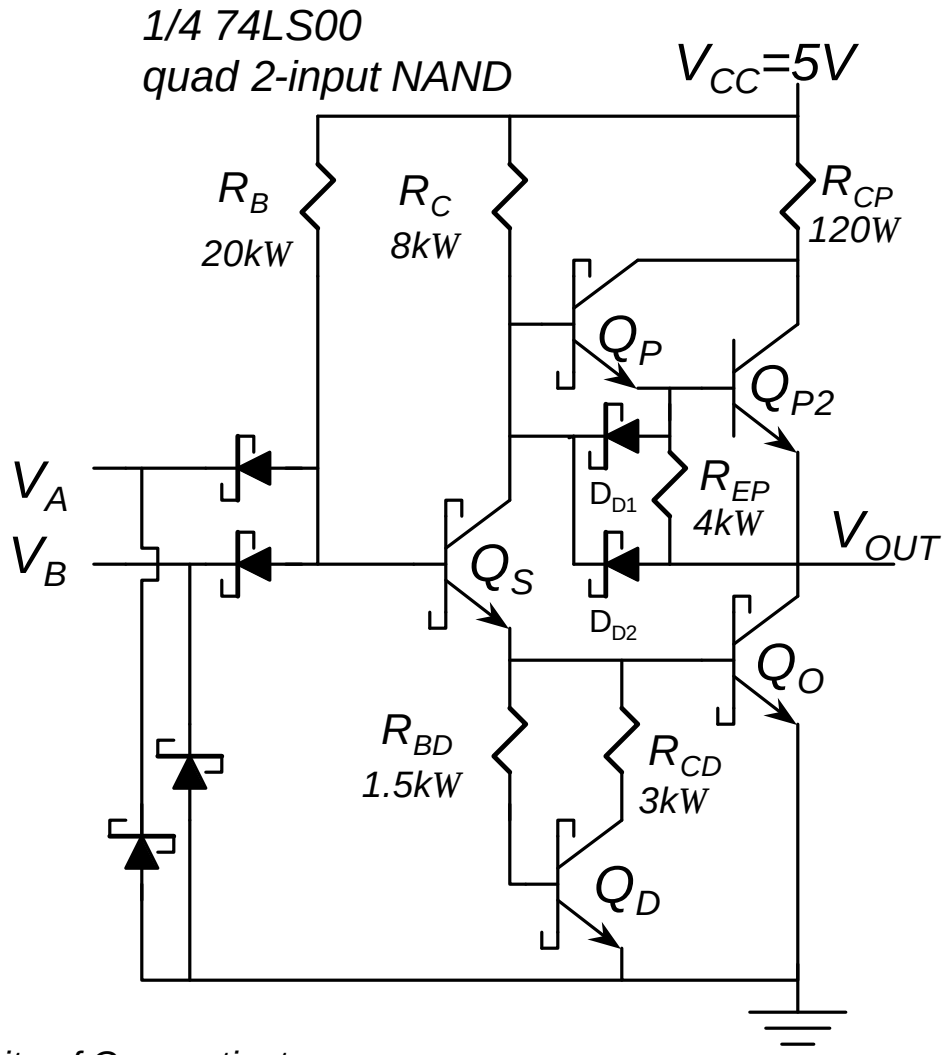
Low-Power Schottky TTL (74LS)

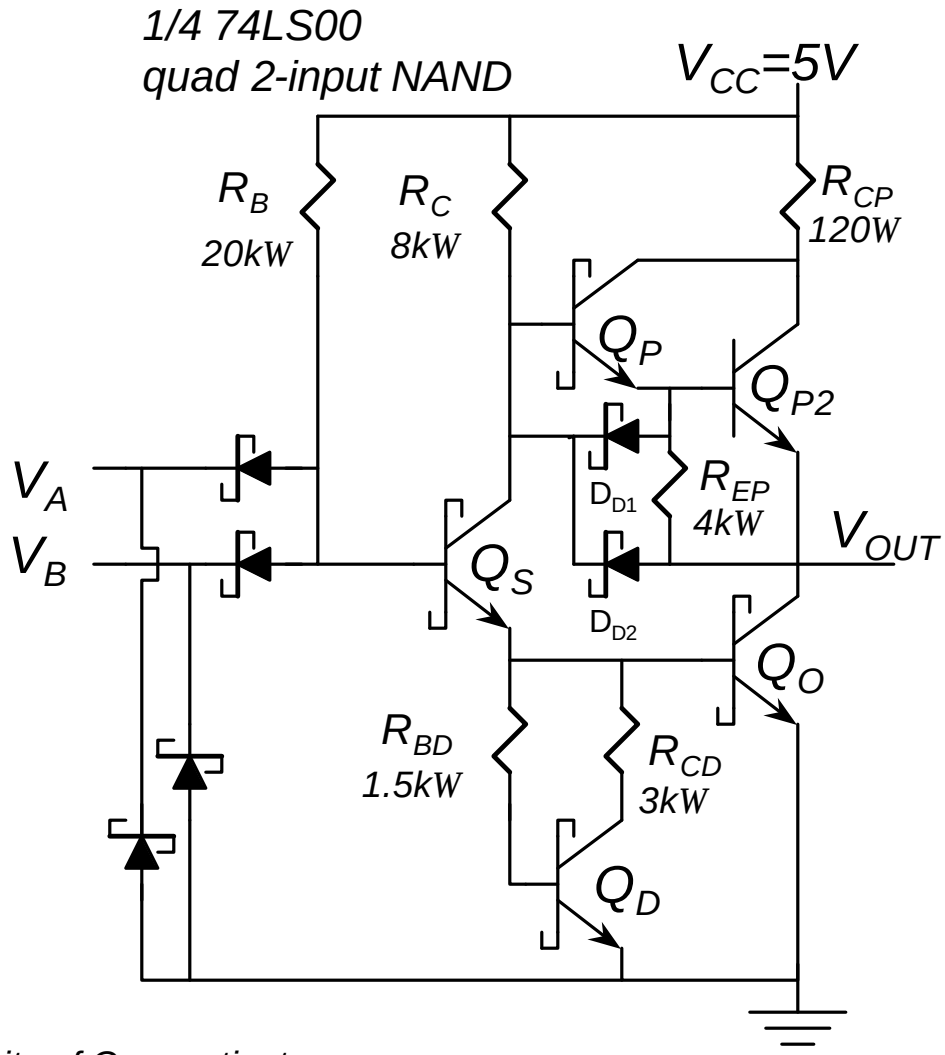


- *Vintage 1975*
- *Scaled Resistors*
- *DTL input*

Why did we go back to DTL?

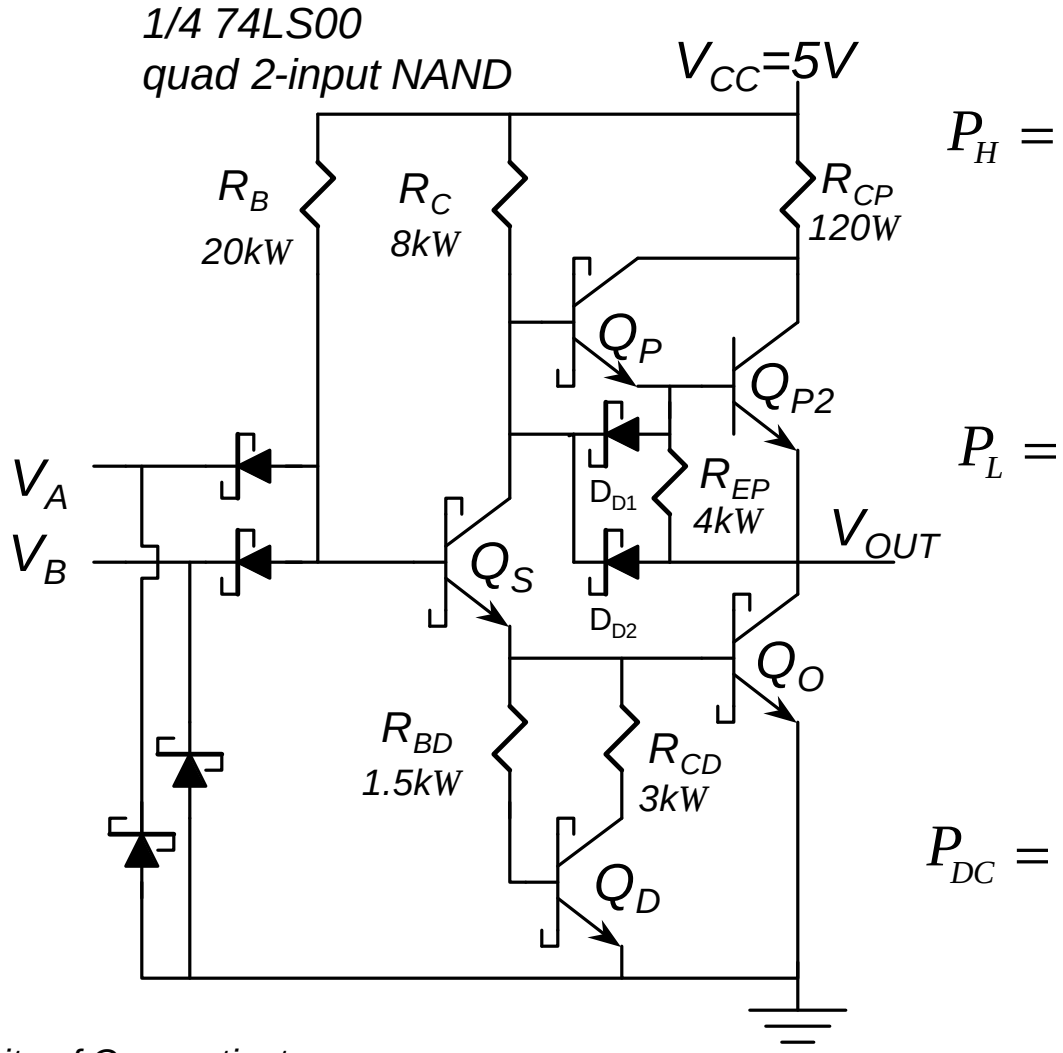
- *The Schottky diodes can be made smaller than Q_I, with lower parasitic capacitances, with post 1975 technology (6mm features).*
- *Q_S can not saturate, so it is not neccessary to remove its base charge with a BJT.*

74LS Circuit Design



- *R_B and R_C. Dominant in determining dissipation, these were scaled up by a factor of 8.*
- *R_{BD} and R_{CD}. These were scaled up with R_B and R_C to maintain reasonable fanout.*
- *R_{CP} and R_{EP}. These affect speed, not power. They were not scaled significantly from 74S.*
- *D_{D1} and D_{D2}. D_{D1} speeds the turn off of Q_{P2}. D_{D2} sinks current from the load. Both improve t_{PHL}.*

74LS DC Dissipation

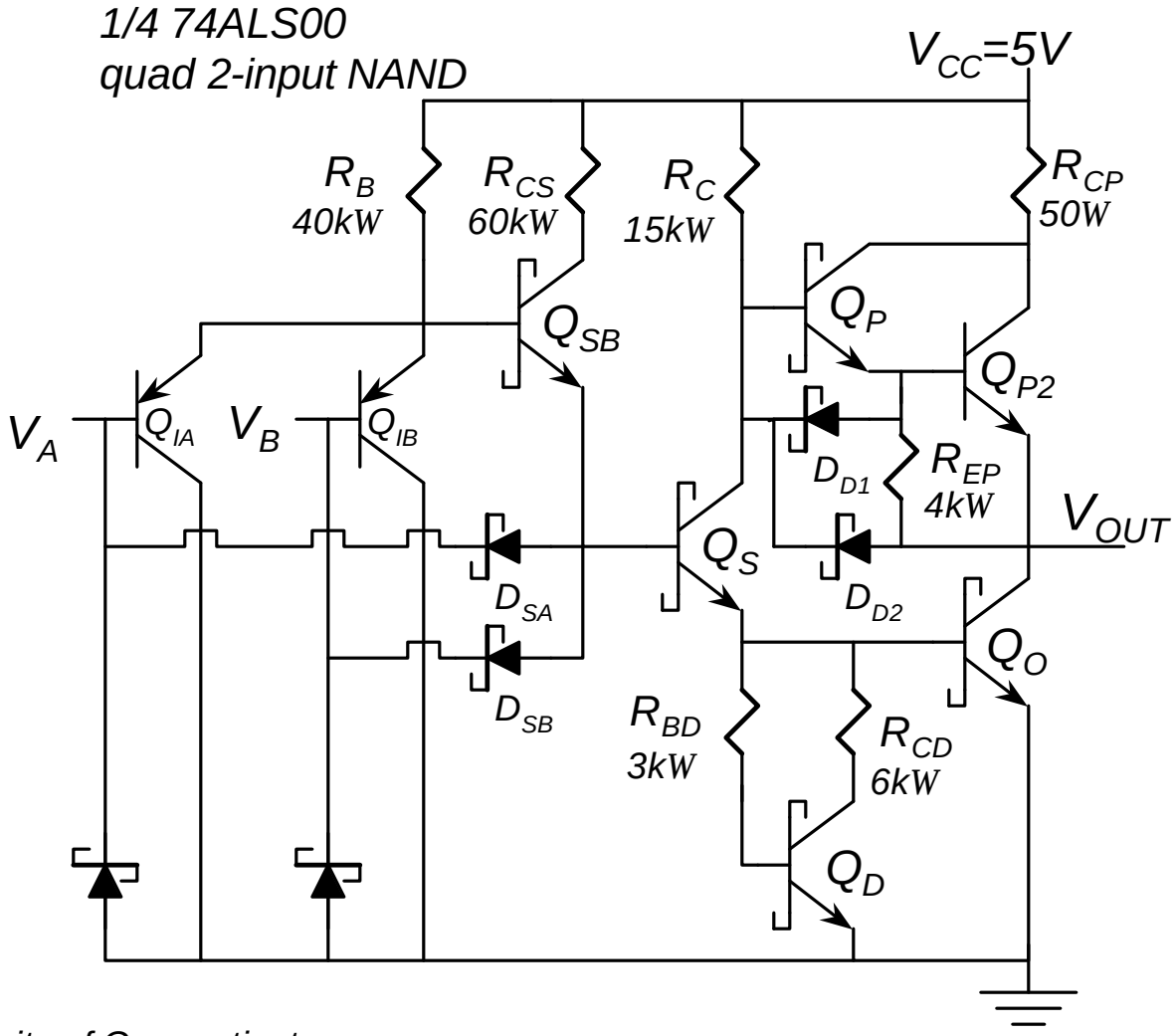


$P_H =$

$P_L =$

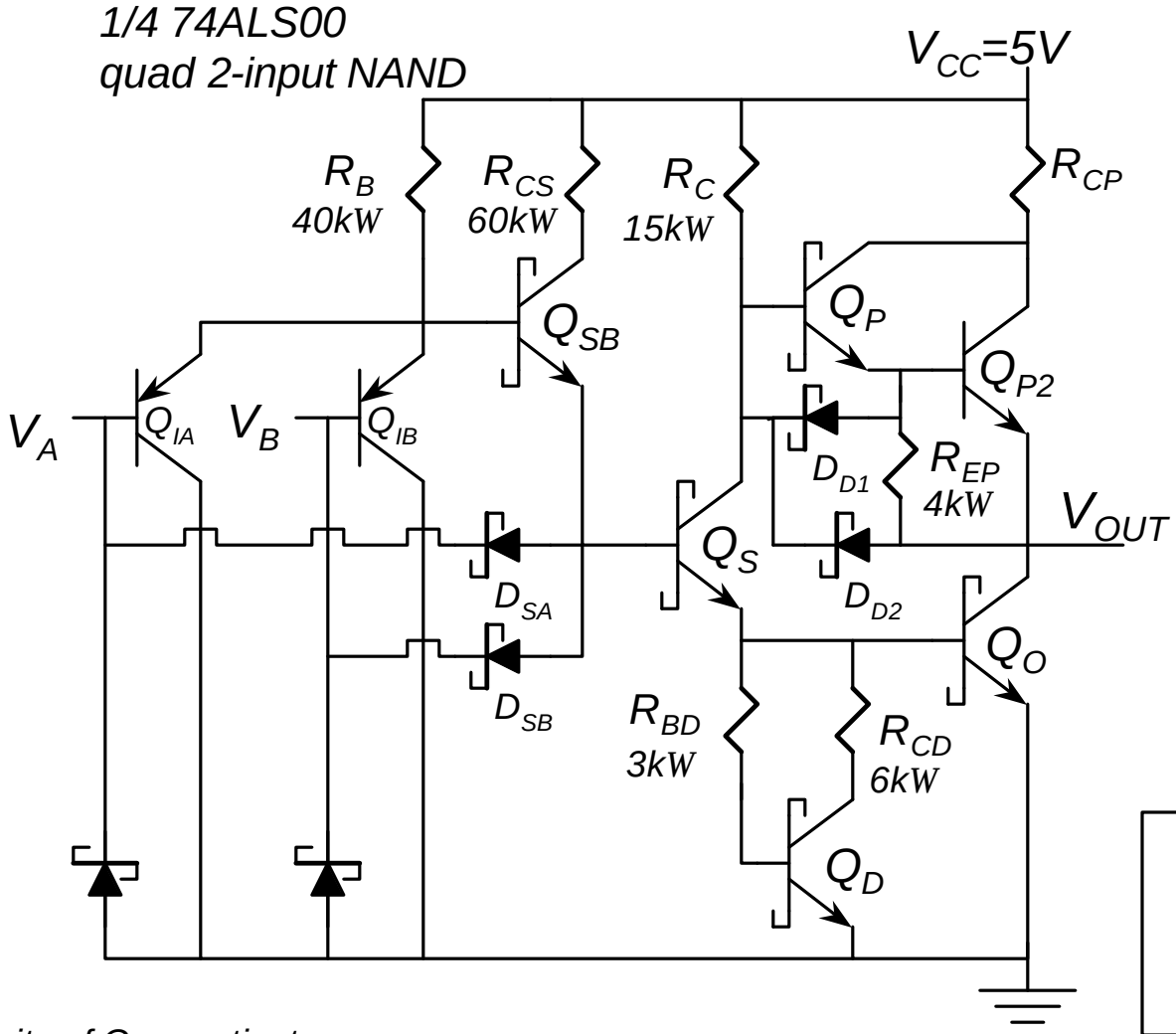
$P_{DC} =$

Advanced Low-Power Schottky TTL (74ALS / 54ALS Series)



- *T.I., circa 1985*
- *Derived from 74LS, but scaled-up resistors further decrease dissipation*
- *Improved transistor fabrication (3mm oxide-isolated transistors, vs. 6mm junction-isolated BJT's for 74LS)*
- *Novel input circuitry also improves performance, but requires the use of lateral PNP's.*

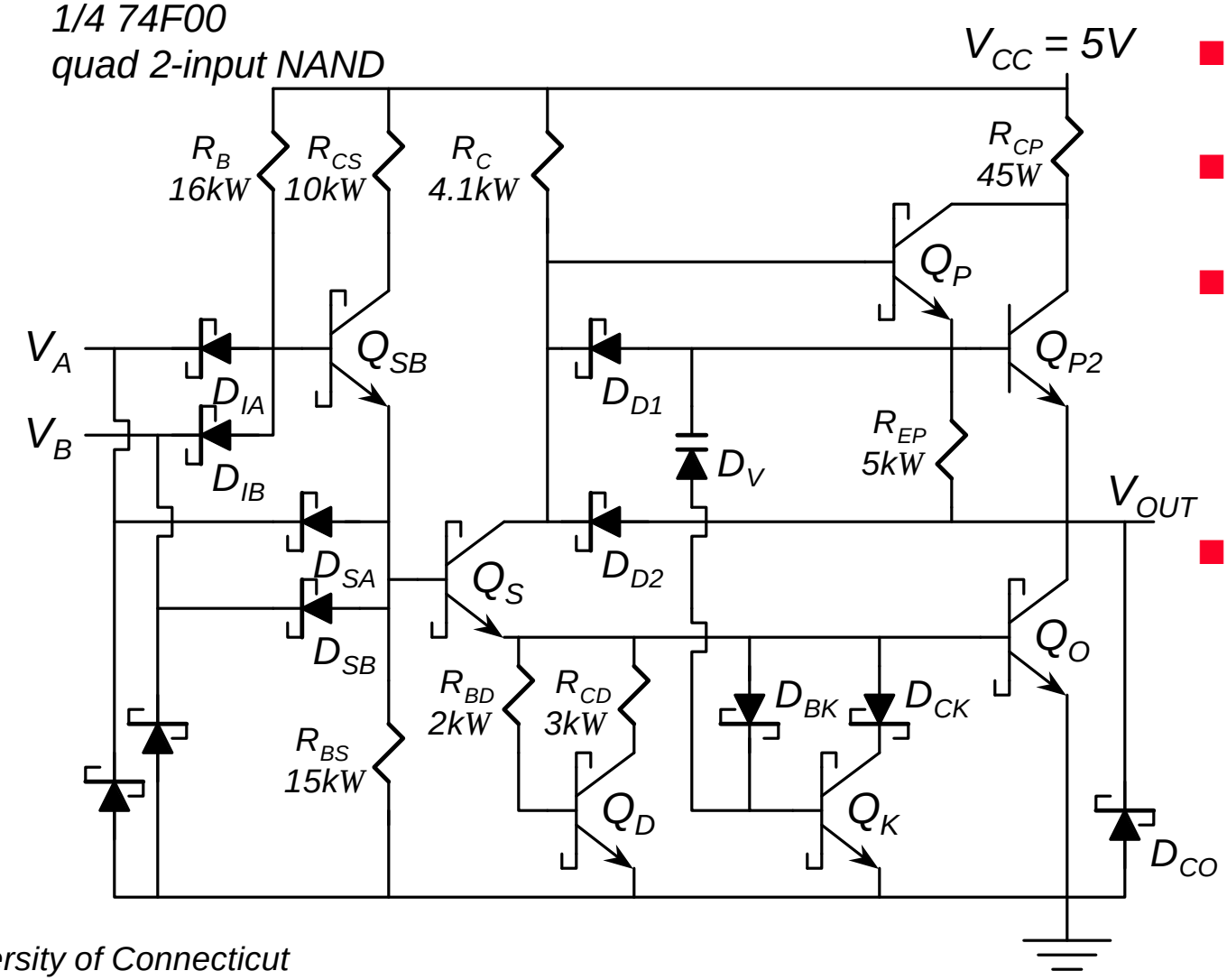
74ALS Circuit Design



- Q_{SB} *increases base drive for* Q_S*, and improves* t_{PHL}.
- *The input emitter followers compensate for the voltage shift of* Q_{SB}.
- *An added benefit is reduced* I_{IL}*, and improved fanout.*
- D_{SA} *and* D_{SB} *remove base charge from* Q_S*, improving* t_{PLH}.

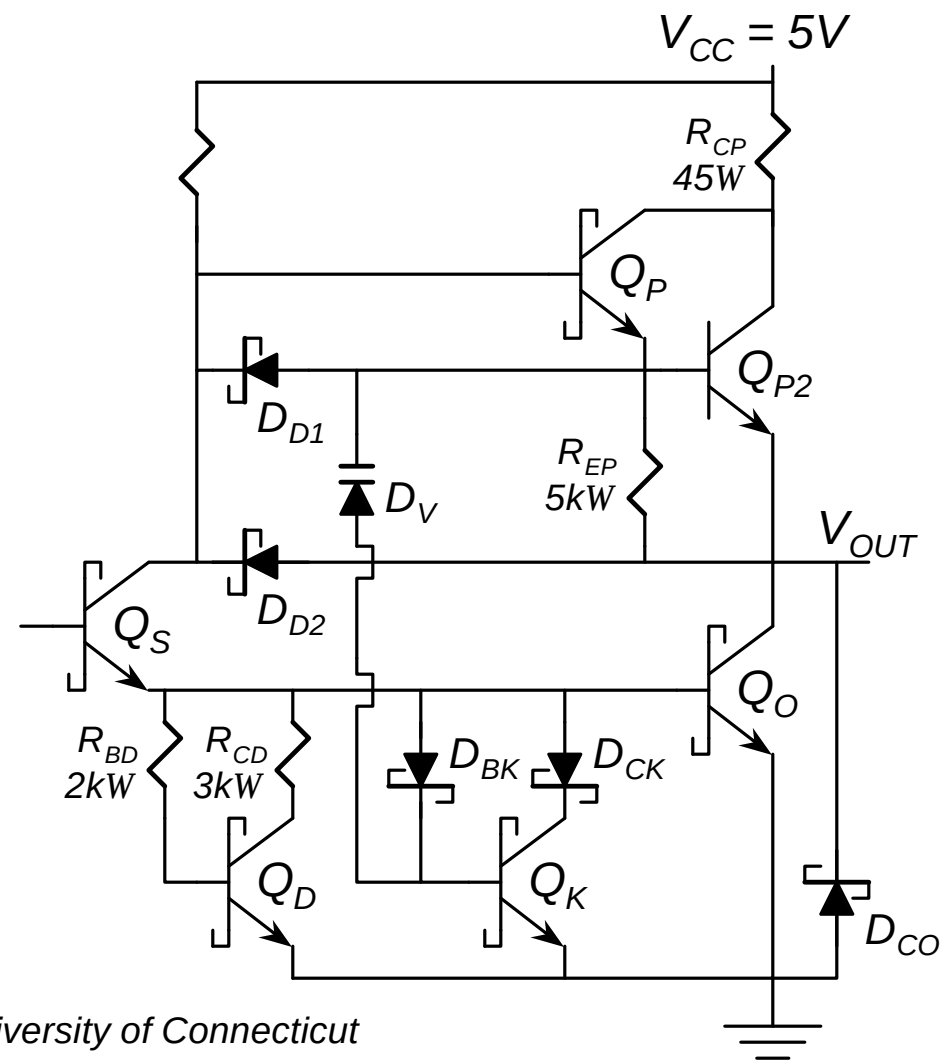
t_P	4ns (15pF)
P	1mW
PDP	4pJ

Fairchild Advanced Schottky TTL (74F /54F Series, a.k.a. FAST)



- *1985, Fairchild Semiconductor*
- *Improved BJT fabrication*
- *DTL input with emitter follower provides good base drive to Q_S.*
- *"Miller killer" greatly improves switching performance*

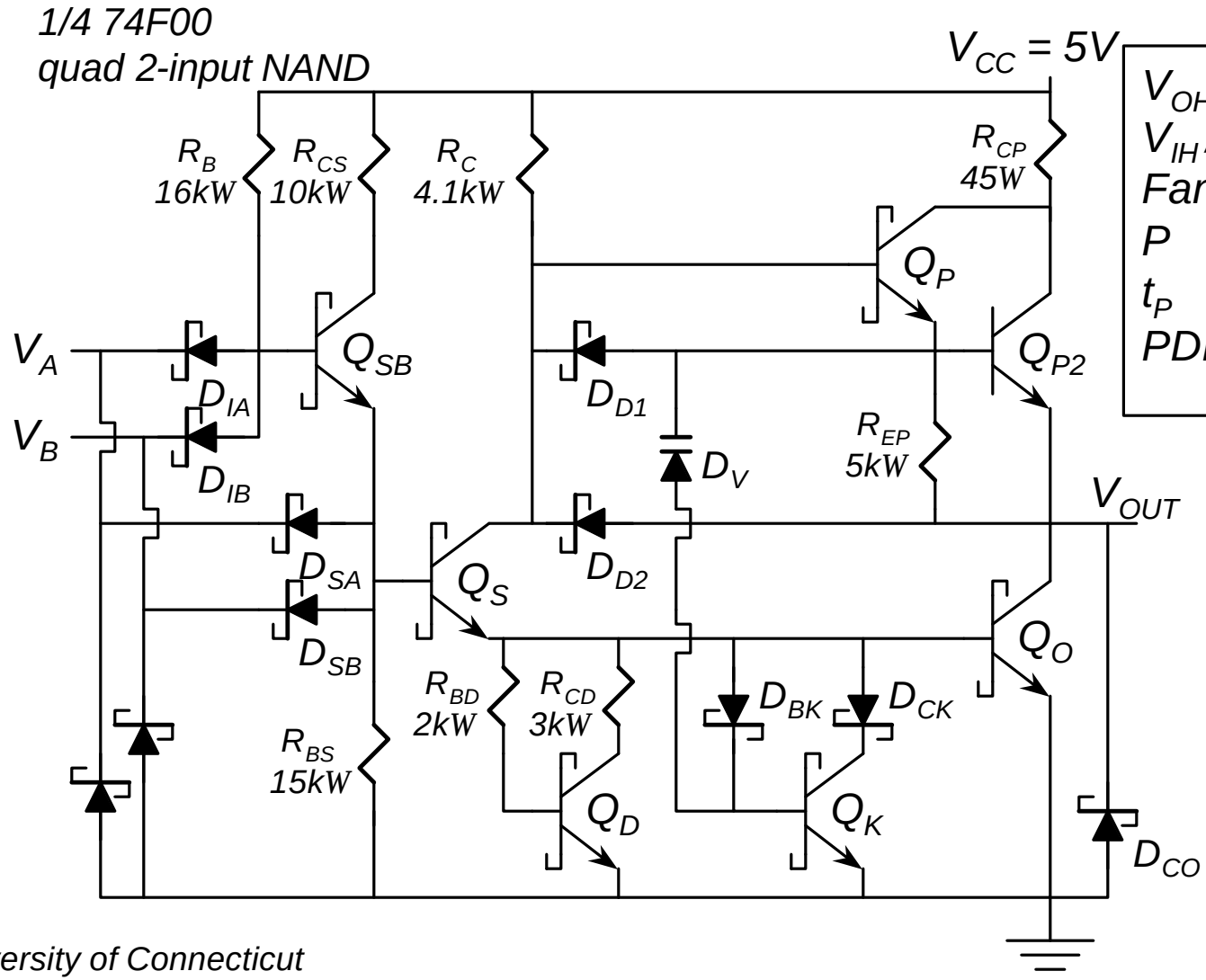
74F /54F "Miller killer"



The "Miller killer" circuit speeds up the low-to-high transition:

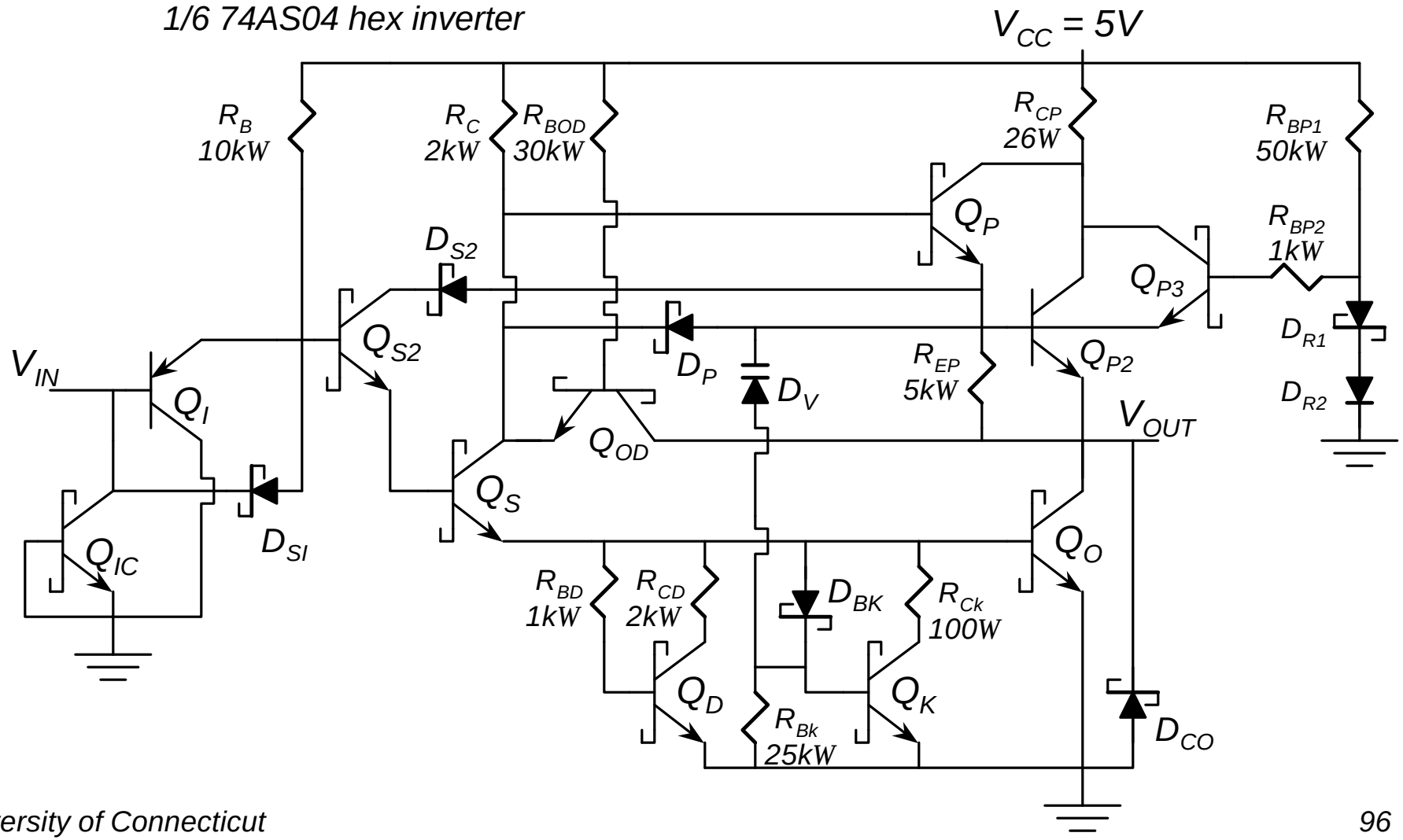
- *On a low-to-high transition, the voltage at the emitter of Q_P begins to increase while Q_O is still on.*
- *The varactor diode D_V conducts, supplying base current to Q_K. ("K" for "killer")*
- *Q_K turns on, and rapidly dissipates the charge stored in the base-collector capacitance of Q_O.*
- *Dynamic power dissipation is reduced by minimizing simultaneous conduction of the pullup and output transistors.*

74F /54F Electrical Characteristics



V_{OH} / V_{OL}	4.3 / 0.5V
V_{IH} / V_{IL}	2.1 / 1.8V
Fanout	10
P	4mW
t_P	2.5 ns (15pF)
PDP	10 pJ

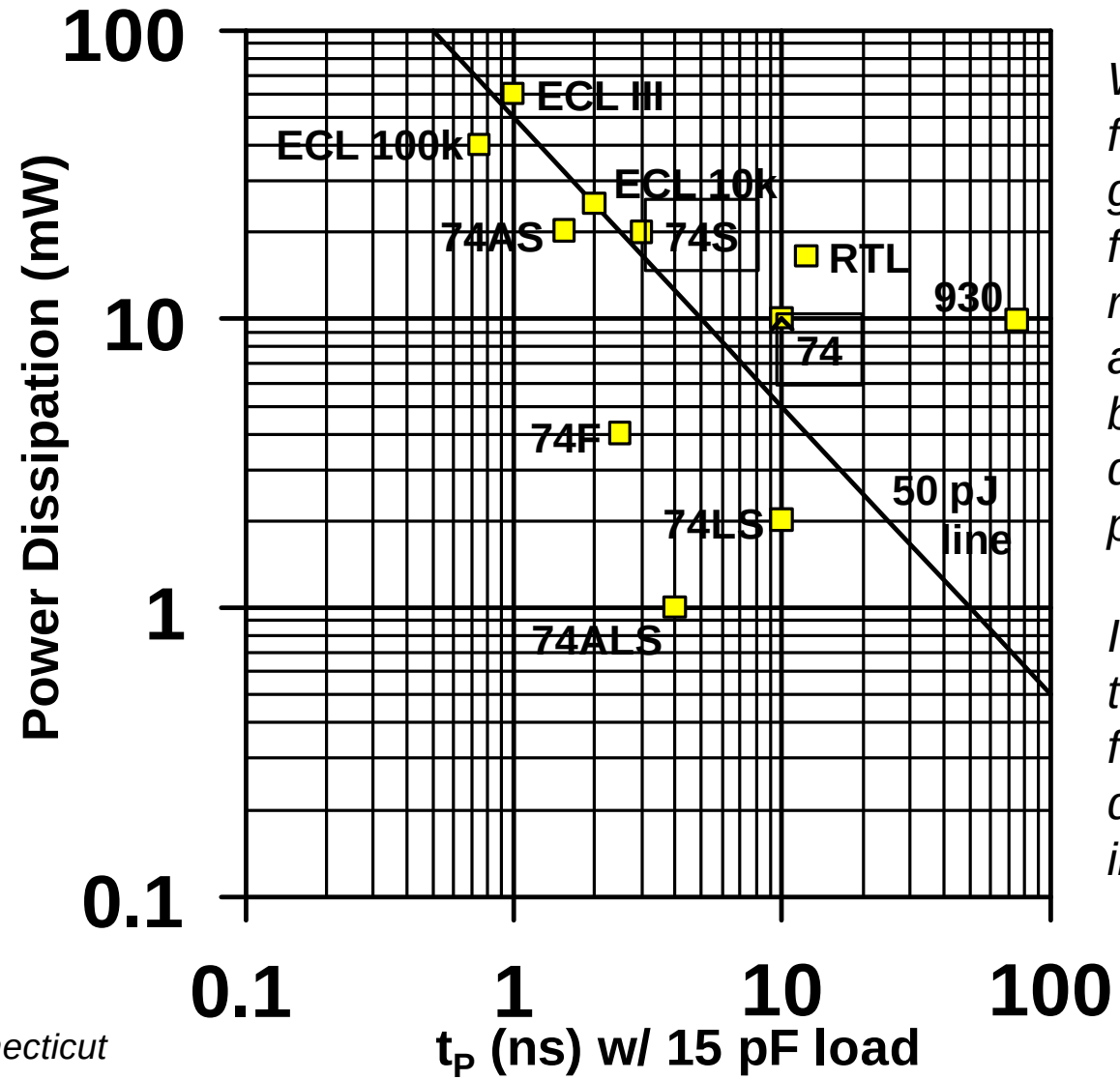
Advanced Schottky TTL (74AS /54AS Series)



74AS / 54AS Circuit Design

- *Texas Instruments, circa 1985, derivative of 74LS series*
- *Input Transistor. Uses a PNP emitter follower like 74ALS. This lowers I_{IL} and improves the fanout.*
- *Input Clamping. Q_{IC} replaces the input clamp diode used in other designs.*
- *Miller killer. The Miller killer is similar in design and operation to the subcircuit used in the 74F series.*
- *Pullup . Q_{P3} increases the base drive for Q_{P2} and also provides extra current to D_V in the "Miller killer."*
- *D_P and D_{S2} help to discharge the base of Q_{P2} during a high-to-low transition.*

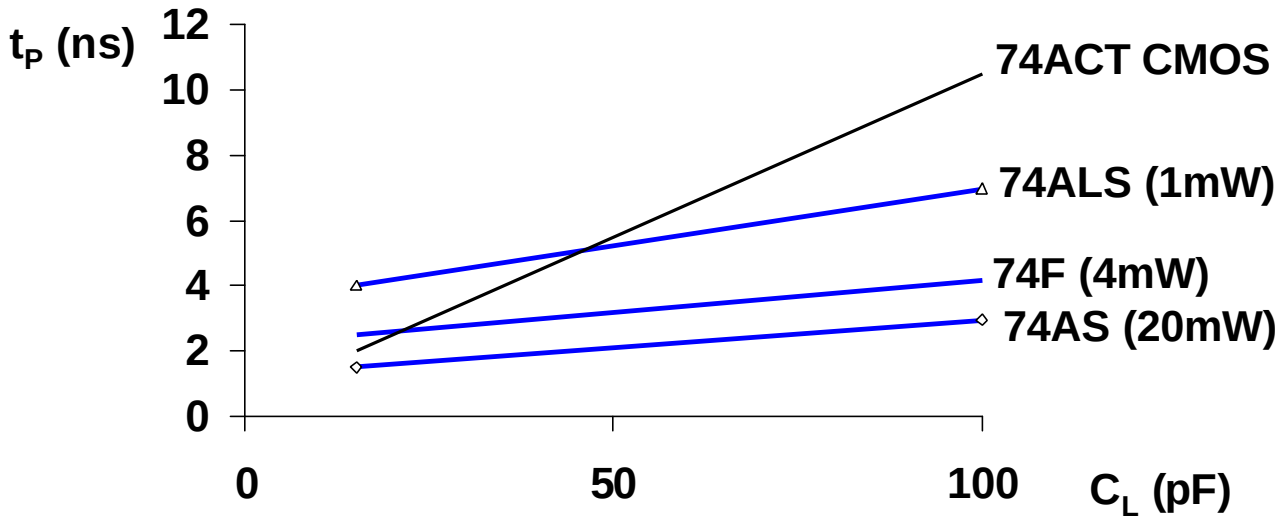
Logic Family Comparison



Within a particular family of logic gates, the PDP is fixed. Scaling resistors results in an even tradeoff between the power dissipation and the propagation delay.

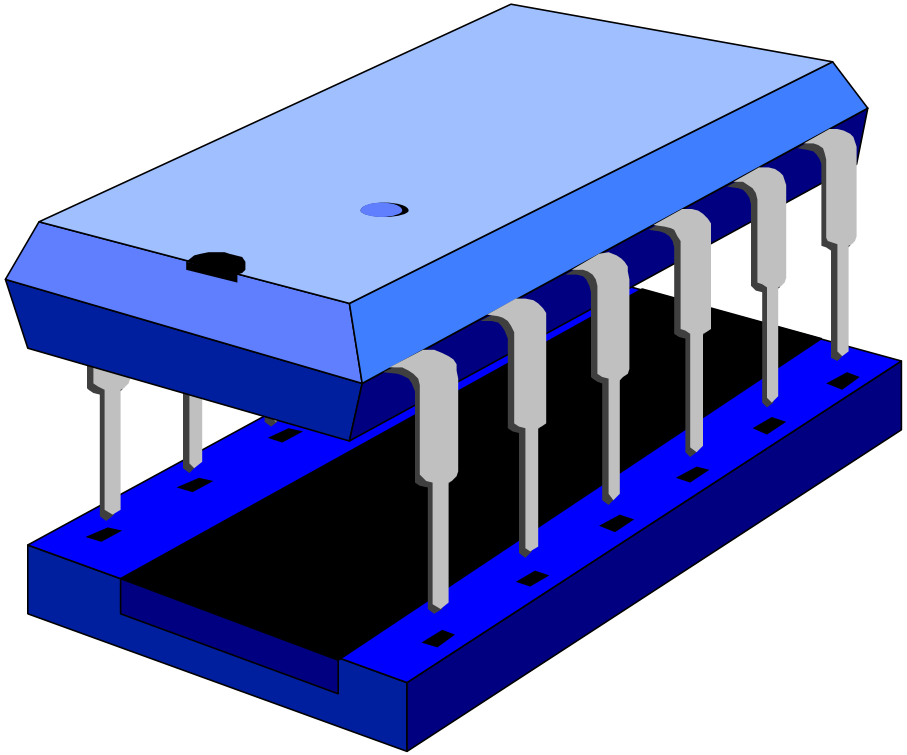
Improvements in the PDP result from circuit and device improvements.

TTL Off-Chip Data Rates

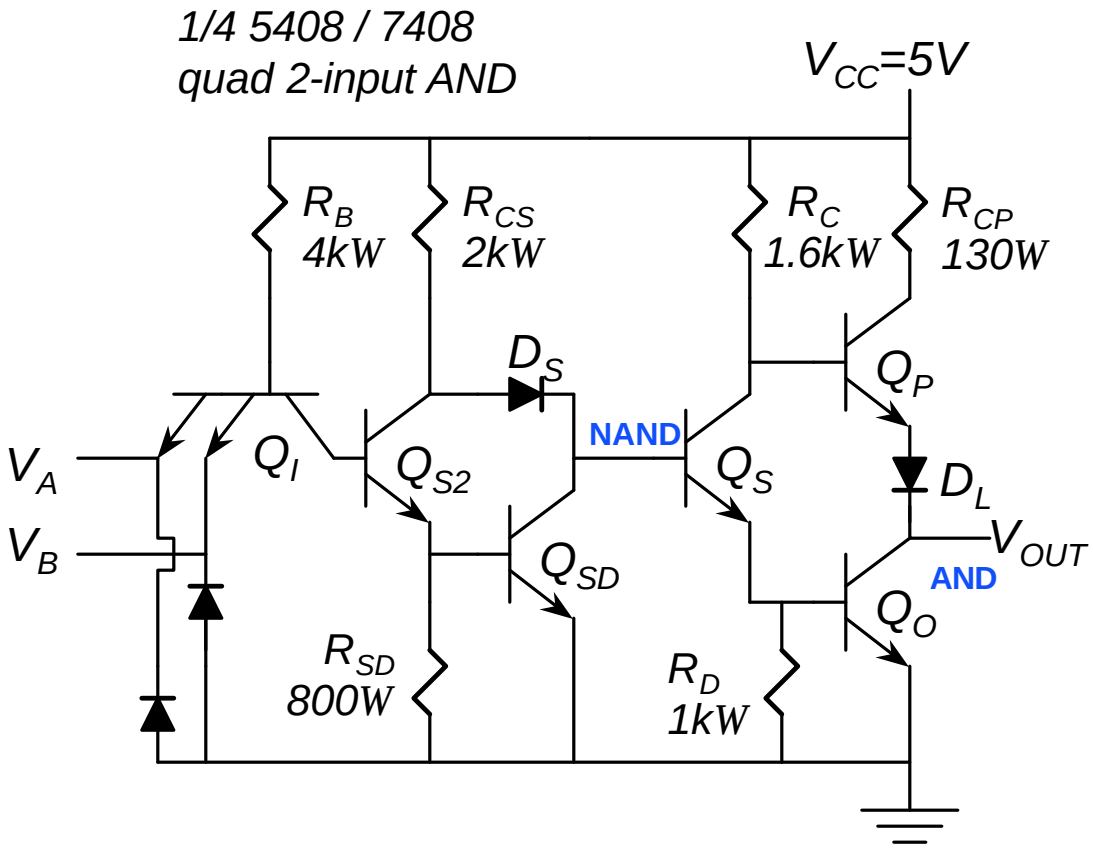


- *State-of-the-art CMOS circuits (0.35m m feature size in 1997 A.D.) achieve on-chip propagation delays of about 100 ps!*
- *Driving highly capacitive off-chip loads, TTL outstrips CMOS by a factor of 2.5.*
- *Motherboards for PC's and workstations use TTL extensively ... but this is changing as BiCMOS gains ground.*

TTL Logic Design Concepts

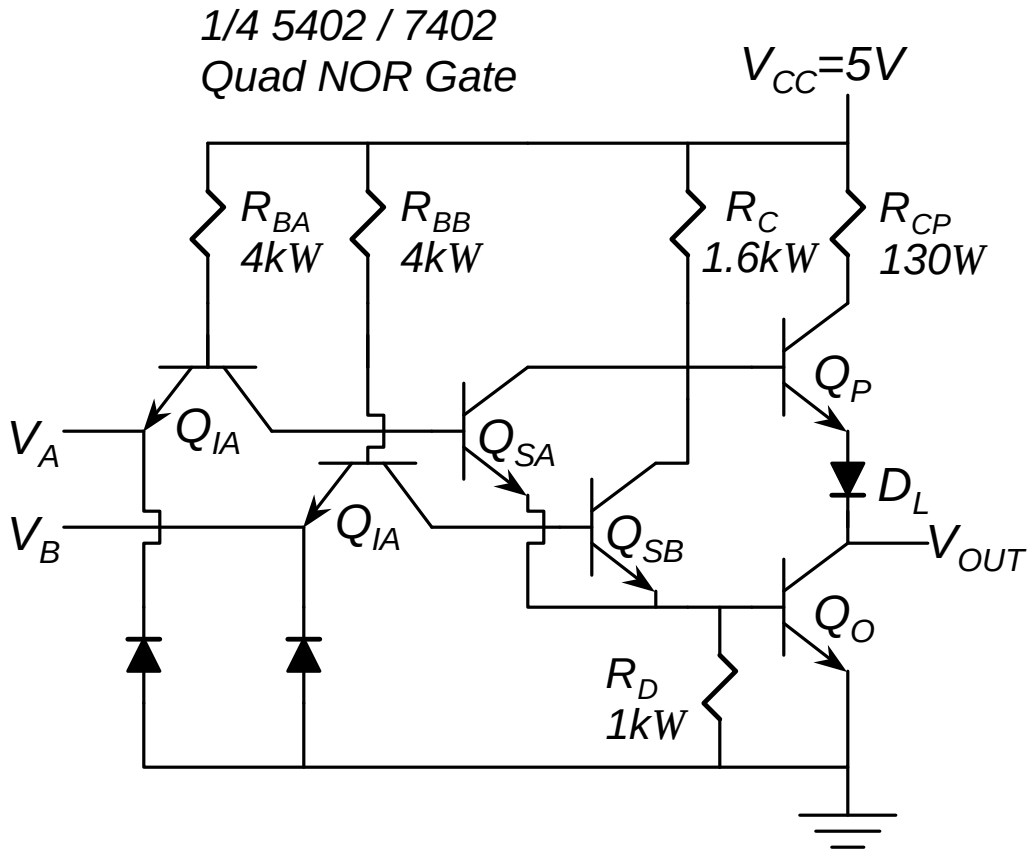


TTL AND Gate



- *Operation is similar to that of the NAND gate, but an extra inversion stage has been added.*
- *With all high inputs, Q_I is RA, Q_{S2} and Q_{SD} are SAT, Q_S and Q_O are CO, and Q_P is FA.*
- *With a low input, Q_I is SAT, Q_{S2} and Q_{SD} are CO, Q_S and Q_O are SAT, and Q_P is CO.*

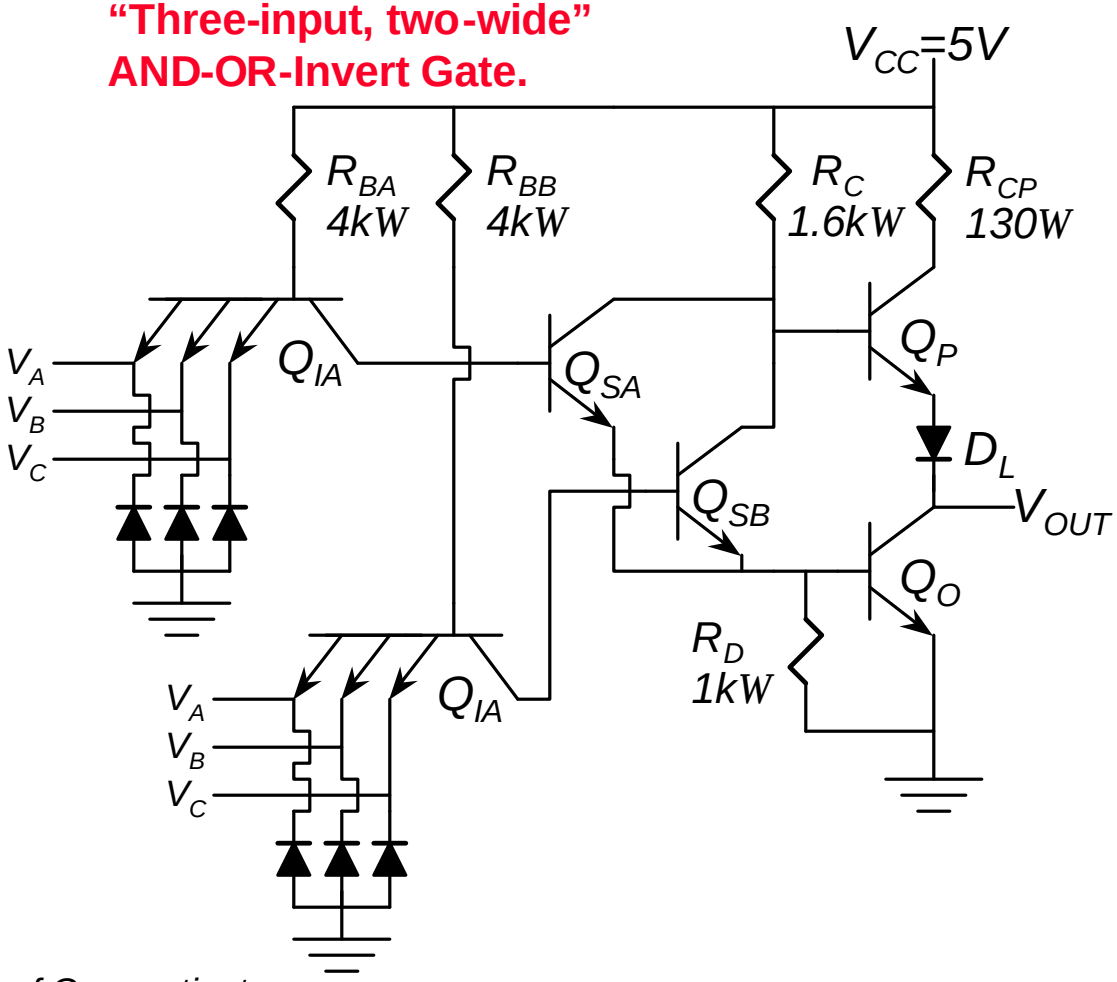
TTL NOR Gate



- *The NOR gate acts like two inverters, with paralleled drive splitters and a shared totem pole output.*
- *With a high input at A, Q_{IA} is RA, Q_{SA} and Q_O are SAT, and Q_P is CO.*
- *With both low inputs, Q_{IA} and Q_{IB} are SAT, Q_{SA} and Q_{SB} are CO, Q_O is CO, and Q_P is FA.*
- *The use of multiple emitters results in the "AND-OR-Invert" function.*

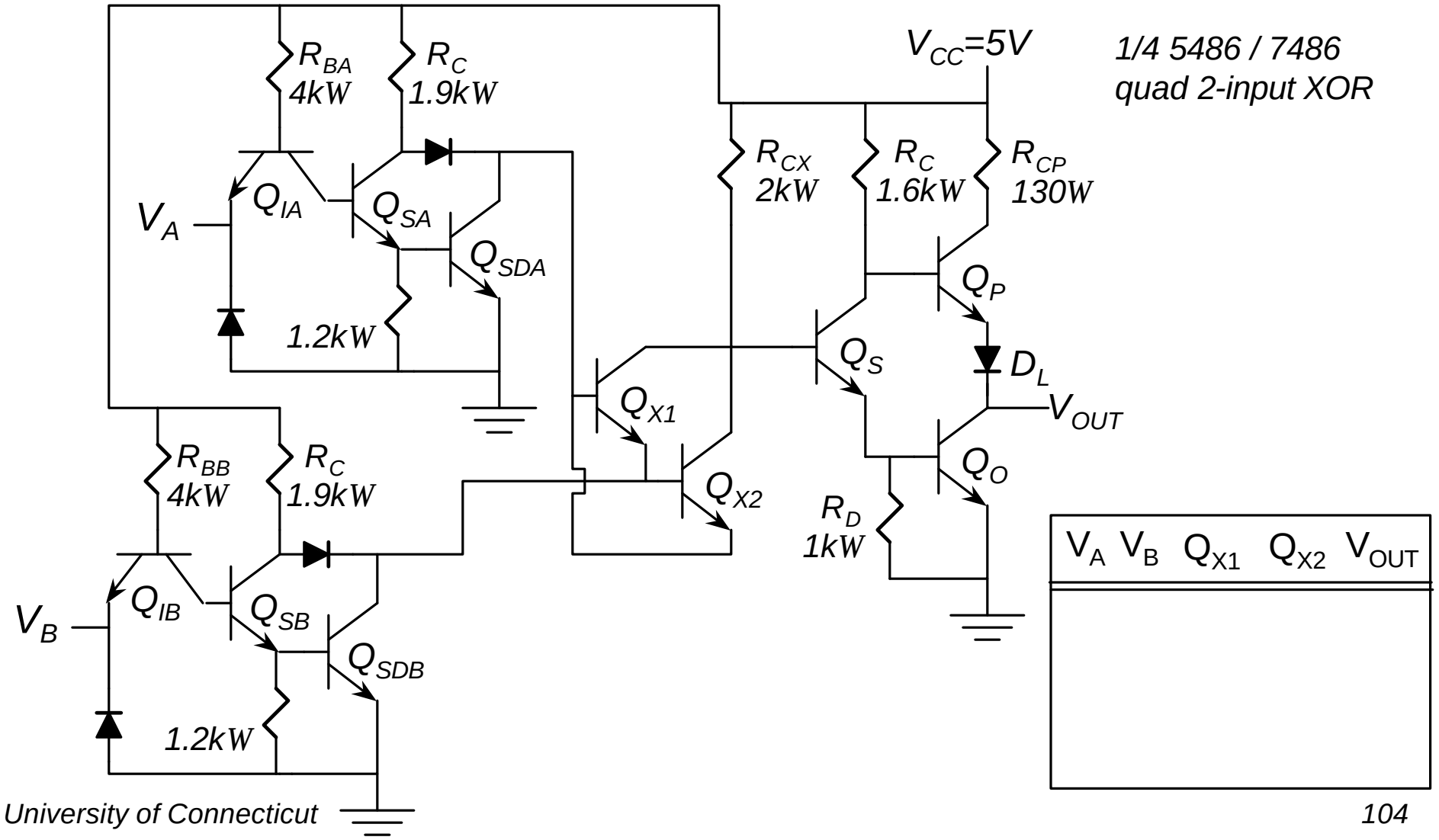
TTL AND-OR-Invert Gates

Shown is a "Three-input, two-wide" AND-OR-Invert Gate.

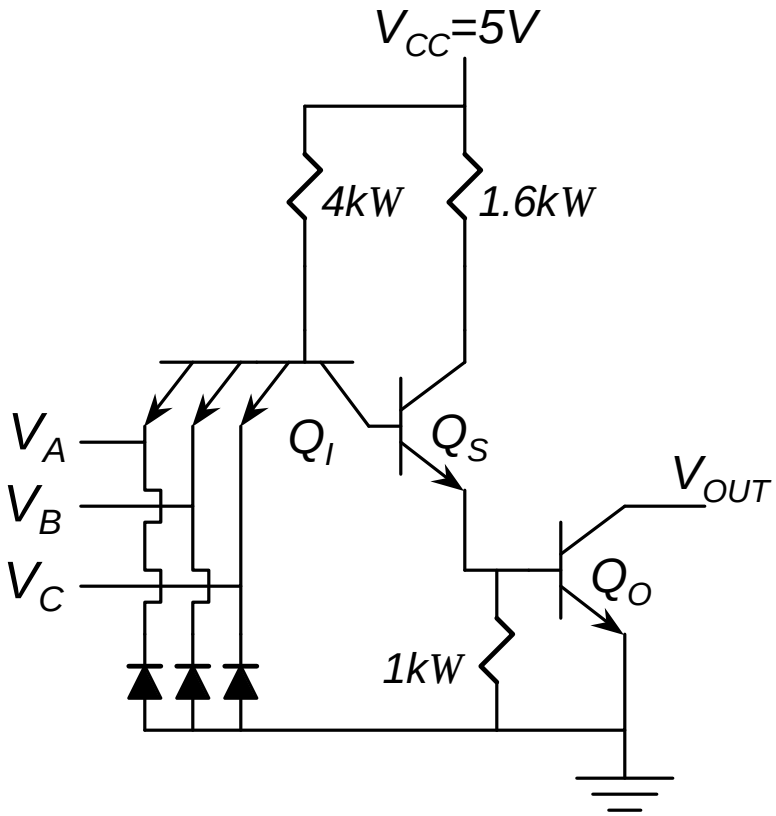


- *Multiple-emitter BJT's perform ANDing.*
- *Drive splitters provide the OR function. Together, the drive splitters and input transistors make up a "three-input expander."*
- *The output stage is inverting as usual. Output stages are available alone and are called "line drivers."*

TTL XOR Gate

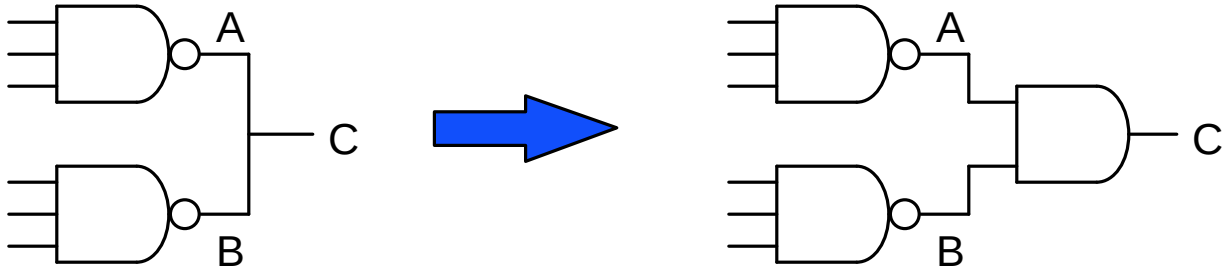

V_{CC}=5V
1/4 5486 / 7486
quad 2-input XOR
R_{BA} 4kW
R_C 1.9kW
R_{CX} 2kW
R_C 1.6kW
R_{CP} 130W
V_A
Q_{IA}
Q_{SA}
Q_{SDA}
1.2kW
Q_P
Q_S
D_L
V_{OUT}
Q_{X1}
Q_{X2}
Q_O
R_{BB} 4kW
R_C 1.9kW
R_D 1kW
V_B
Q_{IB}
Q_{SB}
Q_{SDB}
1.2kW
V_A V_B Q_{X1} Q_{X2} V_{OUT}

Open Collector TTL



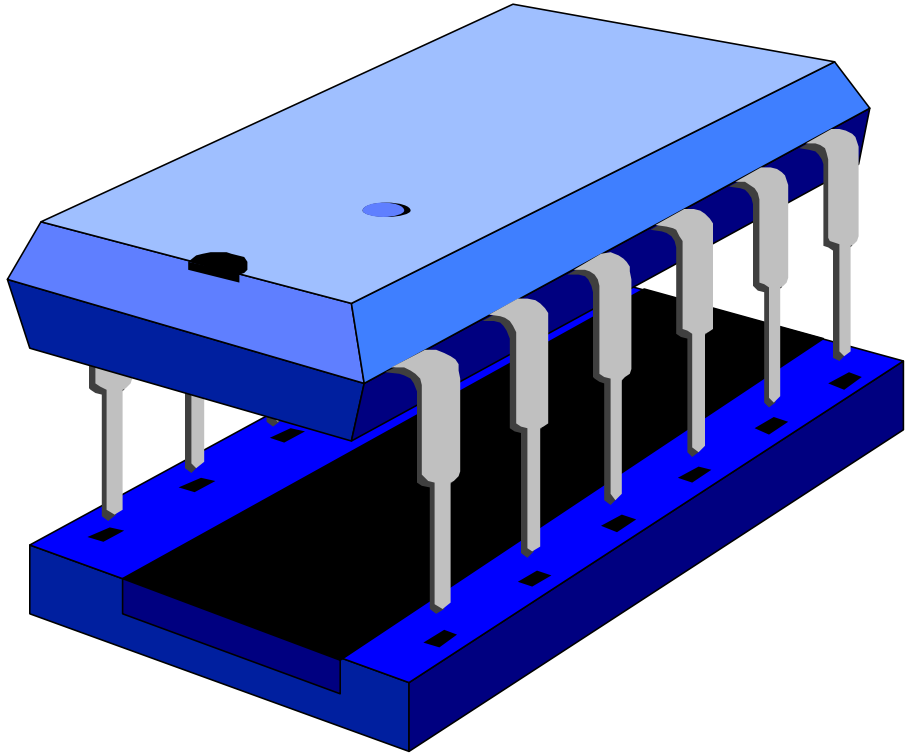
- *An "open-collector" TTL output can sink current, but can not source current.*
- *External pullup (inherently passive) is used.*
- *Open collector outputs can be wired together, resulting in the ANDing of those outputs.*

"Wired Logic" with Open Collector TTL



- *If either output A or B goes low, then C goes low. Hence, the wiring together of TTL open collector outputs results in the creation of the AND function.*
- *Wired logic cannot be implemented successfully with totem pole outputs. Can you see why?*

Integrated Injection Logic (I^2L)



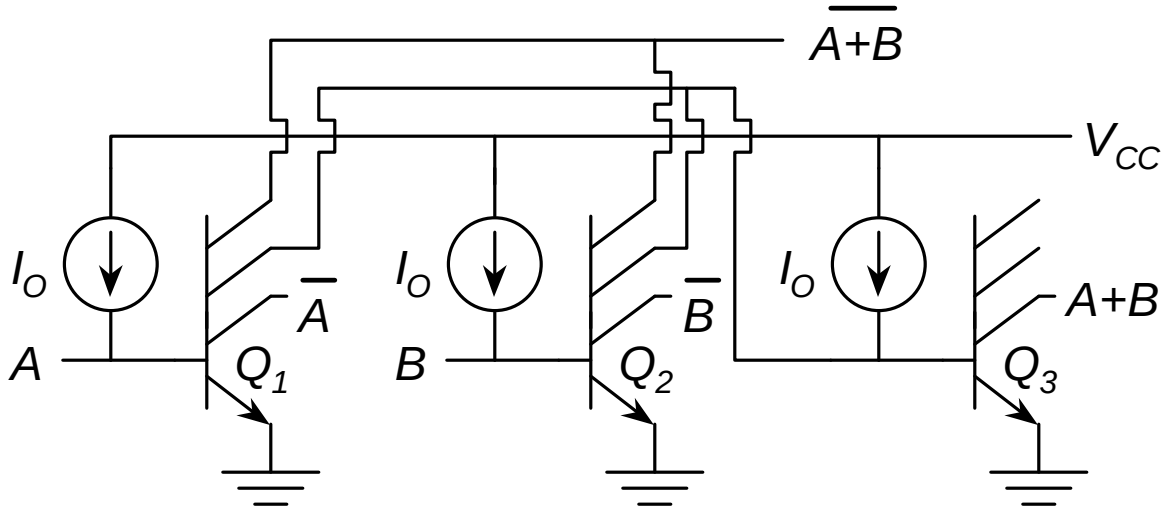
I^2L

- *TTL gates with even modest performance involve fairly complex circuits with low packing density. (74LS permits a packing density of 20 gates mm^2 using 5m m technology.)*
- *I^2L allows a factor of ten improvement in packing density compared to 74LS - even approaching the packing density of CMOS.*
- *I^2L exhibits much better PDP's than TTL - even as low as 1 pJ!*

BUT...

- *I^2L can't compete with CMOS in terms of DC dissipation.*
- *I^2L exhibits a small logic swing compared to TTL or CMOS.*

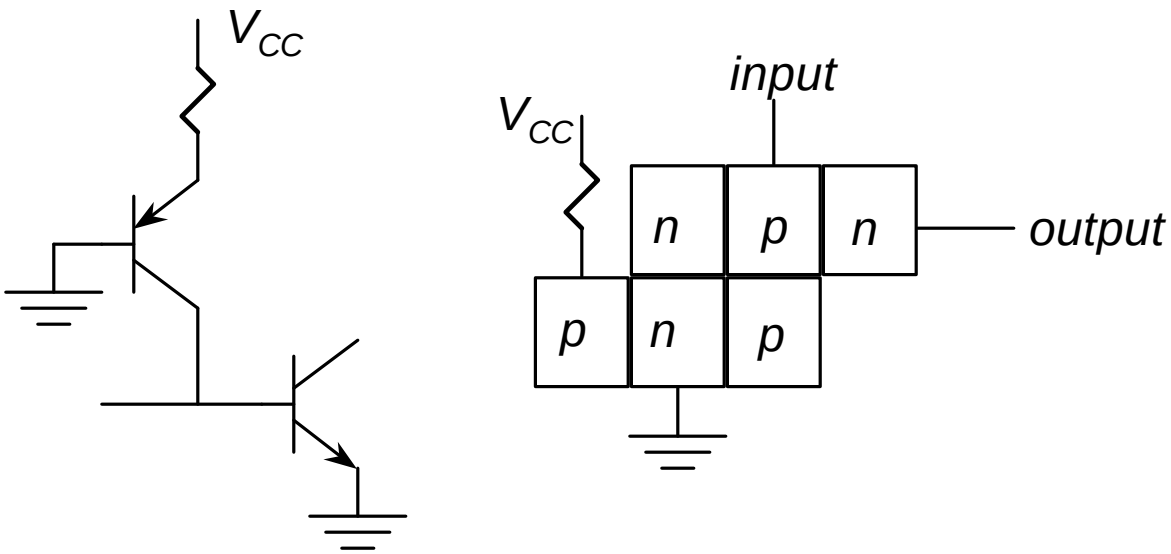
Basic I^2L



The basic I^2L building block is a multi-collector BJT with a current source driving the base.

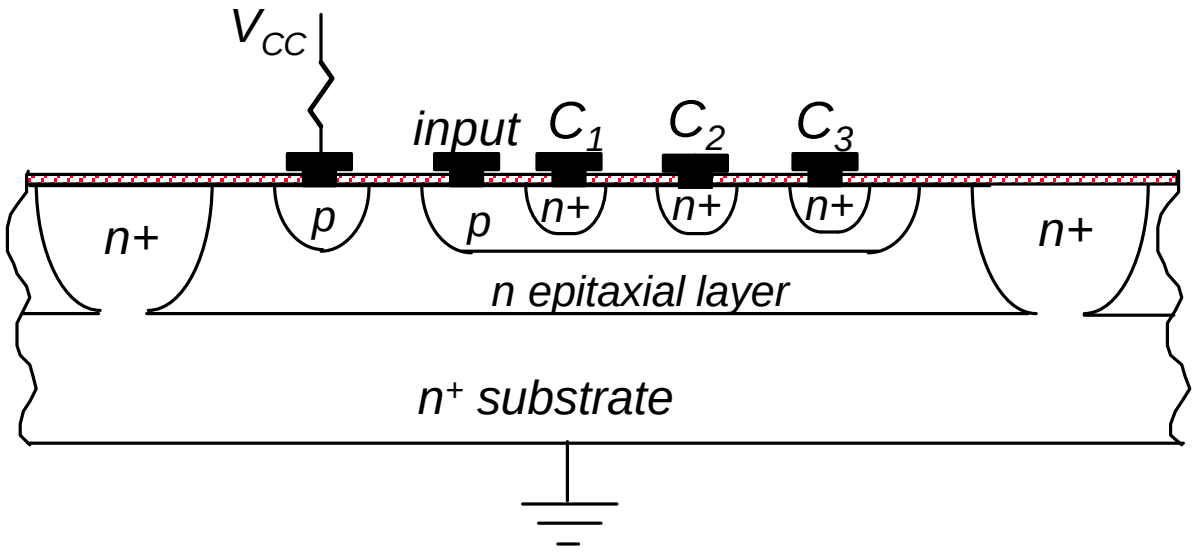
- *The output transistors switch between cutoff and saturation.*
- *Multiple collectors are connected together to form "wired logic," in similar fashion to open collector TTL outputs.*
- *How is "current hogging" prevented?*
- *What determines the fanout for I^2L?*
- *What determines V_{OH}?*

I^2L and "Merged Transistors"



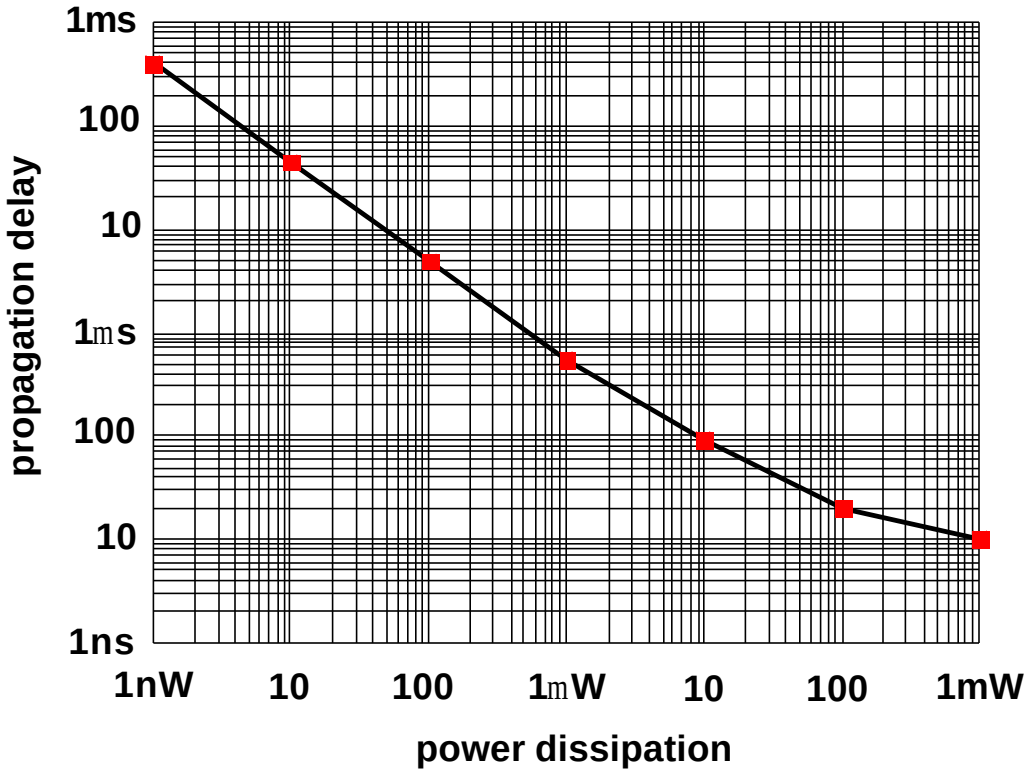
- *The base of the PNP and the emitter of the NPN are both n-type, and connected to ground. They can be "merged."*
- *Similarly, the PNP collector and NPN base are "merged."*
- *Sometimes, I^2L is also called MTL (Merged Transistor Logic).*
- *Whatever you call it, the structure is compact and results in high packing density in gates / mm^2.*

Fabrication of Merged BJT's



- *The PNP is lateral; the NPN is vertical, but "upside down."*
- *All of the ground connections are made through the substrate, saving area on the top surface.*
- *The resistors and PNP emitters ("injector rails") may be shared by multiple cells ("gate bars") to further improve the packing density.*

Standard I^2L Characteristics



- *Fantastic on-chip PDP's have been achieved (< 1pJ) with a 1V supply*
- *Off-chip loads are driven through TTL level translators.*
- *The packing density is ten times better than for 74LS.*
- *Fanout is limited to about 5.*

Advanced I^2L Circuitry

- *Schottky Integrated Injection Logic. The multiple collector regions are replaced by Schottky diodes. This improves the packing density. In addition, the reduced voltage swing improves the propagation delays.*

- *Schottky Transistor Logic. STL is similar to Schottky I^2L, but the switch transistors are Schottky clamped. Great performance has been demonstrated (0.2 pJ, 2.5 ns). The problem is complicated fabrication (two types of Schottky diodes must be made to allow finite voltage swing) and consequently low yield.*

- *Integrated Schottky Logic. ISL is similar to Schottky I^2L with two changes: The switch NPN is fabricated with the collector on the bottom and is clamped by an extra PNP.*