Section 24. Slope A/D

HIGHLIGHTS

This section of the manual contains the following major topics:

24.1 Introduction

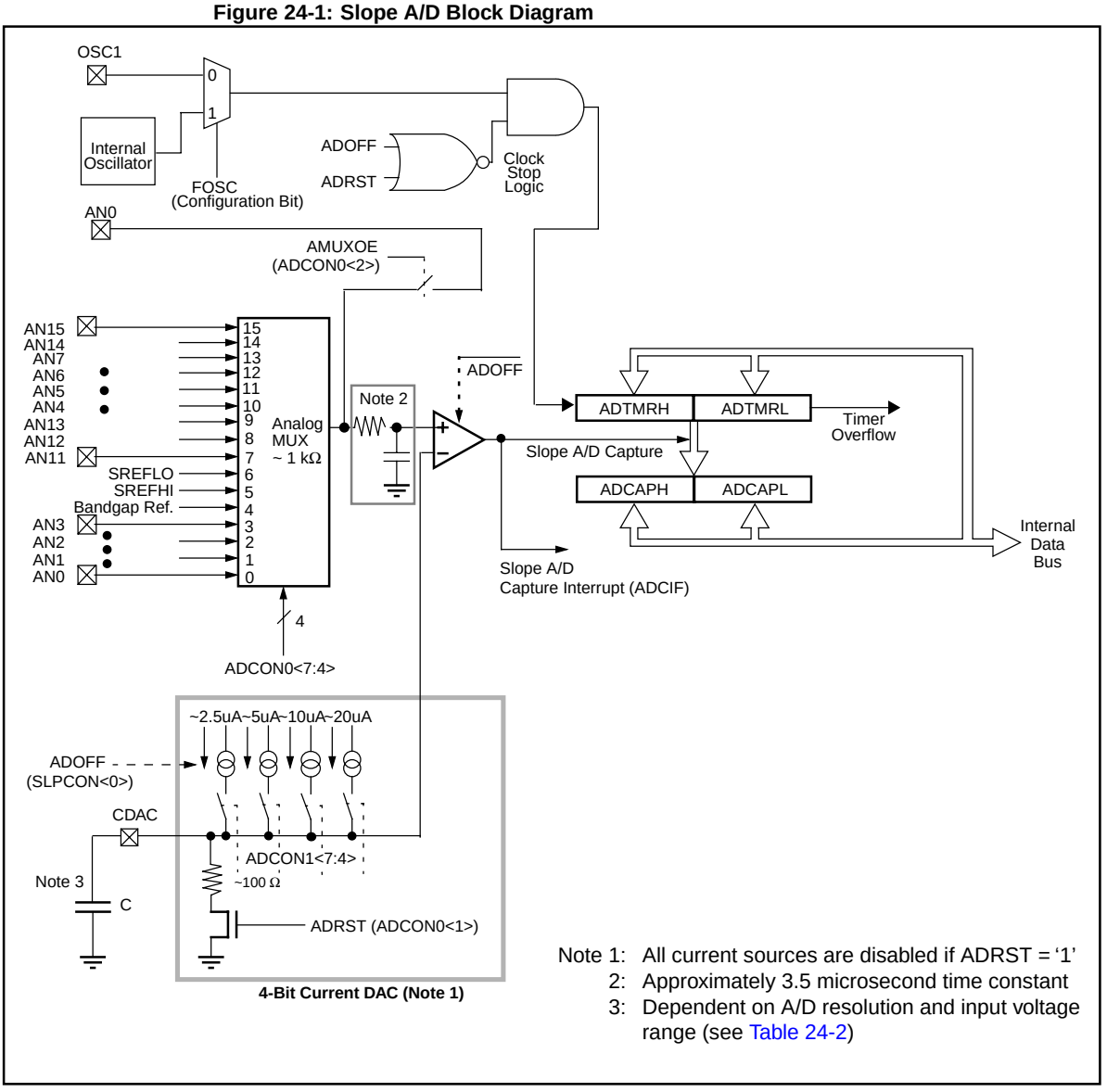
The components required to create a Slope A/D converter include:

- Precision comparator
- 4-bit programmable current source
- 16-channel analog MUX
- 16-bit timer with capture register

This section will discuss using these components for a Slope A/D.

Each analog input channel is multiplexed to a single analog input source to be converted by means of a slope conversion method (using a single precision comparator). The programmable current source feeds an external capacitor to generate the ramp voltage used in the conversion.

Figure 24-1: Slope A/D Block Diagram



Note 1: All current sources are disabled if ADRST = '1'
2: Approximately 3.5 microsecond time constant
3: Dependent on A/D resolution and input voltage range (see Table 24-2)

24.2 Control Registers

Two A/D control registers are provided to control the conversion process. They are ADCON0 and ADCON1. Both registers are readable and writable.

Register 24-1: ADCON0 Register

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-1	R/W-0
ADCS3	ADCS2	ADCS1	ADCS0	—	AMUXOE	ADRST	ADZERO
bit 7							bit 0

bit 7-4: **ADCS3:ADCS0**: Analog Channel Select bits

0000 = AN0 input
0001 = AN1 input
0010 = AN2 input
0011 = AN3 input
0100 = Bandgap reference voltage input
0101 = Slope reference SREFHI input
0110 = Slope reference SREFLO input
0111 = AN11 input
1000 = AN12 input
1001 = AN13 input
1010 = AN4 input
1011 = AN5 input
1100 = AN6 input
1101 = AN7 input
1110 = AN14 input
1111 = AN15 input

Note: For devices that do not use the full 16 A/D input channels, the unimplemented selections are reserved. Do not select any unimplemented channels.

bit 3: **Unimplemented:** Read as '0'

bit 2: **AMUXOE:** Analog MUX Output Enable

1 = Connect AMUX Output to AN0 pin (overrides TRIS setting)
0 = AN0 pin normal

bit 1: **ADRST:** A/D Reset Control Bit

1 = Stop the A/D Timer, discharge CDAC capacitor
0 = Normal operation (A/D running)

bit 0: **ADZERO**: A/D Zero Select Control

1 = Enable zeroing operation on AN1 and AN5
0 = Normal operation, sample AN1 and AN5 pins

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Register 24-2: ADCON1 Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDAC3	ADDAC2	ADDAC1	ADDAC0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7-4: **ADDAC3:ADDAC0**: Programmable Current Source Select bits

0000 = OFF - all current sources disabled
0001 = 2.25 µA
0010 = 4.5 µA
0011 = 6.75 µA
0100 = 9 µA
0101 = 11.25 µA
0110 = 13.5 µA
0111 = 15.75 µA
1000 = 18 µA
1001 = 20.25 µA
1010 = 22.5 µA
1011 = 24.75 µA
1100 = 27 µA
1101 = 29.25 µA
1110 = 31.5 µA
1111 = 33.75 µA

bit 3-0: **PCFG3:PCFG0**: Port Configuration Selects

PCFG3:PCFG2	AN4	AN5	AN6	AN7
00	A	A	A	A
01	A	A	A	D
10	A	A	D	D
11	D	D	D	D

PCFG1:PCFG0	AN0	AN1	AN2	AN3
00	A	A	A	A
01	A	A	A	D
10	A	A	D	D
11	D	D	D	D

A = Analog input D = Digital I/O

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Note: On any device reset, all port pins multiplexed with analog functions (ANx pins), are forced to be an analog input.

Register 24-3: SLPCON Register

R/W-0	U-0	R/W-1	R/W-1	U-1	R/W-1	R/W-1	R/W-1
Resv	—	REFOFF	Resv	OSCOFF	Resv	Resv	ADOFF
bit 7							bit 0

bit 7: **Reserved:** Always maintain this bit cleared.

bit 6: **Unimplemented:** Read as '0'

bit 5: **REFOFF:** Slope A/D Voltage Reference Power Control bit

1 = Voltage references are disabled (not consuming current)
0 = Voltage references are powered (consuming current)

bit 4: **Reserved:** Always maintain this bit cleared.

bit 3: **OSCOFF:** Slope A/D Oscillator Sleep Control bit

1 = Slope A/D Oscillator is disabled during SLEEP mode (not consuming current)
0 = Slope A/D Oscillator is enabled during SLEEP mode (consuming current)

bit 2: **Reserved:** Always maintain this bit cleared.

bit 1: **Reserved:** Always maintain this bit cleared.

bit 0: **ADOFF:** Slope A/D Power Control bit

1 = Slope A/D is disabled (not consuming current)
0 = Slope A/D is powered (consuming current)

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

24.3 Conversion Process

There are two methods for performing a conversion. To determine the end of conversion, the first method uses the ADTMR overflow interrupt (OVFIF bit). The second method uses the A/D Capture Interrupt (ADCIF bit). At the end of conversion both bits are used to determine if an overrange condition has occurred.

Method 1 uses a fixed conversion time, this means that the capacitor voltage always ramps to the full scale voltage. Immediately after the overflow of the ADTMR, we recommend that the ADRST bit is set to discharge the external capacitor. This will ensure that the residual voltage on the external capacitor, due to dielectric absorption, is independent of input voltage or previous conversions.

Method 2 uses a variable conversion time, which results in faster conversions for lower input voltages.

Steps for Method 1 (“fixed conversion time”):

1. Initialize the Slope A/D module:
   a) Clear the REFOFF bit (SLPCON<5>)
   b) Clear the ADOFF bit (SLPCON<0>)
   c) Initialize ADCON1<7:4> to select the programmable current source.
2. Set the ADRST bit (ADCON0<1>), until the ramp capacitor reaches ground. This is capacitor dependent. A minimum of 200 µs is recommended.
3. Select Input Channel
4. Clear the OVFIF and ADCIF bits.
5. Initialize Slope A/D Timer (ADTMR). ADTMR value depends on bits of resolution required (see Table 24-1).
6. To start a conversion, clear the ADRST bit, this allows the ramp capacitor to begin charging and the ADTMR to increment.
7. Conversion is complete when the Slope A/D timer (ADTMR) overflows from FFFFh to 0000h. This causes the OVFIF bit to be set.
8. Check if the ADCIF bit is set. If this bit is set, the value in the capture register ADCAP is valid. This method depends on minimum latency to verify the capture interrupt flag bit after the ADTMR overflows. If the ADCIF bit is cleared, then the input voltage was out of the A/D input range.
9. Set the ADRST bit (ADCON0<1>) to stop ADTMR and discharge external capacitor
10. Do Conversion Calculations
11. Goto Step 2

Steps for Method 2 (“variable conversion time”):

1. Initialize the Slope A/D module:
   a)Clear the REFOFF bit (SLPCON<5>).
   b)Clear the ADOFF bit (SLPCON<0>).
   c)Initialize ADCON1<7:4> to select the programmable current source.
2. Set the ADRST bit (ADCON0<1>), until the ramp capacitor reaches ground. This is capacitor dependent. A minimum of 200 µs is recommended.
3. Select Input Channel.
4. Clear the OVFIF and ADCIF bits.
5. Initialize Slope A/D Timer (ADTMR). ADTMR value depends on bits of resolution required (see Table 24-1).
6. To start a conversion, clear the ADRST bit, this allows the ramp capacitor to begin charging and the ADTMR to increment.
7. Conversion is complete when the ramp voltage exceeds the analog input so the comparator output changes from high to low. This causes the ADCIF bit to be set.
8. Check if the ADTMR did not increment more counts than the maximum resolution allowed. If there were more counts, then the input voltage was out of the A/D input range.
9. Set the ADRST bit (ADCON0<1>) to stop ADTMR and discharge external capacitor
10. Do Conversion Calculations.
11. Go to Step 2.

Note:	The Slope A/D timer continues to run following a capture event.

The maximum Slope A/D timer count is 65,536. It can be clocked by the on-chip or external oscillator. At a 4 MHz oscillation frequency, the maximum conversion time is 16.38 ms for a full count. A typical conversion should complete before full-count is reached. The timer overflow flag is set once the timer rolls over (FFFFh to 0000h), and an interrupt occurs, if enabled.

End-user calibration is simplified or eliminated by making use of the on-chip EPROM. Internal component values are measured at factory final test and stored in the memory for use by the application firmware.

Periodic conversion cycles should be performed on the bandgap and slope references (described in Subsection **24.4 “Other Analog Modules”**) to compensate for Slope A/D component drift. Measurements for the reference voltage counts are equated to the voltage value stored into EPROM during calibration. Since all measurements are relative to the reference, offset voltages inherent in the comparator are minimized. The Slope A/D clock source does not require a precise frequency, only a stable frequency.

See AN624, “PIC14000 Slope A/D Theory and Implementation” for further details of Slope A/D operation.

24.3.1 Slope A/D Timer (ADTMR)

The Slope A/D timer (ADTMR) is comprised of a 16-bit timer (ADTMRH:ADTMRL), which is incremented every oscillator cycle. The ADTMR registers are cleared by a power-on reset; otherwise the software must initialize it after each conversion. A separate 16-bit capture register (ADCAPH:ADCAPL) is used to capture the ADTMR count if a Slope A/D capture event occurs (see below). Both the Slope A/D timer and capture registers are readable and writable. The 16-bit timer is a read/write register and is cleared on any device reset.

Note 1:	Reading or writing the ADTMR register during an Slope A/D conversion cycle can produce unpredictable results and is not recommended.
Note 2:	The correct sequence for writing the ADTMR register is HI byte followed by LO byte. Reversing this order will prevent the Slope A/D timer from running.

During a conversion one or both of the following events will occur:

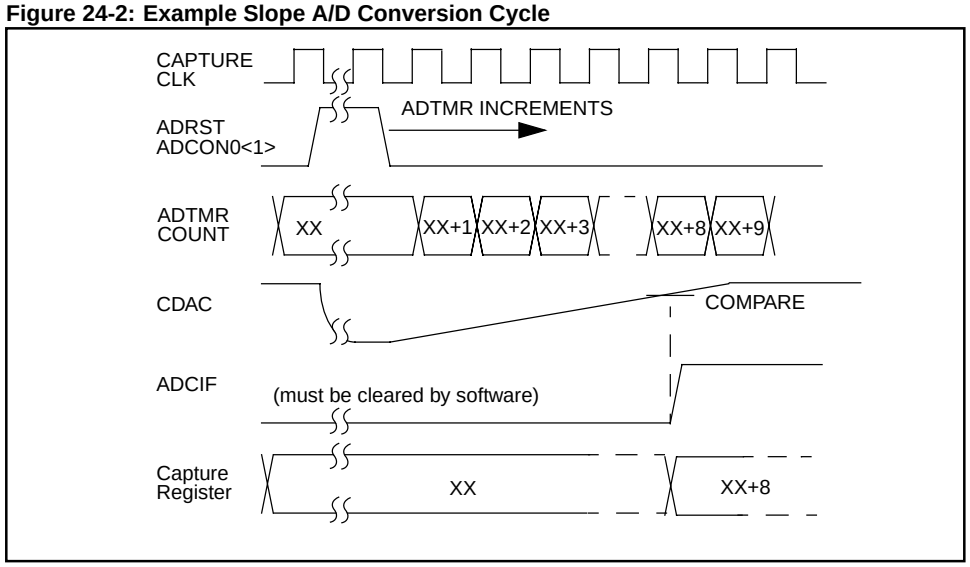
- capture event
- timer overflow

In a capture event, the comparator trips when the slope voltage on the CDAC output exceeds the input voltage from the selected Slope A/D channel, causing the comparator output to transition from high to low. This causes a transfer of the current timer count to the capture register and sets the ADCIF flag bit.

An interrupt will be generated if the ADCIE bit is set (interrupt enabled). In addition, GIE and PIE bits must be set. Software is responsible for clearing the ADCIF flag bit prior to the next conversion cycle. This interrupt can only occur once per conversion cycle.

In a timer overflow condition, the timer rolls over from FFFFh to 0000h, and a capture overflow flag (OVFIF) is asserted. The timer continues to increment following a timer overflow. An interrupt can be generated if bit OVFIE is set (interrupt enabled). In addition, the GIE and PIE bits must be set. Software is responsible for clearing the OVFIF flag bit prior to the next conversion cycle.

Figure 24-2: Example Slope A/D Conversion Cycle



24.3.2 Sleep Operation

The Slope A/D may operate when the device is in Sleep mode. For the Slope A/D to do a conversion during Sleep mode, the Slope A/D module must have a device clock. For a clock to be present the OSCOFF bit must be cleared before going to SLEEP. Also the REFOFF and ADOFF bits must be cleared to ensure that the results reflect the voltage on the input channel. By doing an A/D conversion during Sleep mode, the result has improved accuracy due to a reduction of system noise.

When the device clock is disabled, the Slope A/D Timer (ADTMRH:ADTMRL) stops incrementing. Even if the Slope A/D module is not disabled, the slope A/D cannot wake-up the device. This is because the ADCIF bit cannot be set, which is one of the control bits used to wake the device from SLEEP mode. When the device awakes, if the comparator value has tripped, the capture and interrupt will occur. The value in the ADCAP registers is meaningless.

For maximum power savings, all analog components of the Slope A/D module should be disabled (no conversion in progress).

24.3.3 Effects of a Reset

After any device reset, the Slope A/D module is disabled (lowest current state) and the device I/O are configured as analog channels.

24.3.4 Slope A/D Comparator

This module includes a high gain comparator for Slope A/D conversions. The non-inverting input terminal of the Slope A/D comparator is connected to the output of an analog MUX through an RC low-pass filter. The inverting input terminal is connected to the external ramp capacitor.

The output of the comparator is used to cause the capture event to occur. This causes the value in the ADTMR registers to be loaded into the ADCAP registers. This output will also cause the ADCIF bit to be set.

24.3.5 Analog MUX

A total of 16 channels are internally multiplexed to the single Slope A/D comparator positive input. Four configuration bits (ADCON0<7:4>) select the channel to be converted.

24.3.6 Programmable Current Source

Four configuration bits (ADCON1<7:4>) are used to control a programmable current source for generating the ramp voltage to the Slope A/D comparator. This allows compensation for full-scale input voltage, clock frequency and the external capacitor tolerance variations.

Setting the ADRST bit disconnects the current source from the CDAC pin. Current flow begins when the ADRST bit is cleared.

The programmable current source output is tied to the CDAC pin. This current source is used to charge an external capacitor, which generates the ramp voltage for the Slope A/D comparator (Figure 24-1).

24.3.7 Slope A/D Resolution, Speed, Voltage Range, and Capacitor Selection

The Slope A/D module allows many trade-offs. For a conversion the user needs to make the following Trade-offs:

- The Resolution of the Result
- The Speed of the Conversion
- The Analog Input Voltage Range
- The External Capacitor

The resolution is the number of bits that is used by the ADTMR to represent the measured input voltage. This resolution affects the time that the conversion can be completed in. Table 24-1 shows the trade-off between the resolution of the conversion and the maximum conversion time.

The conversion time for the Slope A/D converter can be calculated using the equation:

Conversion Time = (1/Fosc) x 2^N

Where Fosc is the oscillator frequency and N is the number of bits of resolution desired.

Therefore at 4 MHz, the conversion time for 16 bits is 16.384 msec. Conversely, it is 256 µsec for 10-bits.

Table 24-1: ADTMR Initialization Values and Conversion Times

Resolution Bits	Value Loaded into ADTMR	Maximum Conversion Time		
		Cycles	20 MHz	4 MHz
16	0000h	65536 TOSC	3.28 ms	16.38 ms
15	8000h	32768 TOSC	1.64 ms	8.2 ms
14	C000h	16384 TOSC	820 µs	4.1 ms
13	E000h	8192 TOSC	410 µs	2.05 ms
12	F000h	4096 TOSC	204.8 µs	1.03 ms
11	F800h	2048 TOSC	102.4 µs	500 µs
10	FC00h	1024 TOSC	51.2 µs	250 µs

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The selection of the external capacitor is determined by the desired characteristics of the application. These include

- Input Voltage Range (widest range of all input channels)
- Conversion Time
- Programmable Current Source Output Values

The selection of these values should be done to minimize the time between a comparator trip (ADCIF bit is set) to the ADTMR overflow (OVFIF is set). This ensures that the entire range of the ADTMR is used for the A/D conversion process.

The equation for selecting the ramp capacitor value is:

Capacitor = (conversion time in seconds) X
(current source output in amps) / (full scale in volts)

Table 24-2 provides example capacitor values for the desired Slope A/D resolution, conversion time, and full scale voltage measurement.

This capacitor on the CDAC pin should have a low voltage-coefficient as found in teflon, polypropylene, or polystyrene capacitors, for optimum results. This external capacitor must be discharged at the beginning of each conversion cycle by setting the ADRST bit (ADCON0<1>). The time for the ADRST bit to be set depends on the characteristics of the external capacitor for a complete discharge.

Table 24-2: External Capacitor Selection (@ 4 MHz)

Slope A/D Resolution (Bits)	Conversion Time (ms)	Full Scale (Volts)	Slope A/D Current Source Select		Calculated CDAC Capacitor	CDAC Capacitor Nearest Standard Value
			ADDAC3:ADDC0	Typical Output (μamps)		
16	16.384	3.5	1100	27	0.126 μF	0.12 μF
		2.0	1010	22.5	0.184 μF	0.18 μF
		1.5	1011	24.75	0.270 μF	0.27 μF
14	4.096	3.5	1101	29.25	34 nF	33 nF
		2.0	1011	24.75	50.7 nF	47 nF
		1.5	1100	27	73.7 nF	68 nF
12	1.024	3.5	1101	29.25	8.56 nF	8.2 nF
		2.0	1001	20.25	10.4 nF	10 nF
		1.5	1010	22.5	15.4 nF	15 nF
10	0.256	3.5	1011	24.75	1.81 nF	1.8 nF
		2.0	1010	22.5	2.88 nF	2.7 nF
		1.5	1011	24.75	4.22 nF	3.9 nF

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24.4 Other Analog Modules

Additional analog modules for mixed signal applications are required. These include:

- bandgap voltage reference
- slope reference voltage divider

24.4.1 Bandgap Voltage Reference

The bandgap reference circuit is used to generate a 1.2V nominal stable voltage reference for the Slope A/D, the low-voltage detector, and the slope reference divider. The bandgap reference voltage is available on the analog MUX. To enable the bandgap reference REFOFF (SLPCON<5>) must be cleared. The bandgap reference must be enabled for any slope A/D conversion.

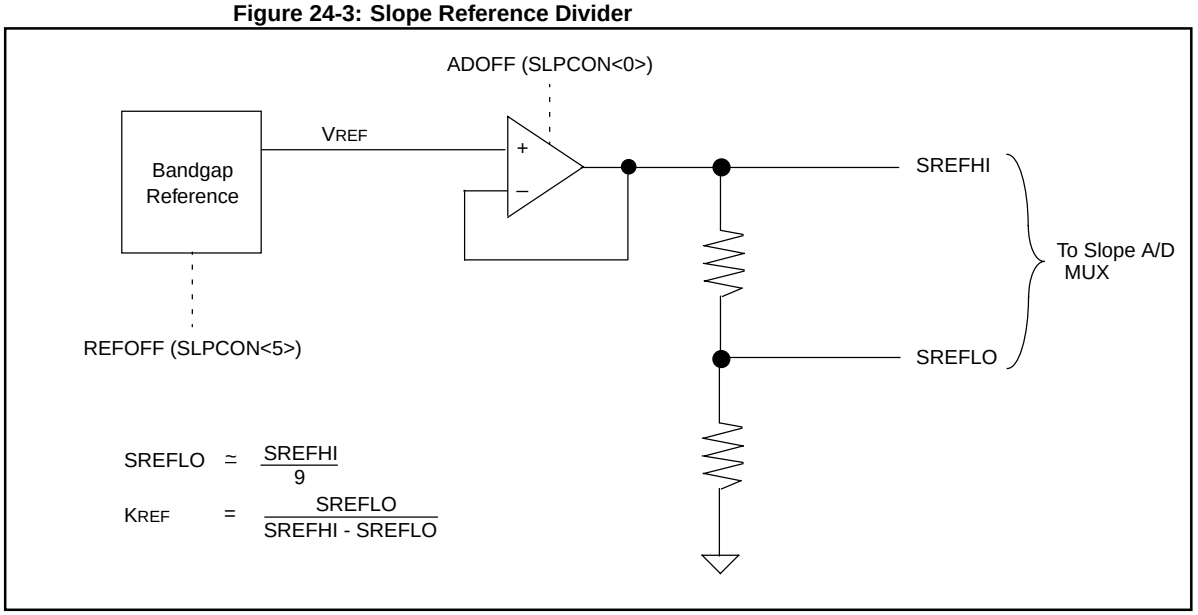
The bandgap reference calibration factor is stored in the calibration space EPROM.

24.4.2 Slope Reference Voltage Divider

The slope reference voltage divider circuit, consisting of a buffer amplifier and resistor divider, is connected to the internal bandgap reference producing two other voltage references called SREFHI and SREFLO (see Figure 24-3). SREFHI is nominally the same as the bandgap voltage, 1.2V, and SREFLO is nominally 0.13V. These reference voltages are available on two of the analog multiplexer channels. The Slope A/D module and firmware can measure the SREFHI and SREFLO voltages, and in conjunction with the KREF and KBG calibration data correct for the ADC's offset and slope errors.

See AN624 for further details.

Figure 24-3: Slope Reference Divider



24.5 Calibration Parameters

The Slope A/D module has several analog components. Like all CMOS circuitry the parametric values vary with process, temperature, voltage, and time. Devices have been designed to minimize the effect of these variations. In addition, each device, with the slope A/D module, is calibrated at factory test by measuring several key parameters and storing these values into EPROM at specified locations. The customer's application program may access this data and use it to mathematically compensate for device variations.

Collectively, these data values are referred to as calibration constants. The calibration constants are listed in Table 24-3. The 32-bit floating point representation has an exponent byte, and three bytes of mantissa. For information on floating point algorithms, refer to AN575.

Table 24-3: Calibration Constants

Parameter	Symbol	Number of Bytes	Representation of Value
A/D Slope reference ratio	KREF	4	32-bit Floating Point
Bandgap reference voltage	KBG	4	32-bit Floating Point

For additional information on using the calibration parameters see Application Note 624.

24.5.1 Using Calibration Data

The calibration constants should be used by the application firmware to obtain the best accuracy. KREF and KBG are used in A/D conversions.

24.5.2 Parameter Variation

Table 24-4 lists the "Maximum Parameter Variation" attainable when the calibration data is not used as well as the "Expected Parameter Variation with Calibration."

If the accuracies without calibration are adequate for the task at hand, no further calibrations of the module are necessary. If greater accuracy is needed, the calibration constants must be used.

Table 24-4: Parameter Variation

Symbol	Parameter	Maximum Variation Without Calibration	Achievable Variation with Calibration
KREF	A/D slope reference ratio	+/- 2.2%	+/- 0.13%
KBG	Bandgap reference voltage	+/- 4.2%	+/- 0.058%

24.5.3 Device Programming

24.5.3.1 Non-Windowed Parts

Non-windowed parts are programmed just like any PIC16CXXX processor. The calibration area is write-protected during factory calibration.

24.5.3.2 Windowed Parts

Caution:

Windowed parts must not be write-protected. If the parts are erased by ultraviolet light, the calibration parameters are lost and cannot be reprogrammed once the part has been write-protected.

Calibration data must be read out and saved before erasing a windowed part. There is no way to recreate these values, so if they are lost the part can no longer be calibrated.

24.6 Design Tips

Question 1: ***What are some recommended Capacitor types?***

Answer 1:

Polypropylene film capacitor is a good trade-off between cost, availability and performance

Question 2: ***Can you suggest some sources for Capacitors***

Answer 2:

A source is:

Southern Electronics Company
Telephone: (203) 876-7488

Question 3: ***I used the recommended capacitor and Programmable Current Source from Table 24-2, and my A/D input range does not match.***

Answer 3:

That table is meant to be a good starting point, but does not include variation that is the result of the device not operating at exactly 4 MHz; tolerance of the external capacitor and variations of the Programmable Current Source, due to process and application temperature.

A conversion on the Bandgap Reference can be used to judge how to adjust the Programmable Current Source Output to ensure proper A/D full scale conversions. Example code (routine ad_optimize, in P14_RV10.ASM) for this adjustment is available with the PICDEM-14A Demo Board, and may be also available on the Microchip web site.

Question 4: ***I am using the PIC14C000 which also has the on-chip Temperature sensor. The sensor results seem to be a little high.***

Answer 4:

This may be caused by self heating of the DIE. Self heating of the DIE may be caused by a few things, including:

- I/O sinking and/or sourcing significant amount of current
- Power dissipation of the device running
  (remember the PIC14C000 can operate in sleep mode)
- Package type due to junction to ambient temperature coefficient of package

For best results the power dissipation should be kept low. Calibration is performed with the device in a low power state.

Question 5: ***My A/D conversion results seem affected by the operation of high current components on my board. What can I do to minimize this?***

Answer 5:

The high current components on your board may cause the ground potential difference across the ground trace or ground plane. To minimize this effect, you should employ two system grounds on the application board. The first ground, analog ground, used for the reference analog signals (Slope A/D external capacitor ground, Resistor Divider ground, and etc.). No high current nor any digital power returns should go through this analog ground system.

The second ground, digital ground, is used for all other digital logic in the system. The application's digital logic will inject noise onto this ground. Proper grounding techniques should be used to minimize this noise.

These two grounds are connected at the PICmicro's ground pin. Ideally the two grounds are implemented using separate ground planes. In most cases, this can still be implemented on a two layer board. One layer is used for both ground systems, where the two planes are separated by a gap. The second layer is used as the trace layer.

24.7 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the Slope A/D are:

Title	Application Note #
PIC14C000 Calibration Parameters	AN621
PIC14C000 A/D Theory and Implementation	AN624
Lead Acid Battery Charger Implementation using the PIC14C000	AN626

24.8 Revision History

Revision A

This is the initial released revision of the Slope A/D module description.