Chapter

1

History of the High-Voltage Charge Pump

The quest for generating a high voltage supply from an available lower voltage supply has existed since the discovery of electricity. The invention of the "induction ring" by Michael Faraday, the British physicist and chemist, in 1831, began the process of generating high voltages from an available lower input voltage using transformers. The need for producing even higher voltages was accentuated by the requirements from physicists, using particle accelerators, to create high energy particles for studying subatomic physics. It was only during this time that Cockcroft and Walton invented a novel method for generating extremely high voltages using a unique connection of discrete diodes and capacitors—a technique that was later adopted by John F. Dickson for implementation on a modern integrated circuit. This chapter will start by examining the transformer and its shortcomings and then gradually lead to a discussion of Dickson's implementation of the charge pump.

1.1 Using a Transformer to Generate High Voltages

A transformer makes it possible to convert AC power at a given voltage level to AC power at a different voltage level. It, of course, cannot increase the maximum power that could be delivered to the output load through the transformation process. In the ideal situation, the power delivered at the transformed output is equal to the power consumed at the input port. If the transformed voltage level is raised, the current at transformed node is proportionally lowered, and vice versa. The transformer, shown in Figure 1-1, is constructed using a ferromagnetic core around which two sets of coils, or multiple coils, of insulated wire

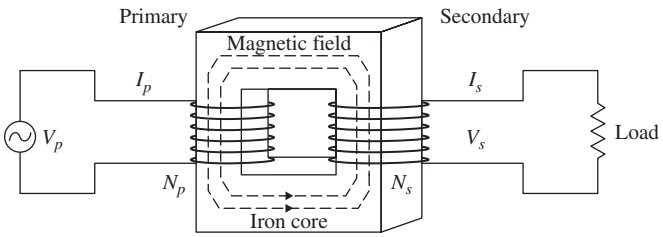

Figure 1-1 A simple transformer.

are wrapped. The input line connects to the "primary" coil, whereas the output lines connect to the "secondary" coils. The alternating current in the primary coil induces an alternating magnetic flux that "flows" around the ferromagnetic core, changing direction during each electrical cycle. The alternating flux in the core, in turn, induces an alternating current in each of the secondary coils. The voltage at the output of the secondary coils is directly related to the primary voltage by the turn's ratio, or the number of turns in the primary coil divided by the number turns in the secondary coil.

For an ideal transformer,

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} \tag{1-1}$$

where V_s and V_p are the voltages at the secondary and the primary nodes, respectively, and N_s and N_p are the number of turns of the secondary and primary coils, respectively. For instance, if the primary coil consists of 100 turns and carries 110 volts, and a secondary coil consists of 1000 turns, the secondary voltage is the following:

$$V_s = 110 \text{ V} \frac{1000}{100} = 1100 \text{ V}$$

The voltage transformation ratio (primary voltage to secondary voltage) and the current transformation ratio (primary current to secondary current) actually depend on the turns' ratio. Thus, the AC output voltage can either be decreased or be increased by selecting the correct number of turns. A transformer may have multiple secondary coils to feed a number of electrical loads. Yet, a transformer will only work with an input that is alternating voltage source, whereas, in general, electronic circuits require a DC voltage supply to operate. If a high-voltage DC output is required, the stepped-up output AC signal needs to be converted into a DC voltage by using a rectifier—a cumbersome process especially at high voltages. Further, generating high voltages using a

transformer makes the transformer very large, heavy, and inefficient—a sure handicap in the modern trend of micro-miniaturization.

1.2 The Cockcroft-Walton High-voltage Charge Pump

Voltage multiplication greater than twice the supply voltage can also be achieved by cascading more than one diode capacitor voltage stage in series. The Swiss physicist Heinrich Greinacher first proposed this kind of voltage multiplier back in 1919. Later, this technique was used by John Douglas Cockcroft and Ernest Thomas Sinton Walton to generate voltage potentials of more than 800,000 volts in their particle accelerator, which in 1951 won Cockcroft and Walton the Nobel Prize in Physics for their research, titled "Transmutation of atomic nuclei by artificially accelerated atomic particles."[1] Cockcroft and Walton, depicted in Figure 1-2, at the Cavendish Laboratory in Cambridge, England, sought a way into the nucleus through a prediction of quantum mechanics. In 1930, Cockcroft and Walton used a 200-kilovolt transformer to accelerate subatomic particles along a straight discharge tube, but they concluded that the particle's energy was not sufficient to trigger any effects and therefore decided to seek higher particle energies.

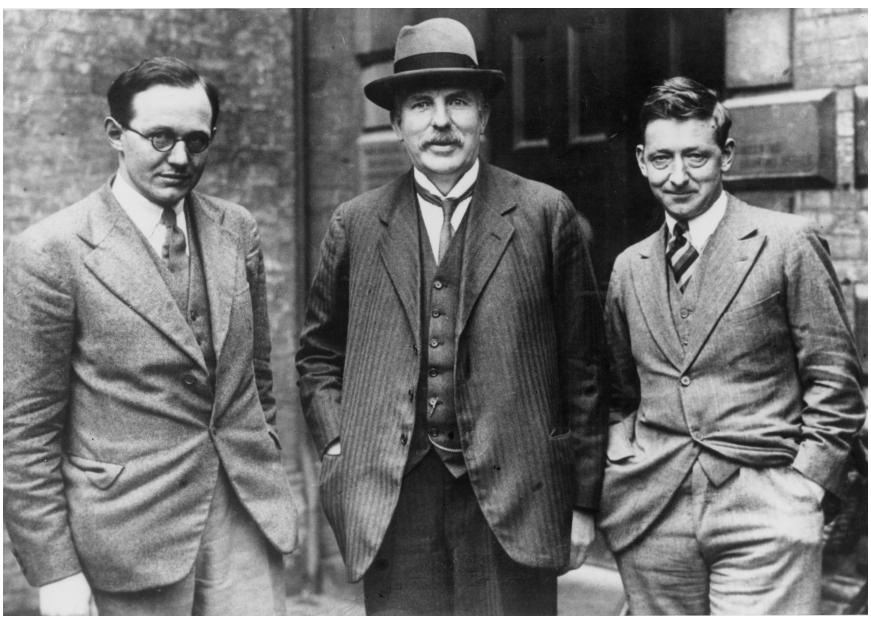

Figure 1-2 John Cockcroft, Ernest Rutherford, and E.T.S. Walton.

To penetrate the atomic nucleus, Cockcroft and Walton built a voltage multiplier that used an elaborate stack of capacitors connected by diodes acting as switches. By using only capacitors and diodes, these voltage multipliers can step up relatively low voltages to extremely high values, while at the same time being far lighter and cheaper than transformers. By activating and deactivating switches in proper sequence, they could build up a potential of more than 800 kilovolts from a transformer, acting as a primary source, generating 200 kilovolts. They used the potential to accelerate subatomic particles along an evacuated tube 8 feet long. In 1932, Cockcroft and Walton put a lithium target at the end of the tube and found that the accelerated particles successfully disintegrated a lithium nucleus into two alpha particles.

The Cockcroft-Walton multiplying circuit is shown in Figure 1-3. Three capacitors (C_A, C_B, and C_C), each of capacity C, are connected in series, and capacitor C_A is connected to the supply voltage, V_{DD}. During phase ϕ, capacitor C_1 is connected to C_A and charged to voltage V_{DD}.

When the switches change position during the next cycle, ϕ_b, capacitor C_1 will share its charge with capacitor C_B, and both will be charged to $V_{DD}/2$ if they have equal capacity. In the next cycle, C_2 and C_B will be connected and share a potential of $V_{DD}/4$, while C_1 is once again charged to V_{DD}. It is thus obvious that if this process continues for a few cycles, charge will be transferred to all the capacitors until a potential of $3V_{DD}$ is developed across the output V_{out}. In general, the switches are replaced by diodes in the actual circuit, and the clocking action is provided by an alternating voltage source, as shown in Figure 1-4.

It can be observed from Figure 1-4 that the output voltage, V_{out}, of each stage is twice the peak input voltage, V_{peak}. Hence, theoretically by using five stages, the input voltage can be stepped up by ten times. This type of circuit can actually be used to generate voltages in the order of megavolts, in some applications, by cascading a larger number of stages.

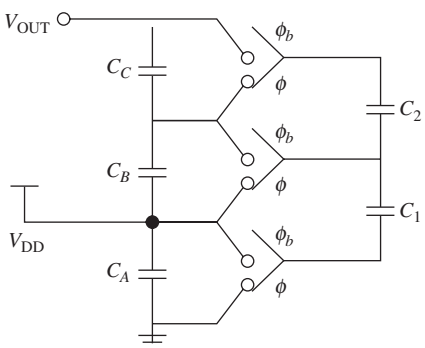

Figure 1-3 Cockcroft-Walton multiplying circuit.

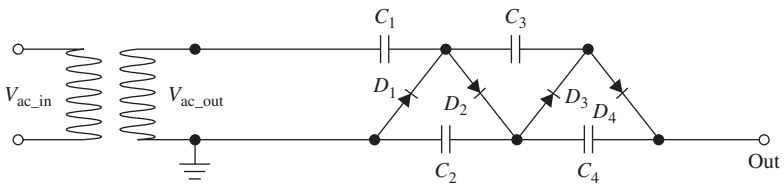

Figure 1-4 Cockcroft-Walton multiplying circuit using diodes and with a step-up transformer in the primary stage.

The Cockcroft-Walton voltage multipliers were, and still are, used in applications such as X-ray tubes, particle accelerators, electrostatic devices, and many other devices, making use of very high DC voltages.

The output voltage of the Cockcroft-Walton voltage multiplier can be expressed as

$$V_{\text{out}} = 2 \times n \times V_{\text{peak}} - V_{\text{load}} \tag{1-2}$$

where V_{load} is the drop in the output voltage when the multiplier is supplying an output current. In the absence of any output load, or at steady conditions, $V_{\text{load}} = 0$ V. Even though the number of stages, n, can be very large, efficient voltage multiplication will occur only when the coupling capacitors, C, are much greater than the stray parasitic capacitors, C_S, present at every node. The capacitive division effect in essence will reduce the voltage coupled at every stage. Further, the output impedance increases rapidly as the number of multiplying stages are increased. Because the original Cockcroft-Walton multiplier was built using discrete components, the coupling capacitors could be made sufficiently large for efficient multiplication and adequate drive capability. However, this type of multiplier does not lend itself to integration in monolithic form because, in practice, on-chip capacitors are limited to a few picofarads with relatively high values of stray capacitance to substrate.[2,3]

1.3 The Dickson Charge Pump

In order to overcome the aforementioned limitations,[4] John F. Dickson proposed a voltage multiplier circuit, shown in Figure 1-5. It operates in a similar manner as the classic Cockcroft-Walton multiplier circuit. However, the nodes of the diode chain are coupled to the inputs via capacitors in parallel, instead of in series, so that the capacitors have to withstand the full voltages developed along the chain. This is not a problem here, provided that the integrated circuit process limits are not exceeded. As will be shown later, the advantages of this configuration are that efficient multiplication can be achieved with relatively

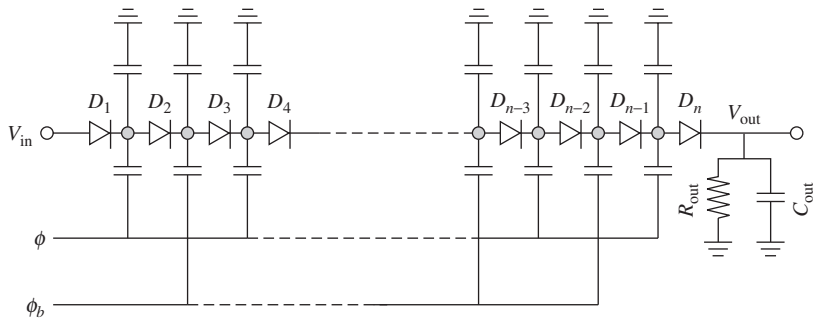

Figure 1-5 Original Dickson charge pump with diode-capacitor implementation.

high value of stray capacitances and that the current drive capability is independent of the number of multiplier stages.[5]

A practical implementation of the Dickson charge pump used in nonvolatile memories is shown in Figure 1-6. In most of the semiconductor logic process, isolated diodes are not available, and hence the multiplier chain is implemented using diode-connected MOS transistors, as shown in Figure 1-6. In this case, because NMOS transistors are used instead of diodes, the diode forward voltage, V_D, is replaced by the NMOS threshold voltage, V_t, which is a function of the node voltage of each stage.

For a few years, the basic Dickson charge pump addressed almost all different high-voltage-generation issues until the advent of submicron design technology. The continuous quest for better CMOS performance has scaled the supply voltage below 1.8 volts, and a new problem has gained the spotlight—the body effect.

1.3.1 The body effect

The threshold voltage of a NMOS transistor can be represented as

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}\right) \tag{1-3}$$

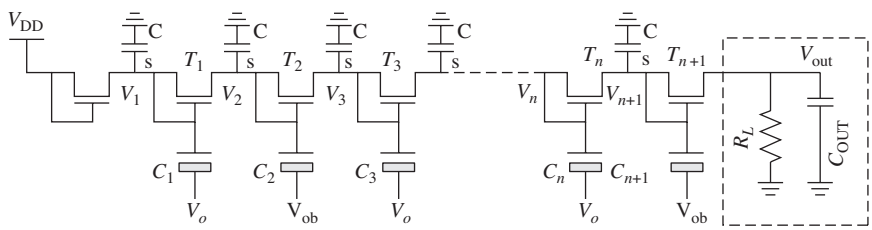

Figure 1-6 MOSFET implementation of Dickson charge pump.

where ϕ_s equals the surface potential at threshold and is represented by

$$\phi_s = 2V_t \ln \frac{N_A}{n_i} \tag{1-4}$$

γ equals the body effect coefficient and is represented by

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2q\varepsilon_{si} N_A} = \frac{\sqrt{2q\varepsilon_{si} N_A}}{C_{ox}} \tag{1-5}$$

V_{t0} equals the zero-bias threshold voltage, and V_{SB} is the source-to-body voltage bias.

It can be seen from the preceding equations that as the source voltage of a NMOS MOSFET increases, the threshold voltage of the MOSFET also rises, which results in decreased MOSFET current, I_{ds}, and hence less charge transfer takes place. The graph in Figure 1-7 shows the variation of V_{SB} versus V_t. As V_{SB} reaches above 15 V (for a particular process with V_{t0} ~ 0.08 V), the actual V_t exceeds 2.5 V, an effect that seriously diminishes the charge pump performance.

1.3.2 Implication of body effect on the Dickson charge pump

In the conventional Dickson charge pump circuit, shown earlier in Figure 1-4, the voltage gained at the nth stage is given by

$$V_n = \frac{CV_{cc}}{(C + C_s)} - V_t[V_{SB}(n)] \tag{1-6}$$

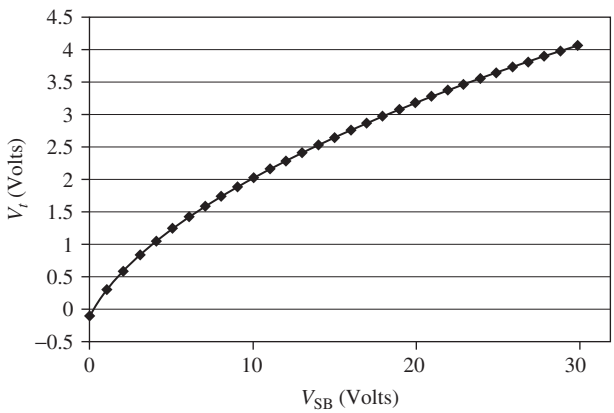

Figure 1-7 Variation of V_t with NMOS V_{SB} voltage.

where C and C_s are clock coupling capacitance and parasitic capacitance at the input node of each unit stage, respectively, V_{cc} is the clock amplitude equal to the power supply voltage, and $V_t[V_{bs}(n)]$ represents the threshold voltage of the nth NMOS transistor with a substrate bias of V_{bs}. This equation indicates that as the output voltage of each stage increases, V_n decreases due to increasing body effect. When the threshold voltage of the last stage's transistor becomes equal to $CV_{cc}/(C+C_s)$, the output voltage will not increase even with the addition of subsequent stages. Because C is much larger than C_s in typical conditions, the maximum output voltage (V_{max}) obtained by a conventional charge pump is given by

$$V_{max} = \left(\frac{V_{cc} - V_{t0}}{\gamma} + \sqrt{2\Phi_F} \right)^2 - 2\Phi_F \tag{1-7}$$

where V_{t0} is the zero-bias threshold voltage, γ is the body effect coefficient, and Φ_F is the substrate's Fermi potential. Evidently, it can be interpreted from equation 1-7 that as the supply voltage, V_{cc}, is lowered below about 2 V, the threshold voltage of the device will start to dominate the output voltage and hence it will limit the maximum output voltage.[6–8]

1.4 Better Solutions

Several methods have been proposed—such as the 4-phase charge pump, the modified 4-phase charge pump, the boosted pump clock scheme, a CTS scheme, and several hybrid versions of these combinations—to get around problems of V_t dependence and to increase the circuit efficiency for chips operating below 2.5 V supply voltages.

In the conventional 4-phase charge pumps, the pumping gain can be increased by increasing the source to gate voltage drop using the special 4-phase clocks, so the gain degradation due to threshold voltage can be alleviated. Also a 2x–4x boosted pump clock source is often used as an easy way to increase efficiency and obtain higher output voltages.

In the CTS scheme, an additional pass transistor is added for each stage; the gate of the pass transistor is controlled by the next stage voltage, which is in opposite phase. Subsequent chapters in this book describe in detail each scheme, along with its advantages and disadvantages.

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