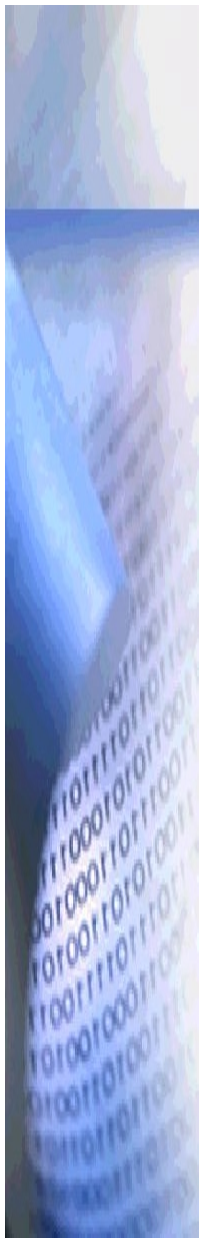


School of Electronic and Communications Engineering

Phase-Locked Loops (PLL)

Recommended Text: Gray, P.R. & Meyer. R.G., Analysis and Design of Analog Integrated Circuits (3rd Edition), Wiley (1992) pp. 681-698

Introduction

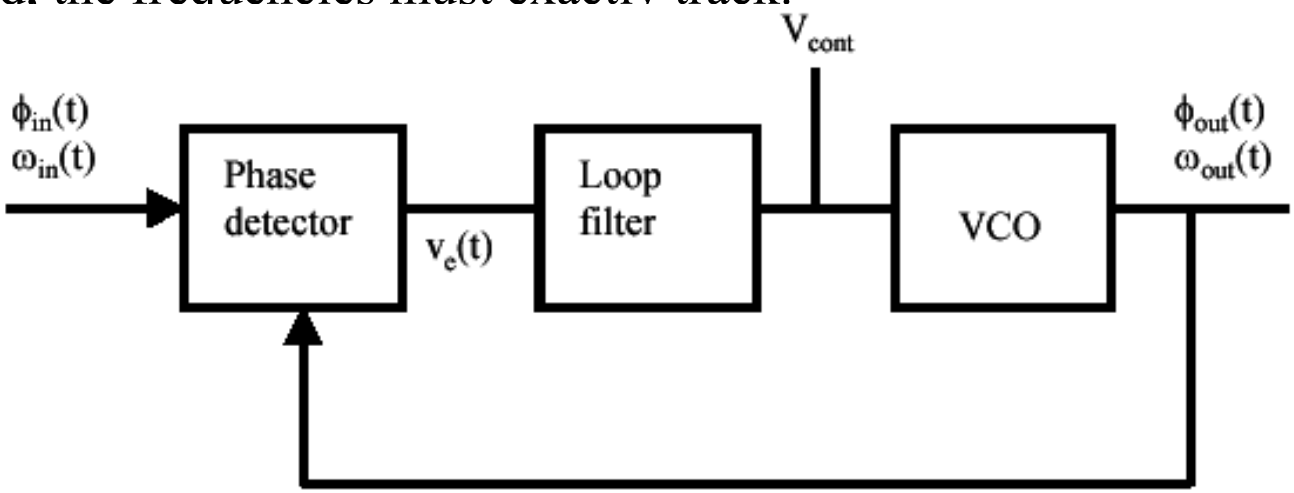
- The phase-locked loop concept was first developed in the 1930s.[4]
- It has since been used in communications systems of many types, particularly in satellite communications systems.
- Until recently, however, phase-locked systems have been too complex and costly for use in most consumer and industrial systems, where performance requirements are more modest and other approaches are more economical.
- The PLL is particularly amenable to monolithic construction, however, and integrated-circuit phase-locked loops can now be fabricated at very low cost.
- Their use has become attractive for many applications such as FM demodulators, stereo demodulators, tone detectors, frequency synthesizers, and others.

Definition

- A PLL is a feedback system that includes a
1. Voltage–Controlled Oscillator (VCO),
2. phase detector, and
3. low pass filter within its loop.

$$\phi_{out}(t) = \phi_{in}(t) + const.$$
$$\omega_{out}(t) = \omega_{in}(t)$$

- Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock.
- The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked. the frequencies must exactly track.



- The PLL output can be taken from either

1. V_{cont}, the filtered (almost DC) VCO control voltage, or
2. from the output of the VCO depending on the application.

- The former provides a baseband output that tracks the phase variation at the input.
- The VCO output can be used as a local oscillator or to generate a clock signal for a digital system.
- Either phase or frequency can be used as the input or output variables.
- Of course, phase and frequency are interrelated by:

$$\omega(t) = \frac{d\varphi}{dt} \quad \text{and} \quad \varphi(t) = \varphi(0) + \int_0^t \omega(t')dt'$$

Applications:

- There are many applications for the PLL:

1. a. FM demodulator
2. b. Frequency synthesizer
3. c. Clock generation

- You should note that there will be different input and output variables and different design criteria for each case,
- but you can still use the same basic loop topology and analysis methods.

Phase detector:

- **Phase detector** compares the phase at each input and generates an error signal, $v_e(t)$, proportional to the phase difference between the two inputs. KD is the gain of the phase detector (V/rad).

$$v_e(t) = K_D\left(\varphi_{out}(t) - \varphi_{in}(t)\right)$$

- As one familiar circuit example, an analogue multiplier (Gilbert cell) can be used as a phase detector.
- Recall that the mixer takes the product of two inputs. $v_e(t) = A(t)B(t)$. If,

$$A(t) = A\cos\left(\omega_0 t + \varphi_A\right) \text{ and } B(t) = B\cos\left(\omega_0 t + \varphi_B\right)$$
$$A(t)B(t) = AB\cos\left(\omega_0 t + \varphi_A\right)\cos\left(\omega_0 t + \varphi_B\right) =$$
$$\left(AB/2\right)\left[\cos\left(2\omega_0 t + \varphi_A + \varphi_B\right) + \cos\left(\varphi_A - \varphi_B\right)\right]$$

$$v_e(t) = (AB/2)[\cos(2\omega_0 t + \varphi_A + \varphi_B) + \cos(\varphi_A - \varphi_B)]$$

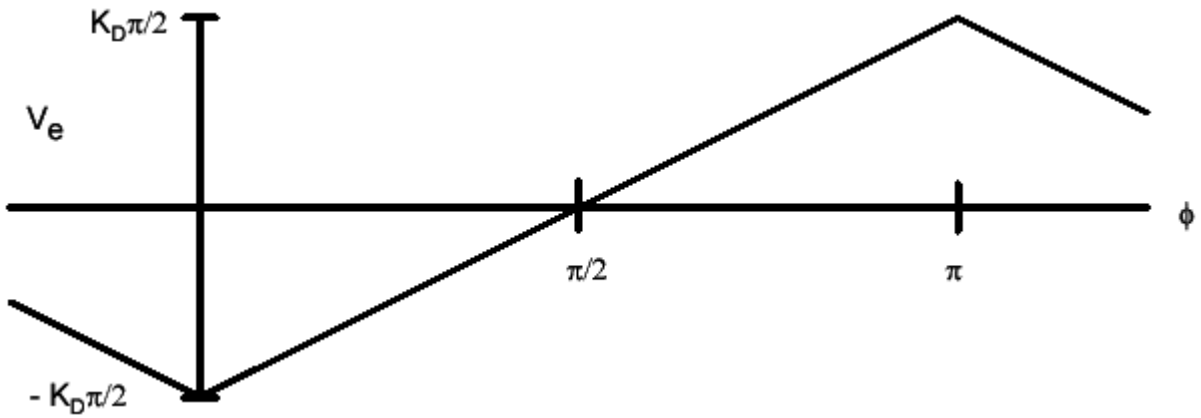
- Since the two inputs are at the same frequency when the loop is locked, we have:

1. one output at twice the input frequency and
2. an output proportional to the cosine of the phase difference.

- The doubled frequency component must be removed by the lowpass loop filter.
- Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.

Transfer Characteristic

- The averaged transfer characteristic of such a phase detector is shown below.



- Note that in many implementations, the characteristic may be shifted up in voltage (single supply/single ended).
- If the phase difference is π /2, then the average or integrated output from the XOR-type phase detector will be zero (or $V_{DD}/2$ for single supply, digital XOR).
- The slope of the characteristic in either case is K_D.

Voltage-Controlled Oscillator (VCO)

- In PLL applications, the VCO is treated as a linear, time-invariant system.
- Excess phase of the VCO is the system output.

$$\varphi_{out} = K_O \int_{-\infty}^{t} V_{cont}\, dt'$$

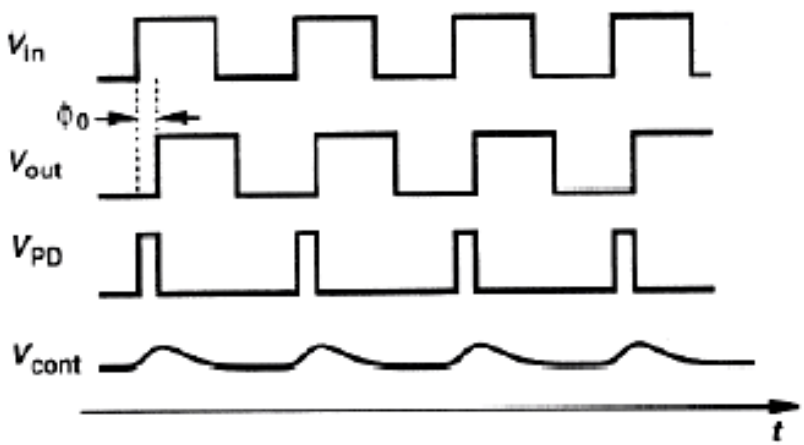
- The VCO oscillates at an angular frequency, ω_{out}. Its frequency is set to a nominal ω_0 when the control voltage is zero.
- Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient K_O or K_{VCO} (rad/s/v).

$$\omega_{out} = \omega_O + K_O V_{cont}$$

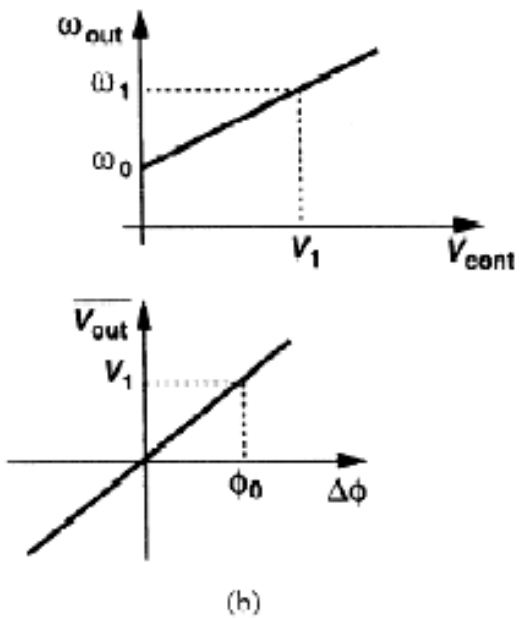
- Thus, to obtain an arbitrary output frequency (within the VCO tuning range), a finite V_{cont} is required.
- Let's define $\varphi_{out} - \varphi_{in} = \Delta\varphi$.

VCO (cont.)

- In the figure below, the two inputs to the phase detector are depicted as square waves.
- The XOR function produces an output pulse whenever there is a phase misalignment.
- Suppose that an output frequency ω_1 is needed. From the upper right figure, we see that a control voltage V1 will be necessary to produce this output frequency.



(a)



(b)

VCO (cont.)

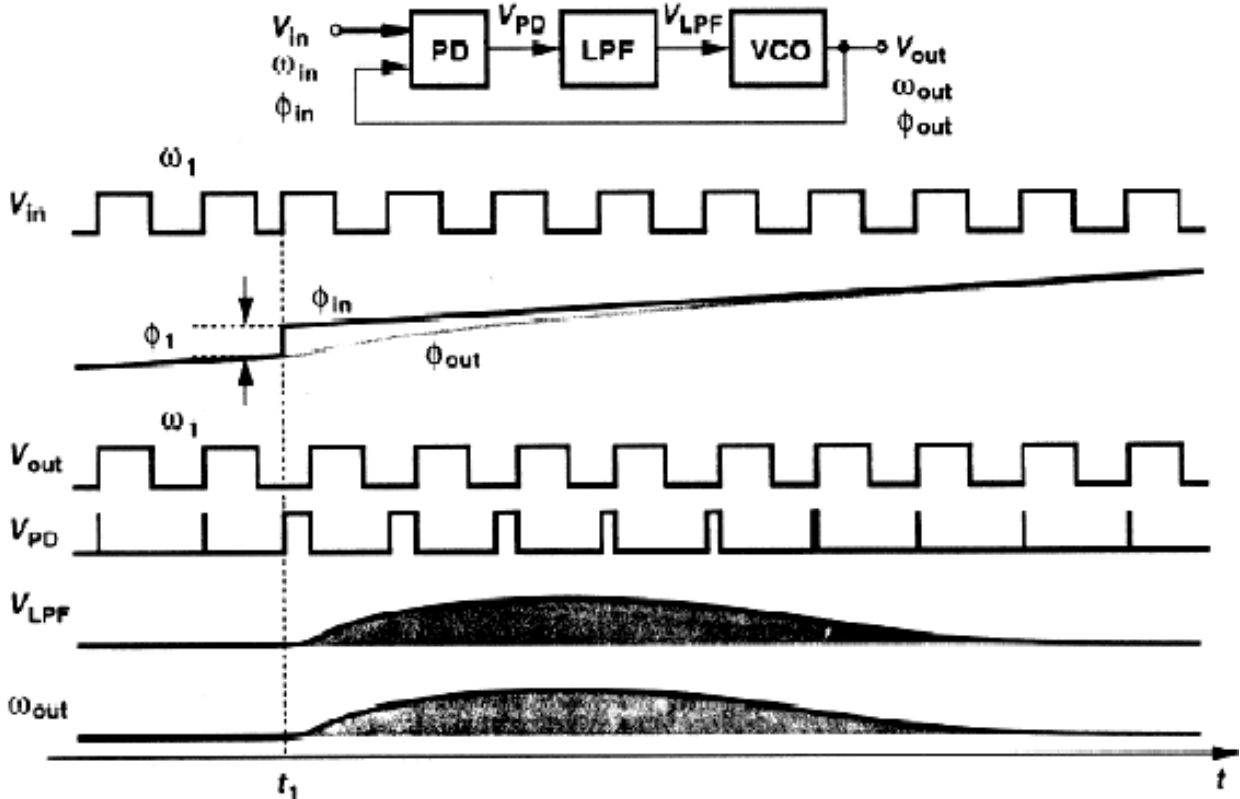
- The phase detector can produce this V1 only by maintaining a phase offset φ_0 at its input.
- In order to minimize the required phase offset or error, the PLL loop gain, $K_D K_O$, should be maximized, since

$$\varphi_0 = \frac{V1}{K_D} = \frac{\omega_1 - \omega_0}{K_D K_O}$$

- Thus, a high loop gain is beneficial for reducing phase errors.

PLL dynamic response

- To see how the PLL works, suppose that we introduce phase step at the input at t = t1. So that, $\varphi_{in} = \omega_1 t + \varphi_0 + \varphi_1 u(t - t_1)$
- Since we have a step in phase, it is clear that the initial and final frequencies must be identical: ω 1.
- But, a temporary change in frequency is necessary to shift the phase by f1.



Dynamic Response ($\Delta\varphi$)

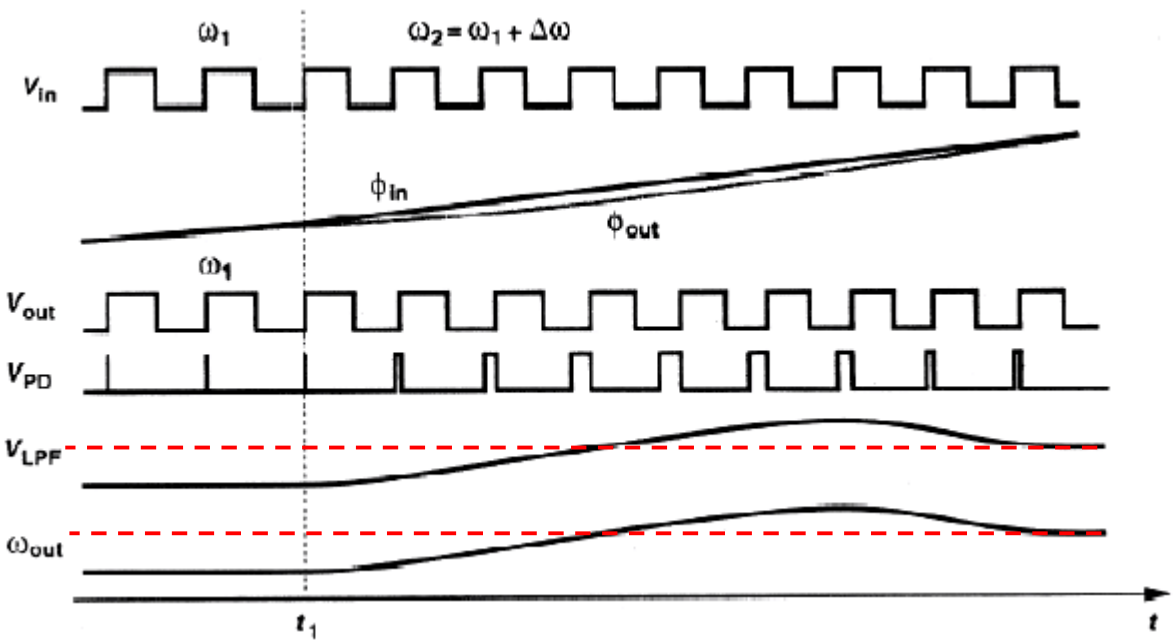
- The area under ω_{out} gives the additional phase because V_{cont} is proportional to frequency.

$$\varphi_1 = \int_{t1}^{\infty} \omega_{out}\, dt = \int_{t1}^{\infty} K_O V_{cont}(t)\, dt$$

- After settling, all parameters are as before since the initial and final frequencies are the same.
- This shows that $V_{cont}(t)$ can be used to monitor the dynamic phase response of the PLL.

Dynamic Response ($\Delta\omega$.)

- Now, let's investigate the behaviour during a frequency step: $\varphi_2=\varphi_1+\Delta\varphi$
- The will cause the phase difference to grow with time
- This in turn causes the control voltage, V_{cont}, to increase, moving the frequency step will cause the phase difference to grow with time since a frequency step is a phase ramp.
- This in turn causes the V_{cont}, to increase, moving the VCO frequency up to catch up with the input reference signal.



In this case, we have a permanent change in ω_{out} since a higher V_{cont} is required to sustain a higher ω_{out}.

If the frequency step is too large, the PLL will lose lock.

PLL in Locked Condition

- **Approach**: We will discuss the details of phase detectors and loop filters as we proceed.
- But, at this point, we will treat the PLL as a linear feedback system.
- We assume that it is already "locked" to the reference signal, and examine how the output varies with the loop transfer function and input.
- A frequency domain approach will be used, specifically describing transfer functions in the s-domain.

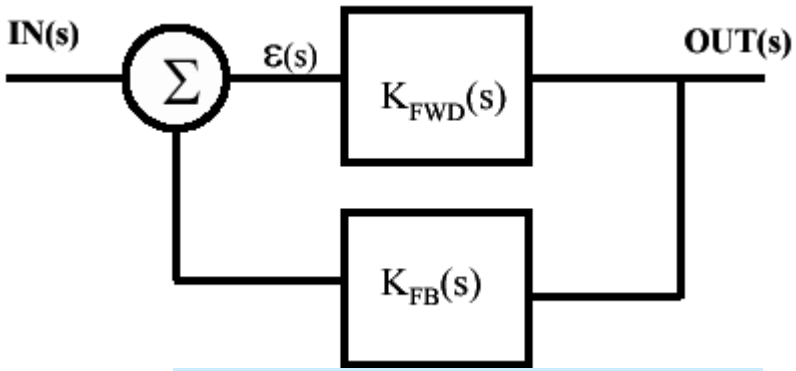
$$V_e(s)/\Delta\varphi = K_D \quad \text{and} \quad \varphi_{out}(s)/V_{cont}(s) = K_O/s$$

- Note that the VCO performs an integration of the control voltage and thus provides a factor of 1/s in the loop transfer function.
- Because of this, a PLL is always at least a first order feedback system.

PLL as Feedback System.

- **Loop Gain:** $T(s) = K_{FWD}(s)K_{FB}(s)$
- **Transfer Function:**

$$\frac{OUT(s)}{IN(s)} = H(s) = \frac{K_{FWD}(s)}{1+T(s)}$$

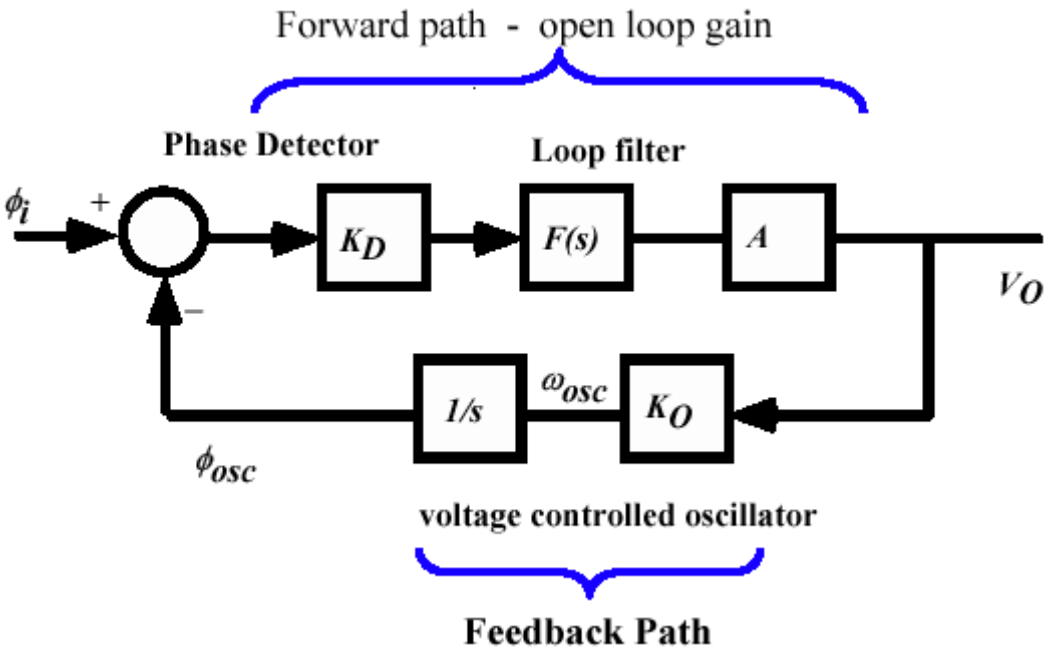


- The Loop gain can be described as a polynomial: $T(s) = \frac{K'(s+a)(s+b)\cdots}{s^n(s+\alpha)(s+\beta)\cdots}$
- **ORDER** = the order of the polynomial in the denominator
- **TYPE** = n (the exponent of the s factor in the denominator)
- **PHASE ERROR** $\varepsilon(s) = IN(s)/[1+T(s)]$
- **STEADY STATE ERROR** $\varepsilon_{SS} = \lim_{s\to 0}[s\varepsilon(s)] = \lim_{t\to\infty}\varepsilon(t)$
- SS error is a characteristic of feedback control systems.
- This is the error remaining in the loop at the phase detector output after all transients have died out. Large loop gain leads to small errorr

PLL as a first-order filter

The closed-loop gain transfer function is given by

$$\frac{V_O}{\varphi_i} = \frac{K_D F(s) A}{1 + K_D F(s) A \cdot (K_O / s)}$$



Assuming

$$\omega_i = \frac{d\varphi_i}{dt} \quad \text{then} \quad \omega_i = s\varphi_i(s)$$

The transfer function in terms of frequency variations therefore can be expressed as:

$$\frac{V_O}{\omega_i} = \frac{1}{s}\frac{V_O}{\varphi_i} = \frac{K_D F(s) A}{s + K_D F(s) A \cdot K_O}$$

Assuming that LP is removed and $K_v = K_O K_D A$, hence

$$\frac{V_O}{\omega_i} = \frac{K_v}{s + K_v}\frac{1}{K_O}$$

Thus the loop inherently produces a first order low-pass transfer characteristic

PLL as a first-order filter

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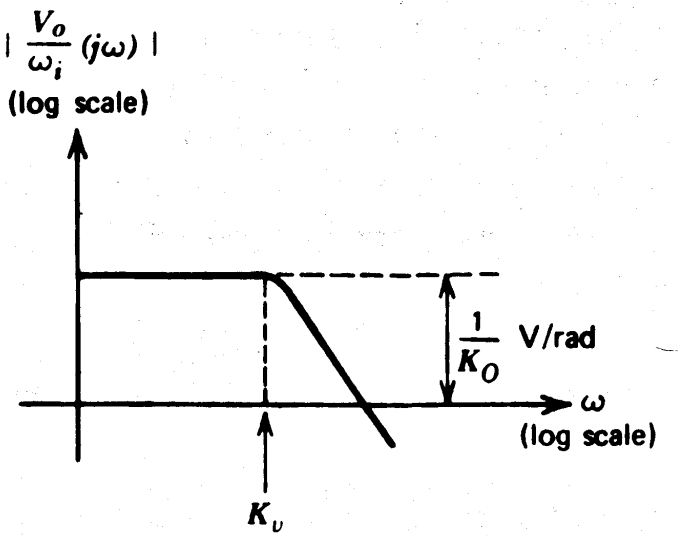
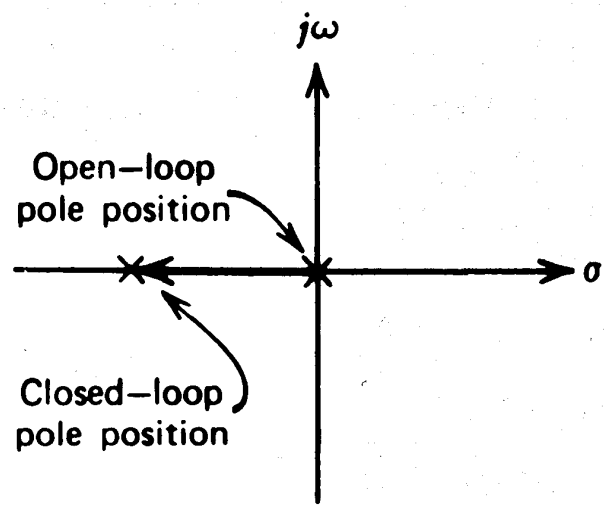




Example

- A PLL has a *Ko* of 2π (1kHz/V), a K_v of 500 s^{-1} and a free-running frequency of 500Hz. Find V_O for a constant input signal frequency of 250 Hz and 1 kHz
- Sketch the response of V_O

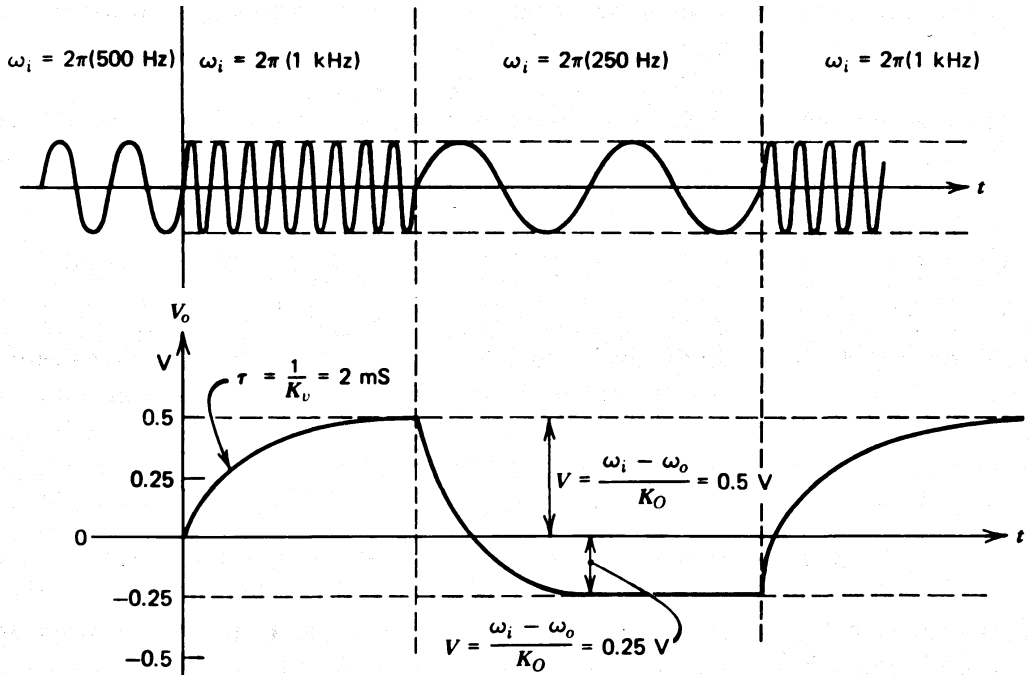
$$V_O = (\omega_i - \omega_o)/K_O$$

- At 250 Hz ,

$$V_O = \left(2\pi(250) - 2\pi(500)\right)/2\pi(1kHz/V) = -0.25V$$

- At 500 Hz

$$V_O = \left(2\pi(1000) - 2\pi(500)\right)/2\pi(1kHz/V) = 0.5V$$



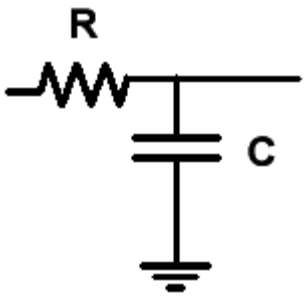
PLL as a first-order filter

- This example shows that PLL can operate with no loop filter
- Nevertheless it has several practical drawbacks.
- Since the phase detector is really a multiplier, it produces a sum frequency component at its output as well as the difference frequency component.
- This component at twice the carrier frequency will be fed directly to the output if there is no loop filter.
- Also, all the out-of-band interfering signals present at the input will appear, shifted in frequency, at the output.
- Thus, a loop filter is very desirable in applications where interfering signals are present.

Second-order PLL

- The most common configuration for integrated circuit PLLs is the second-order loop.
- Here, loop filter *F(s)* is simply a single-pole, low-pass filter, usually realized with a single resistor and capacitor. Thus

$$F(s) = \frac{1}{1 + s/\omega_1}$$



- Substituting this into

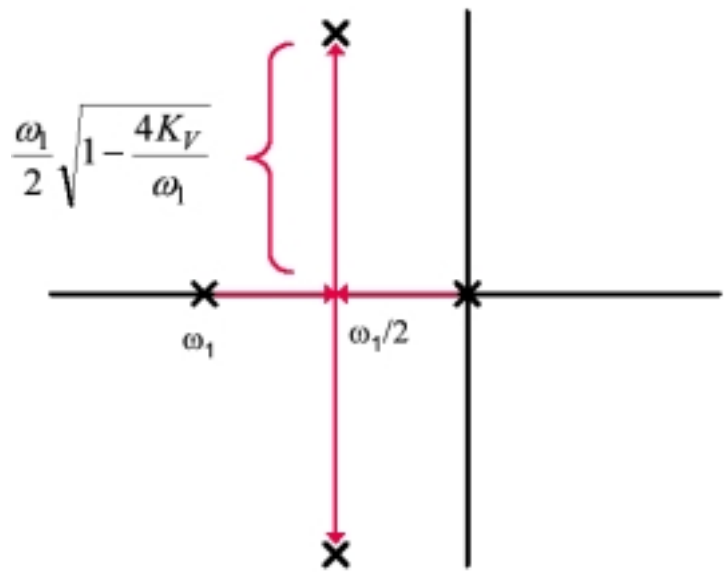
$$\frac{V_O}{\omega_i} = \frac{1}{s}\frac{V_O}{\varphi_i} = \frac{K_D F(s) A}{s + K_D F(s) A \cdot K_O}$$

- It gives:

$$\frac{V_O}{\omega_i} = \frac{1}{K_O}\frac{1}{1 + s/K_v + s^2/\omega_1 K_v}$$

- The roots of this transfer function are

$$s_{1,2} = -\frac{\omega_1}{2}\left(1 \pm \sqrt{1 - \frac{4K_v}{\omega_1}}\right)$$



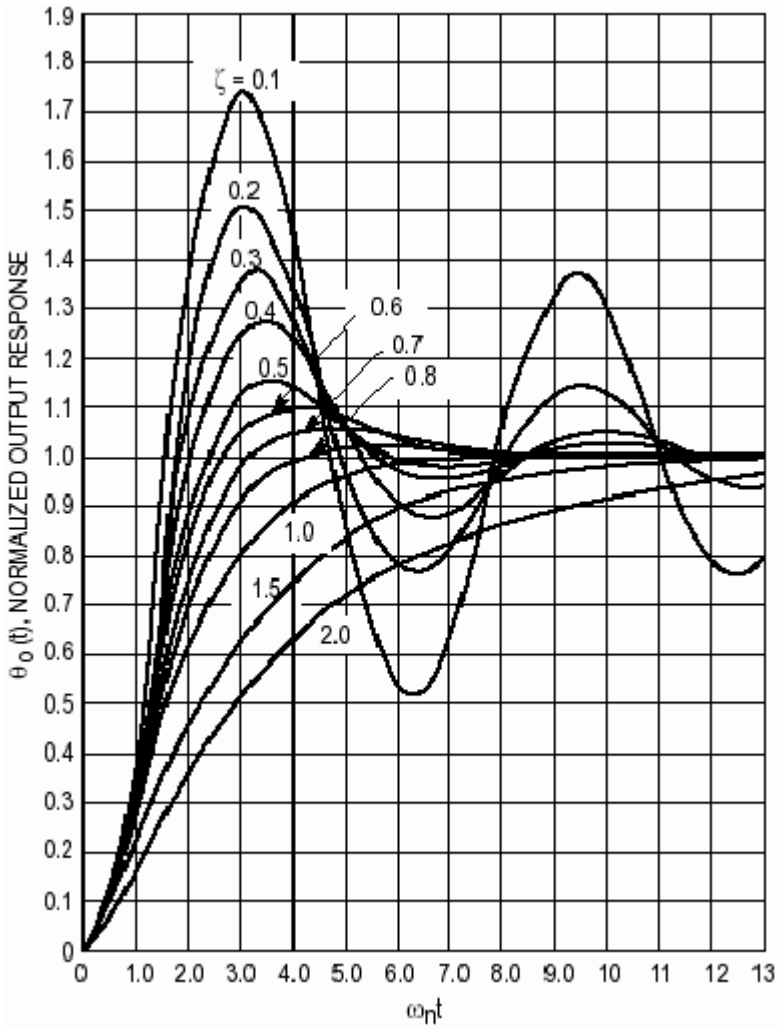
Damping Factor

- This transfer function
- an be also expressed as:
- $$\frac{V_O}{\omega_i} = \frac{1}{K_O} \frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n} s + 1}$$

$\omega_n = \sqrt{\omega_1 K_v}$ is crossover frequency

$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_v}}$ is damping factor

- We can have a very underdamped response when $\omega_1 << K_V$.
- Think about the inverse Laplace transform of the complex conjugate pole pair.



- The inverse Laplace transform of the complex conjugate pole pair.

$$s_{1,2} = -\frac{\omega_1}{2}\left(1 \pm \sqrt{1 - \frac{4K_v}{\omega_1}}\right)$$

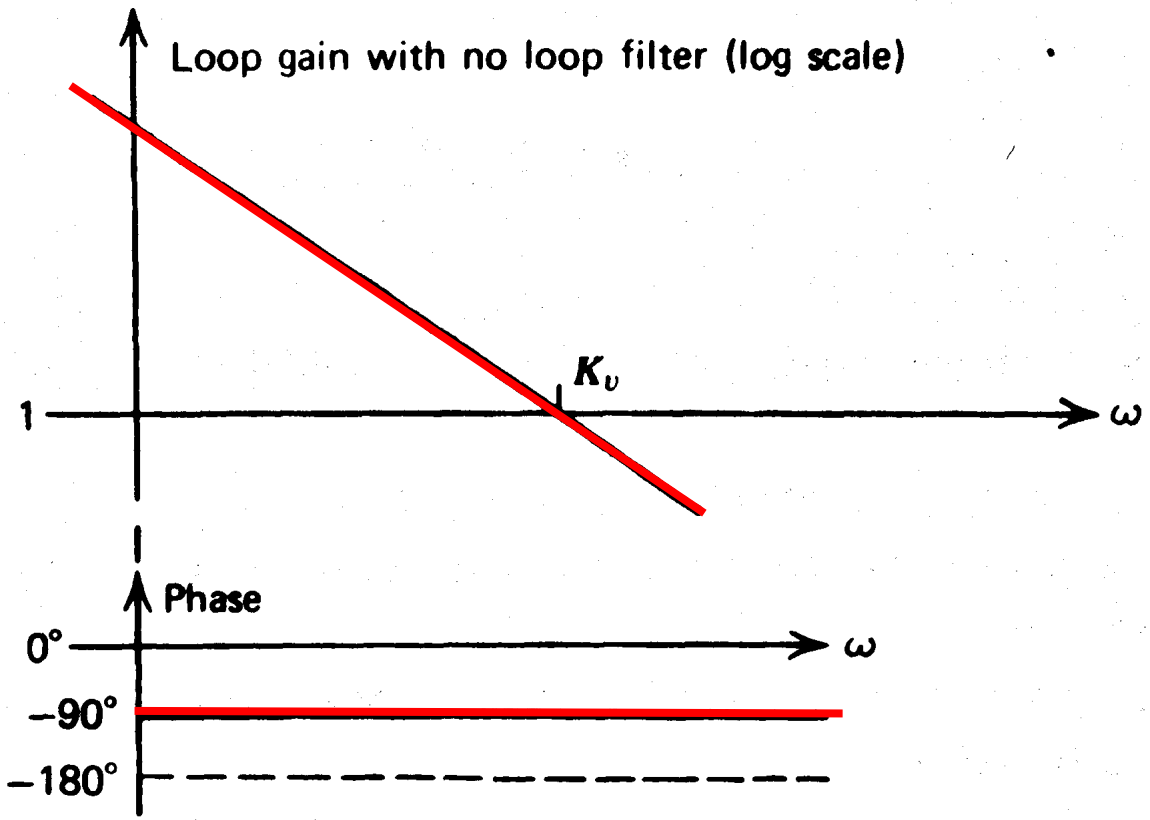
- Gives

$$v(t) = e^{-\frac{\omega_1 t}{2}} \sin\left(\frac{\omega_1}{2}\sqrt{1 - \frac{4K_v}{\omega_1}}\right)t$$

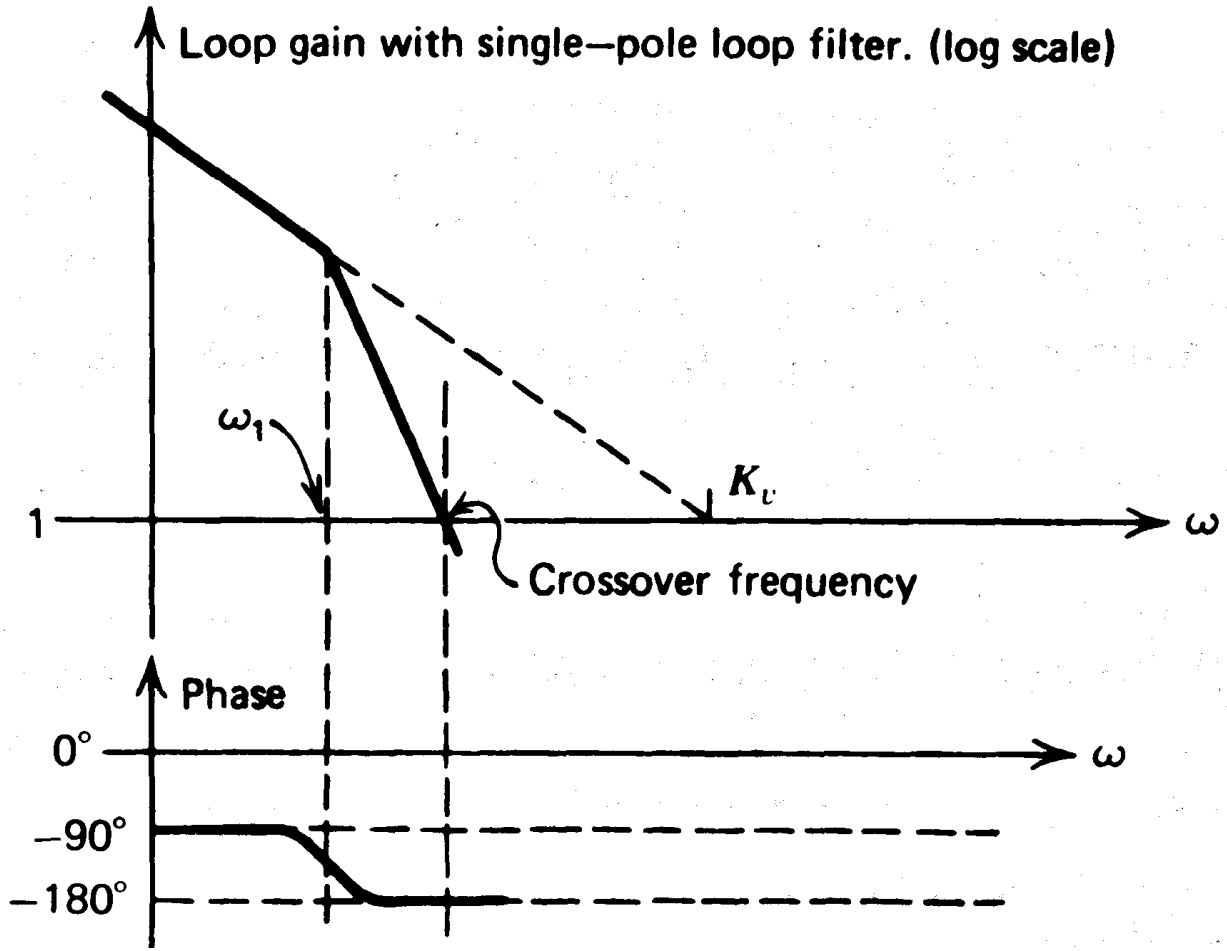
- A good compromise is using a maximally flat low-pass pole configuration in For this response, the damping factor should be equal to $1/\sqrt{2}$
- Thus

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_v}} = \frac{1}{\sqrt{2}} \text{ and } \omega_1 = 2K_v$$

PLL open-loop response with no loop filter



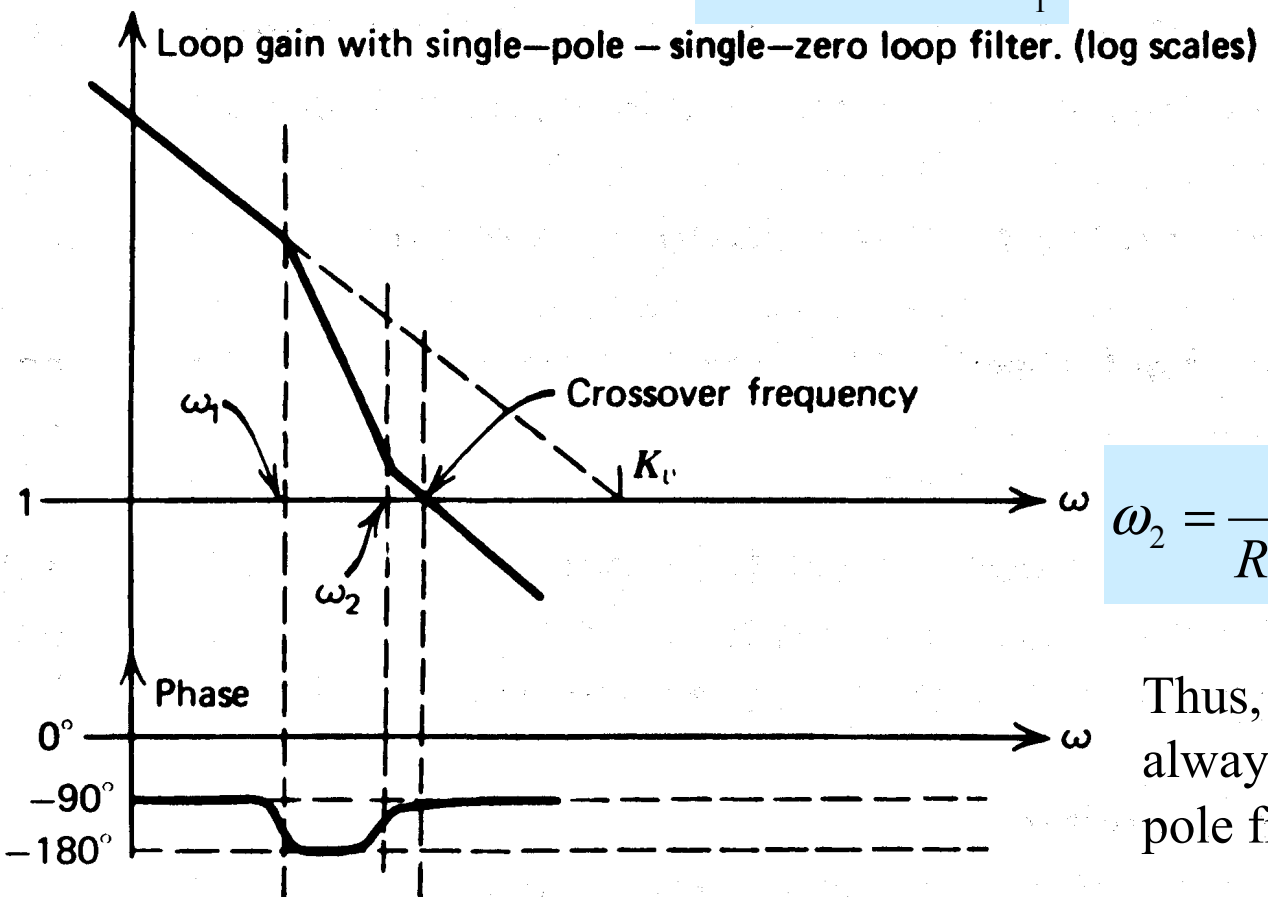
PLL open-loop response with a single-pole filter

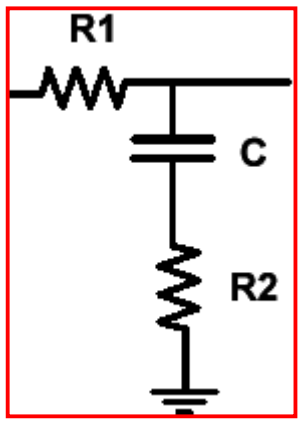


PLL open-loop response with zero added in loop filter

- Adding a resistor to the lowpass loop filter contributes a zero to its transfer function

$$F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$$





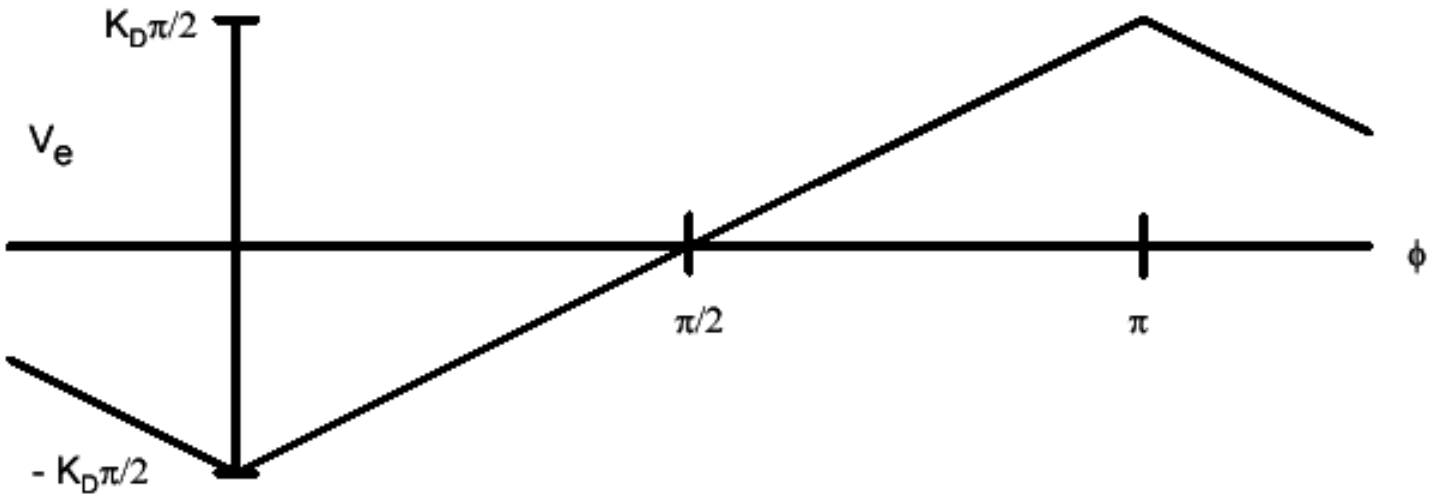
$$\omega_2 = \frac{1}{R_2 C}$$

$$\omega_1 = \frac{1}{(R_1 + R_2)C}$$

Thus, the zero frequency is always higher than the pole frequency, $\omega_2 > \omega_1$.

Lock Range

- **Lock Range**. Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the
- (a) phase detector or
- (b) the VCO frequency range.
- If limited by phase detector: $0 < \varphi < \pi$ is the active range where lock can be maintained.



Lock Range

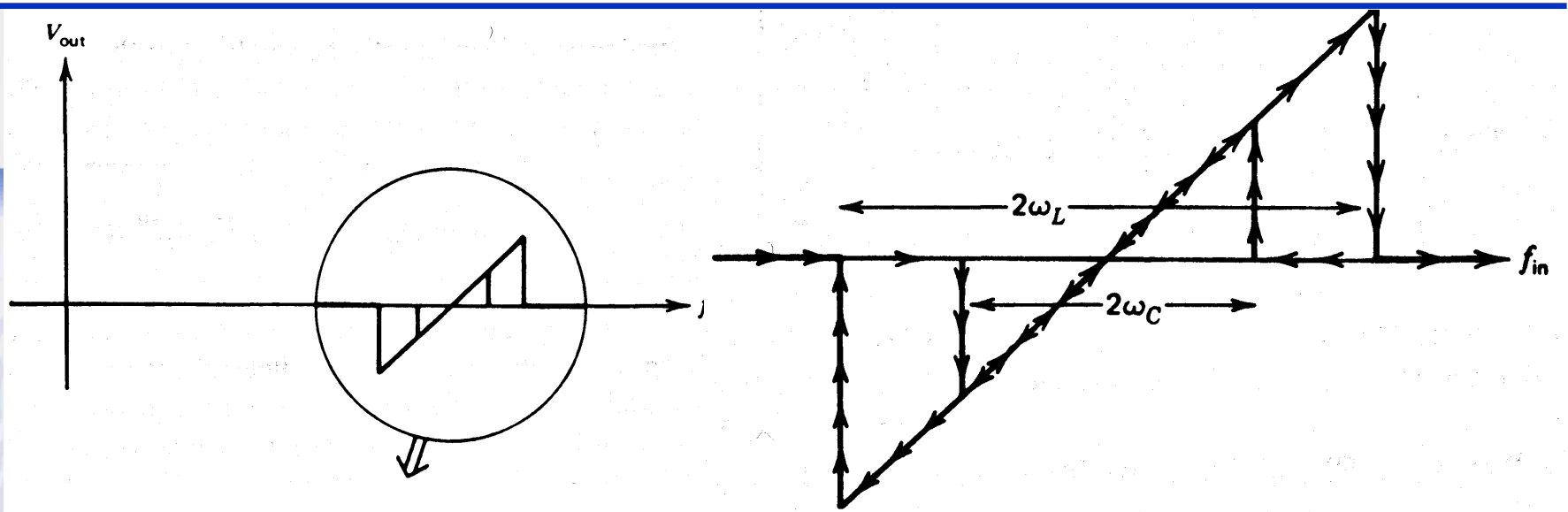
- For the phase detector type shown (Gilbert multiplier or mixer), the voltage vs. phase slope reverses outside this range.
- Thus the frequency would change in the opposite direction to that required to maintain the locked condition. $V_{e\text{-}max} = \pm K_D \pi /2$
- When the phase detector output voltage is applied through the loop filter to the VCO, $\Delta\omega_{out-max} = \pm K_V \pi /2 = \omega_L$ (lock range)
- where $K_V = K_O K_D$, the product of the phase detector and VCO gains.
- This is the frequency range around the free running frequency that the loop can track.
- Doesn't depend on the loop filter
- Does depend on DC loop gain

- b. The lock range could also be limited by the tuning range of the VCO.
- Oscillator tuning range is limited by capacitance ratios or current ratios and is finite. In many cases, the VCO can set the maximum lock range.

Capture Range

- **Capture range:** Range of input frequencies around the VCO centre frequency onto which the loop will lock when starting from an unlocked condition.
- The capture range is the range of input frequencies for which the initially unlocked loop will lock on an input signal and is always less than the lock range.
- the capture range is difficult to predict analytically. As a very rough rule of thumb, the approximate capture range can be estimated using the following procedure:
- When the input frequency is swept through a range around the center frequency, the output voltage as a function of input frequency displays a hysteresis effect.

Capture Range



- Assume that the loop is opened at the loop-amplifier output and that a signal with a frequency not equal to the free-running VCO frequency is applied at the input of the PLL.
- The sinusoidal *difference* frequency component that appears at the output of the phase detector has the value

$$V_p(t) = \frac{\pi}{2} K_D \cos(\omega_i - \omega_{ocs})t$$

Capture Range

- The output from the loop amplifier thus consists of a sinusoid at the difference frequency whose *amplitude* is reduced by the loop filter.
- This component is passed through the loop filter, and the output from the loop amplifier resulting from this component is

$$V_o(t) = \frac{\pi}{2} K_D A \cdot \left| F\left(j(\omega_i - \omega_{ocs})\right) \right| \cdot \cos\left((\omega_i - \omega_{ocs})t - \varphi\right)$$

where φ is $\varphi = \angle F\left(j(\omega_i - \omega_{ocs})\right)$

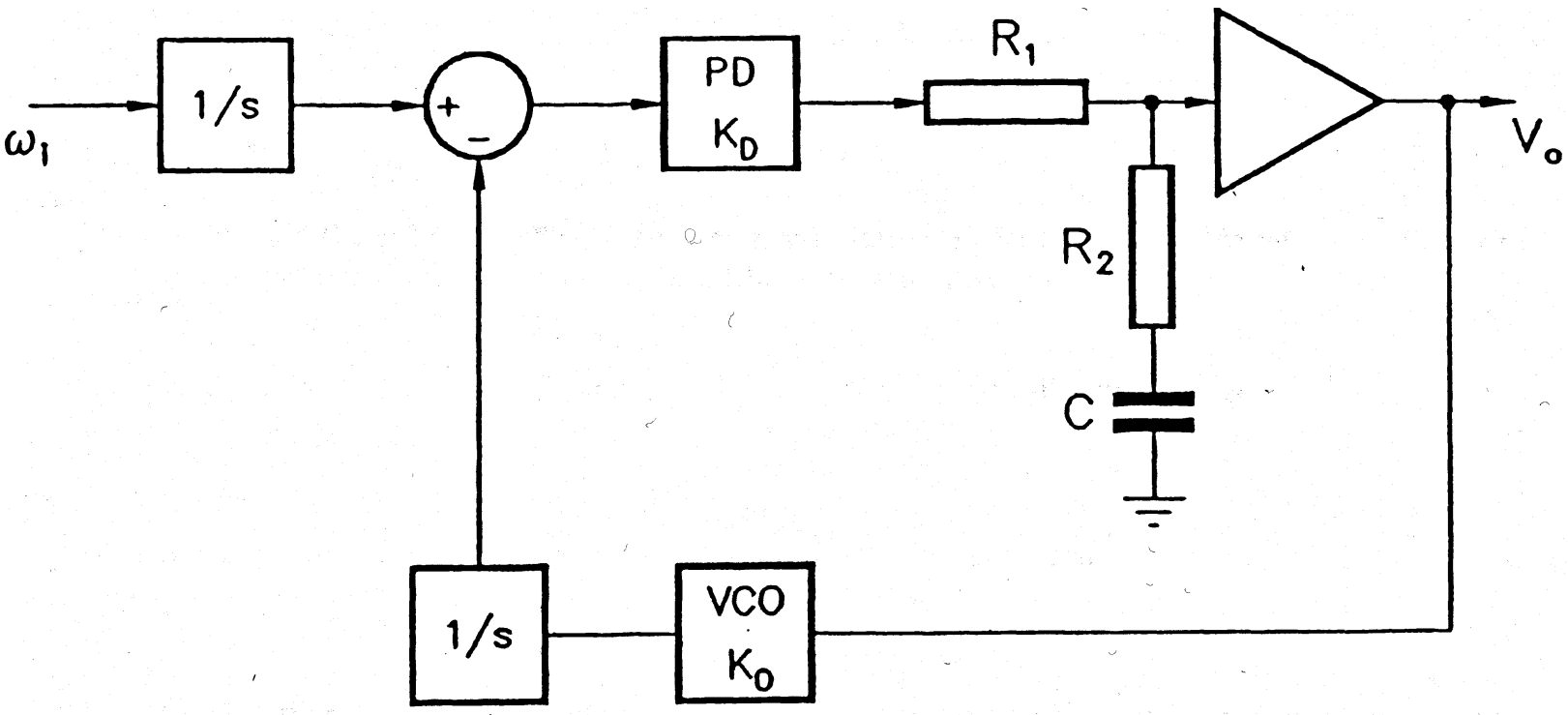
- In order for capture to occur, the magnitude of the voltage that must be applied to the **VCO** input is $V_{osc}(t) = \dfrac{\omega_i - \omega_{ocs}}{K_O}$
- Capture is likely to occur when $V_{osc}(t) < V_o(t)$ Therefore:

$$\omega_i - \omega_{ocs} < \frac{\pi}{2} \cdot K_D K_O A \cdot \left| F\left(j(\omega_i - \omega_{ocs})\right) \right|$$

- Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

Typical Question

- The 2nd-order phase-locked loop (PLL) system illustrated in Fig. 2 contains sub-elements with corresponding gain values as shown in Table 1. The amplifier gain may be assumed to be constant.



Typical Question

Table of Gains

Component	Symbol	Value	Units
Phase Detector	K_D	50	volts/radian
VCO	K_O	10^6	Radians/sec/volt
Amplifier	A	20	dB

- Given loop-filter component values R_1 = 5.6 kΩ, R_2 = 330 Ω and C = 1 nF, sketch
- (a) the asymptotic closed-loop (Vo/ω_1) PLL frequency response and estimate the banbwidth and
- (b) the asymptotic loop-gain response and graphically or otherwise, determine the 0 dB intercept frequency