Performance study of CMOS power amplifiers.

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Abstract

A program is written to design and analyse low voltage Class E power amplifiers. Some recently published Class E amplifiers will be used to verify the program. After this step some new insides will be given. One of the major conclusions will be that the resistance in the DC feed inductor must be incorporated in the design process. This will lead to better power amplifiers in the future, which can work at higher frequencies, higher output powers and higher efficiencies.

1. Introduction

Today's models used to analyse Class E power amplifiers, are far from perfect. A Class E amplifier is in most cases modelled as a set of differential equations. To solve this set of differential equations various methods can be used. Each of the methods have their difficulties, and this leads to the fact that all the models published ignore some important imperfections of the Class E amplifier. One important non-ideality, which has always been omitted until now, is the parasitic resistance of the DC-feed. The reason for excluding this non-ideality is a consequence of following inaccurate assumption: the RMS current flowing through the parasitic resistance of the DC-feed results in a voltage drop. This voltage drop lowers the DC voltage seen by the drain of the CMOS switch, lowering the output power. This modified output power was used to calculate the drain efficiency, still assuming that Class E conditions results in maximum drain efficiency.

In an actual case the on resistance of the switch and the parasitic loss resistance of the DC-feed are of the same magnitude. From paper [1] it was proven that the on-resistance influences the design of the Class E power amplifier. This means that the DC-feed resistance must also have repercussions on the design of Class E power amplifiers. In figure 1 a representation of a switching Class E power amplifier, with losses, is shown. In a general case, correct values for the excess inductance Lx and the shunt capacitance Cshunt are given by:

$$Lx = 1{,}15R/\omega_c \quad (1)$$

$$Cshunt = 0{,}1836/(\omega_c.R) \quad (2)$$

For these values the well-known Class E conditions apply, and the off to on losses are absent. The resistance R used in (1) and (2), is the target load resistance. This target load resistance sets the output power:

$$Pout(R) = \frac{0.576.Vdd^2}{R} \quad (3)$$

For high output powers this resistance is in the order of a few Ohms. To convert the target resistance to the 50 Ohm impedance of the antenna an up-conversion network must be used.

In most CMOS designs, bonding wires are used as inductors [Mert., Tsai, Yoo, Su]. The parasitic resistance and inductance value are proportional to the length. As a consequence the DC-feed inductor must be small, otherwise the voltage drop over this resistance becomes too large. So, our Class E model must be capable of using a lossy DC-feed with finite value. Also, the losses in the matching network and the Ron resistance of the switch must be dealt with. This makes the model quite complex and the most convenient way to solve the differential equations, is to use numerical methods provided by a mathematical program.

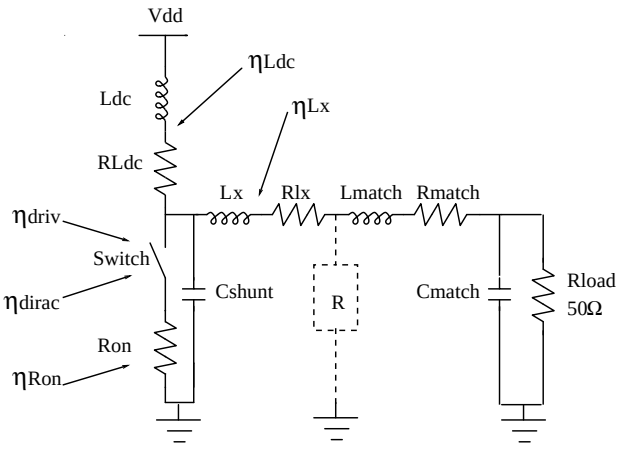

Fig. 1: Class E amplifier model with losses

2. Design guidelines for an ideal Class E P.A.

In figure 2 and 3, the output power and drain efficiency variation curves are shown for Class E designs with different DC-feeds. The X-axis refers to the target load resistance R of figure 1. From figure 2 and 3 some general observations and conclusions can be drawn.

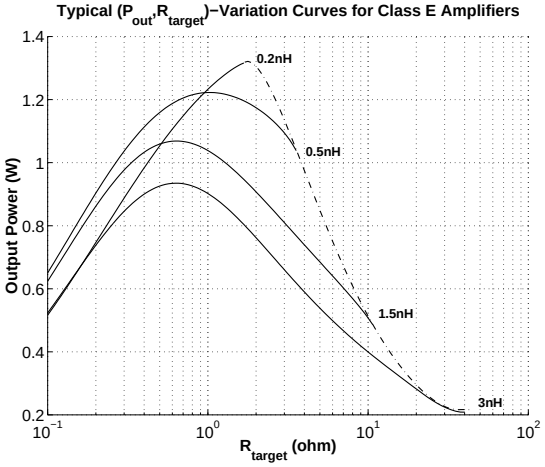

Fig. 2:Pout vs. Rtarget for different DC-feeds

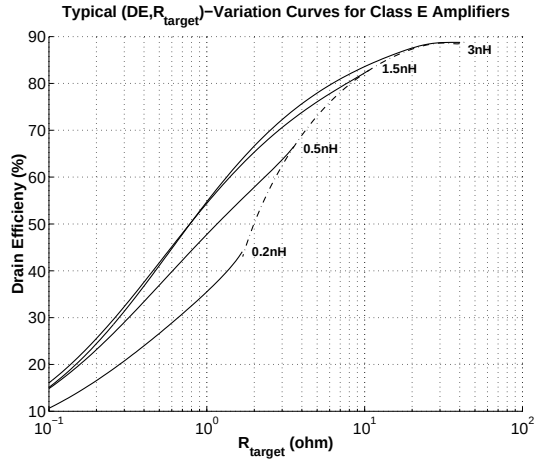

Fig. 3:PAE vs. Rtarget for different DC-Feeds

For a target load resistance less than 1 Ω, a high output power can be achieved. However, a strong decline in drain efficiency can't be avoided. This region is therefore not of interest for designers who want to make P.A. for the wireless market. A better way to achieve high output power is to reduce the DC-feed inductance. Now, the drain efficiency also decreases, see figure 3, but in a more gentle way. For the same output power of 1.06 Watt (see fig.2) a DC-feed of 0.5nH resp. 1.5nH with a target resistance of 4 Ω resp. 0.5Ω, can be used. In figure 3 we see that these points correspond with a drain efficiency of 68 percent resp. 45 percent. From this example, one can conclude that a smaller DC-feed gives a better performance. For a given DC-feed, the rightmost point on an efficiency or output power variation curve will be the optimal point. In this point the excess inductance (Lx) is reduced to zero and the target resistance will be maximized for a certain output power. The currents in the circuit will be small and the power losses in the parasitic resistances are minimal. A dashed line, in figure 2 and 3, connects the optimal points for different DC-feed inductances. An optimal Class E design must be situated on this dashed line. The dashed lines of figure 2 and 3 move in opposite directions, when increasing target resistance R. Achieving a high efficiency and a high output power at the same time is therefore impossible. The curves in figure 2 and 3 are made for a switch size of 6500µm/0.35µm. This switch is driven by a driver circuit, which consumes DC power. A predictor for the minimum driving power, necessary to drive a certain switch size, is implemented into the program. The resulting PAE can be calculated as

$$\mathrm{PAE} = \eta_{DE}.[1-(\mathrm{P}_{\mathrm{driver}} + \mathrm{P}_{\mathrm{in}})/\mathrm{P}_{\mathrm{out}}] \quad (4)$$

where P_{in} is assumed to be 10 dBm. For a design lying on the dashed line an optimal drain efficiency is achieved, therefore the maximum achievable PAE must also be on this curve.

3. Analysing existing Class E CMOS P.A.

For four recently published CMOS designs the variation curves are plotted in figures 4 and 5. These power amplifiers are designed with different CMOS technologies, different switch sizes, different matching networks and different frequencies. Therefore, the designs can not be compared with each other. However, an indication can be given how good the model matches the reality. Also, inside can be given in the trade off's made by the designer during the design process. The designs of [Yoo] and [Su] use a matching network, which is different from the up-conversion match used in our model. For keeping consistency with these designs, a matching network with the same quality factor is used. For the differential circuits of [Mert.] and [Tsai], only one side is treated. The output power published is therefore being halved, without having impact on the efficiencies. Let's focus on the design of [Mert.]. In this design the designer has aimed to achieve a maximum PAE. Form figure 6 we can conclude that the design achieves this goal. The design produces the highest PAE of the four designs. The price of achieving this high PAE, is the reduced output power of 0.5 Watt (see fig. 5). Notice, that for an increase in target resistance R the PAE (figure 5) keeps nearly constant, but the output power (figure 4) drops below 0.5 Watt. So, the design maximizes the PAE, while keeping the output power as large as possible. The design of [Tsai] uses the same topology as [Mert.]. However the frequency is increased from 700MHz to 1.9GHz. To achieve a reasonable output power, a 0.37nH DC-feed inductor is used. For this small DC-feed inductor a measured output power of 0.6 W is achieved, which is close to the predicted output

power of 0.56W. The high output power is accomplished by reducing the target resistance, instead of reducing the DC-feed inductor, because 0.37nH is already difficult to manufacture. For this reason, the design is not located at the rightmost point of the variation curve. We can conclude that for the Class E design of [Tsai] the highest possible output power at 1.9GHz is obtained.

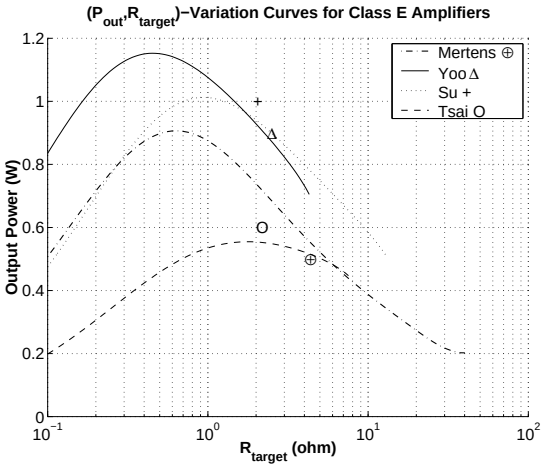

Fig. 4:Pout vs. Rtarget for different designs

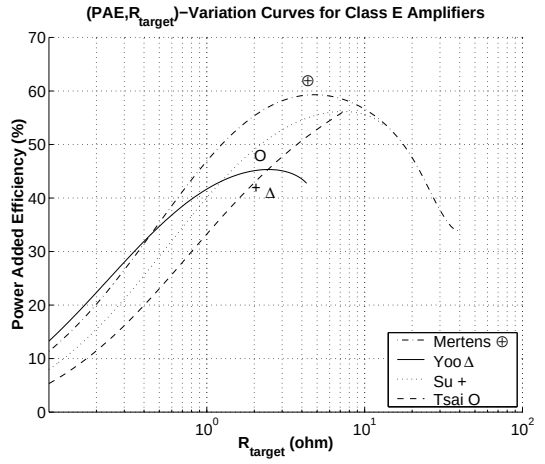

Fig. 5:PAE vs. Rtarget for different designs

The designs of [Yoo] and [Su] both produces an output power of around 1W. The design of [Yoo] is made in a 0.25 μm CMOS technology. The reduced break-down voltage (supply voltage) of this process is compensated by the 0.5nH DC-feed inductance used. Higher output powers for Class E power amplifier, made in smaller gate length technologies, can not be expected. The Class E amplifier of [Yoo] is positioned close to the rightmost point on the variation curve. So, the design of [Yoo] is designed for achieving the highest PAE possible for the demanded output power.

The PAE of [Su] lies 9 percent under the associated variation curve. The design uses a 5dBm input signal instead of the 10dBm reference input signal used by the program. An extra amplifier is necessary to convert the 5dBm input signal into 10dBm. The power consumed by the extra amplifier decreases the PAE. This explains the difference with our model.

4. A new way to boost the performance

The most crucial parameter in a CMOS power amplifier design is the break-down voltage of the NMOS switch transistor. This break-down voltage may not be exceeded during the operation of the amplifier, otherwise permanent damage or performance degradation can occur. The normalized drain voltage expresses the ratio of the peak drain voltage and the DC supply voltage. When changing the values of the DC-feed or the shunt capacitance, the normalized drain voltage (C_{pv}) changes. So, for each design a maximum supply voltage can be calculated, given by expression 5.

$$V_{DC,supply} = V_{Break\text{-}Down} / C_{pv} \quad (5)$$

It was shown from expression 3, that the output power is proportional to the square of the used supply voltage. To compare different designs, the supply voltage must be adapted to the break-down voltage of the used CMOS technology. In the contour plot of figure 6, the design of [Mert.], marked with a ⊕, is taken as the reference point. This design is made in a 0.35um technology with a break-down voltage of 7.2V. For this point a 2.2V supply voltage is needed.

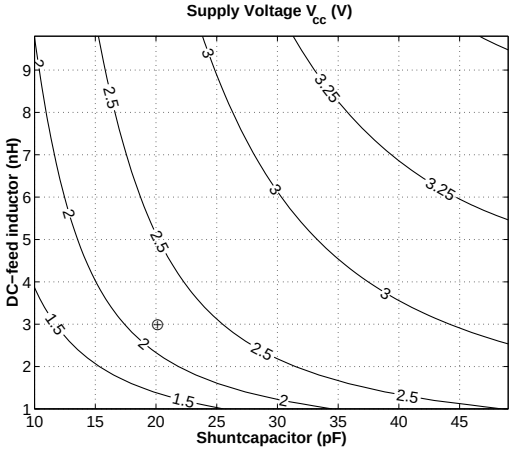

Fig.6:Contour plot for the supply voltage

This means that C_{pv} is equal to 3.27, which is in good agreement with the ideal Class E theory. For a Class E amplifier C_{pv} is equal to:

$$C_{pv} = (V_{DC,supply} + 2.56\eta_{Ron} V_{DC,supply}) / V_{DC,supply} \quad (5)$$

and when no Ron resistance is present, above formula becomes equal to 3.56.

If we deviate from the ideal Class E amplifier design, by increasing L_{dc} or C_{shunt}, the C_{pv} is reduced and the design is moved to a Class C operating point. Hence, the DC supply voltage can be increased to values up to

3.25V, as one can see in the contour plot of figure 6. Moving towards Class C operation has a good influence on the output power and PAE of the design. In figures 7 and 8 the contour plots of the PAE and the output power are given for variations of the DC-feed and the shunt capacitance.

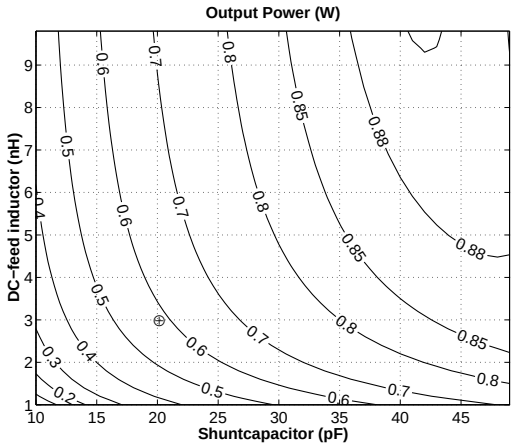

Fig. 7:Contour plot for the Output Power

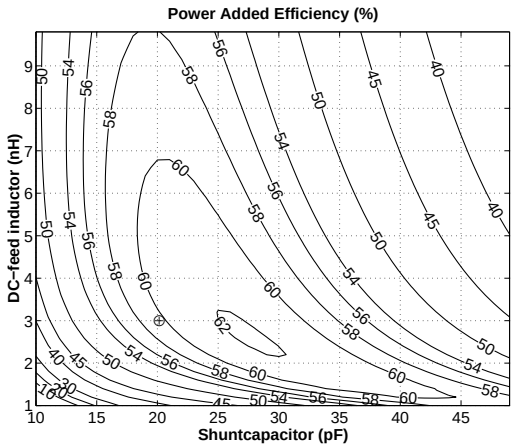

Fig. 8:Contour plot for the PAE

In figure 8, we notice that for an increase of the shunt capacitance, beginning from the reference design ⊕, the PAE increases to 62 percent for a capacitance of 27pF. For a further increase of the capacitance, the PAE will decrease. Still, a PAE of 45 percent can be achieved, for a 50pF capacitance. Looking at the power contour plot of figure 7 reveals that for a shunt capacitance of 50pF, the power is increased with 45 percent. So, for a design that lies between a Class E and a Class C operation point, a better performance can be achieved. This observation is in contrast with the idea that an ideal Class E amplifier achieves the best efficiency for a given output power [Su]. When all losses (DC-feed, Switch and matching), are taken in account, a better performance can be achieved by deviating from the traditional Class E conditions. The reasoning for the shunt capacitance can be repeated for the DC-feed inductor. Also here, a larger DC feed results in an improvement in output power and PAE. Increasing the DC-feed and the shunt capacitance improves the output power and PAE and has some beneficial side effects. A larger shunt capacitance can be used to linearize the non-linear C_{DS} capacitance of the NMOS switch [2]. Also, wider interconnect traces can be used in the layout, making it easier to satisfy the electron migration rules imposed by the used technology. Notice that the shunt capacitance, given by expression 2, becomes smaller for higher frequencies. An increase of the shunt capacitance can be used to counteract this harmful effect. The gain in output power, resulting from the increased shunt capacitance, is also more than welcome, since the maximum achievable output power drops drastically for higher center frequencies [Tsai]. When going to smaller gate lengths the output power will also decrease, because the break-down voltage becomes smaller [Yoo]. Also, here it will be beneficial to go to a Class C design to achieve output powers of one watt.

5. Conclusion

In the past, it was believed that a Class E would always result in a design with the best efficiency for a given output power. However, a better performance is obtained by pushing the amplifier to a Class C operation point. This conclusion can only be made if all the losses are taken into account. A larger DC-feed and shunt capacitance, resulting in a more Class C operating point, would make it possible in the near future to work at higher frequencies and smaller CMOS technologies.

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