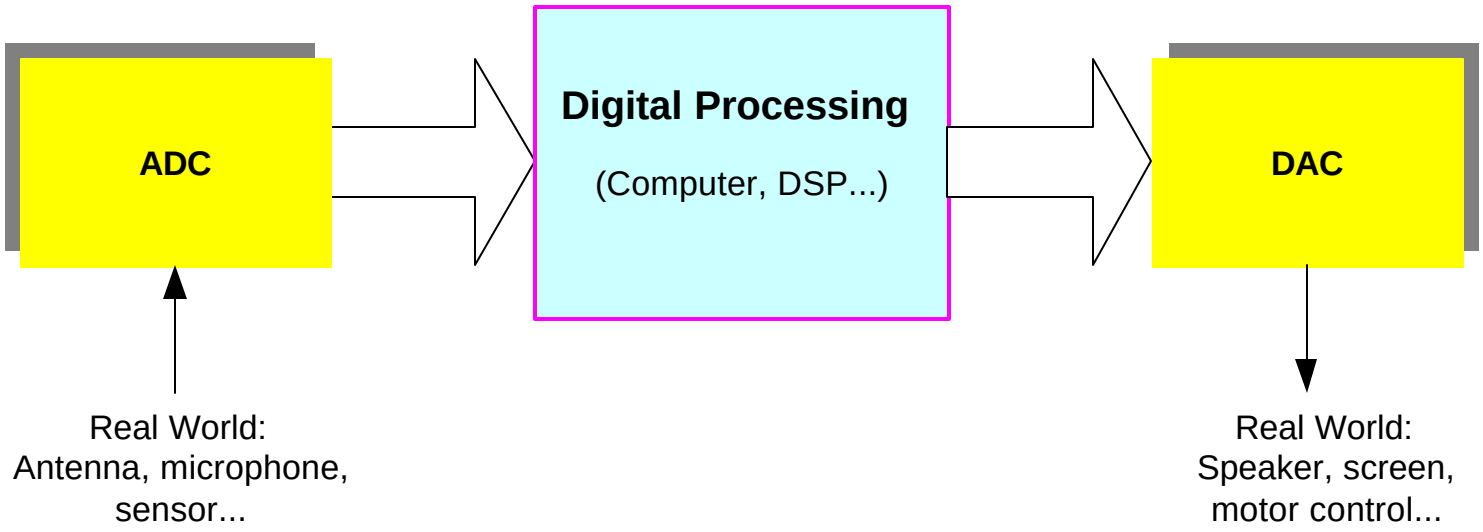
Data Converters

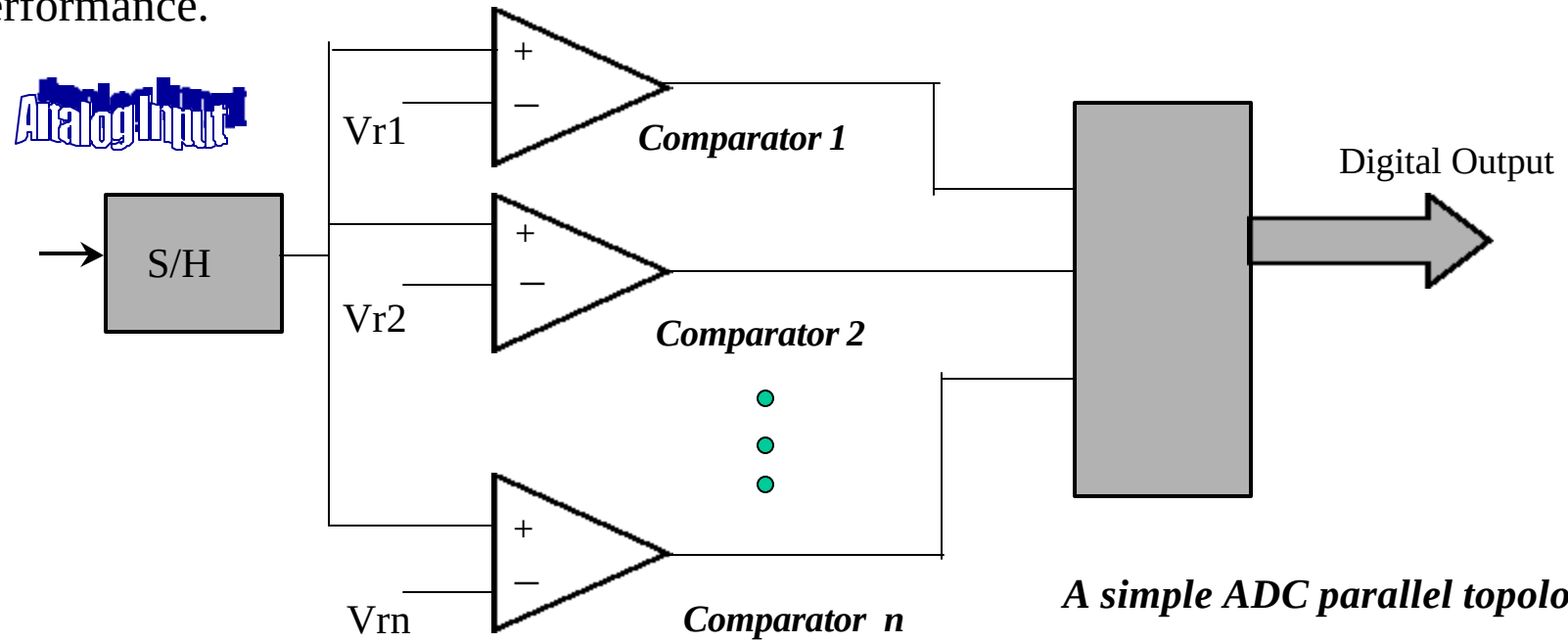
- The Real World is Analog

- ADC are necessary to convert the real world signals (analog) into the digital form for easy processing



Basic Concepts

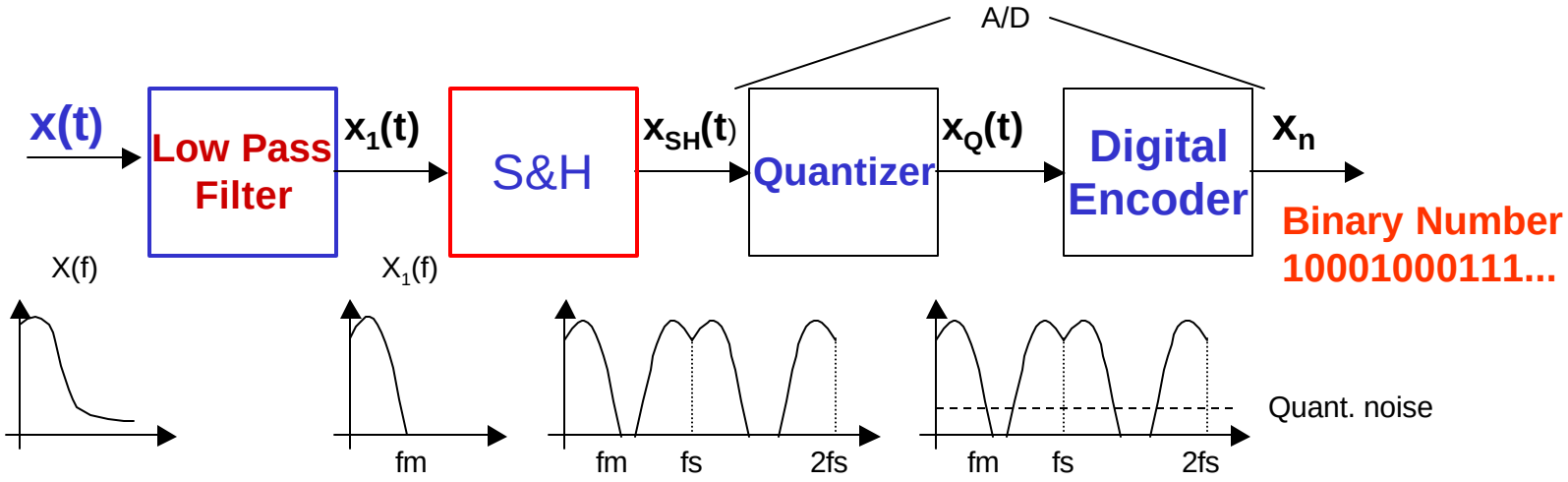
- The goal of an ADC is to determine the output digital word corresponding to an analog input signal.
- The basic internal structures of ADC rely heavily on DACs structures.
- ADCs can be seen as low speed (serial type), medium speed, high-speed and high-performance.



A simple ADC parallel topology

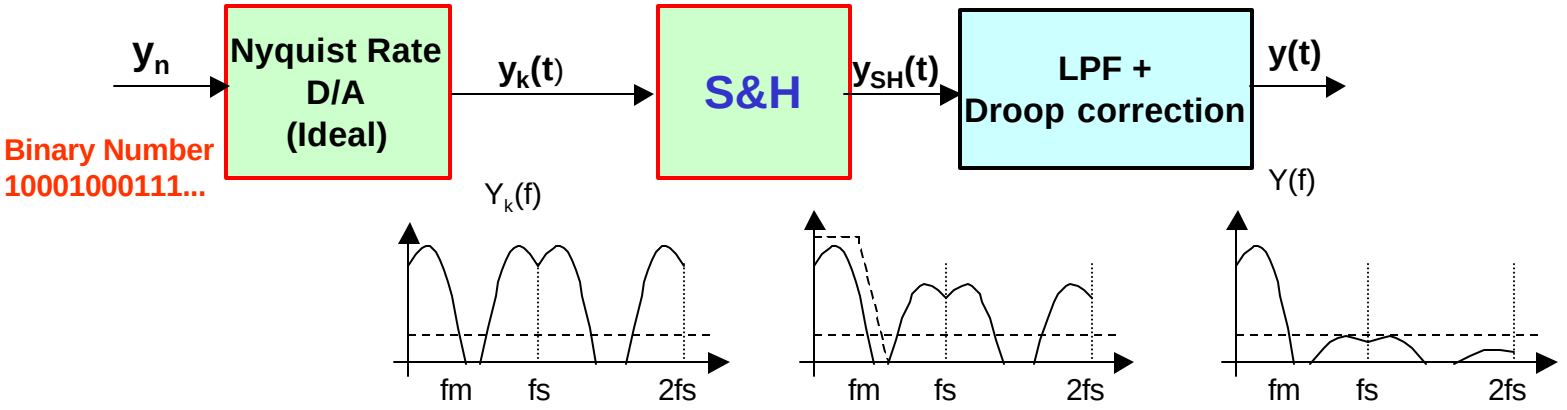
Fundamentals

- Traditional Data Converters at Nyquist Rate (fs>2fm)
  - A/D Converter Details:



Fundamentals

- Traditional Data converters at Nyquist Rate (fs>2fm)
  - D/A Converter:

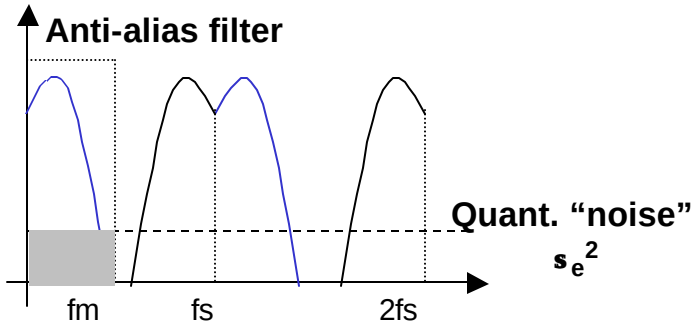


• Droop correction means inverse Sinc

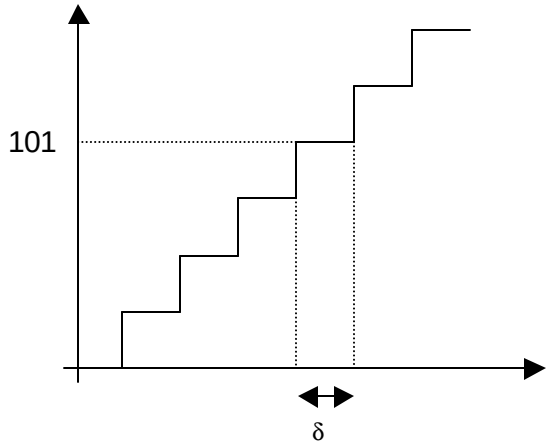
• The S/H is a “deglitching” circuit and could be eliminated for small glitches

Fundamentals

- A/D: Sampled Signal Spectrum:



$$DR = 1.5\,(K-1)^2 = \Big|_{dB}\ 1.76 + n*6.02$$



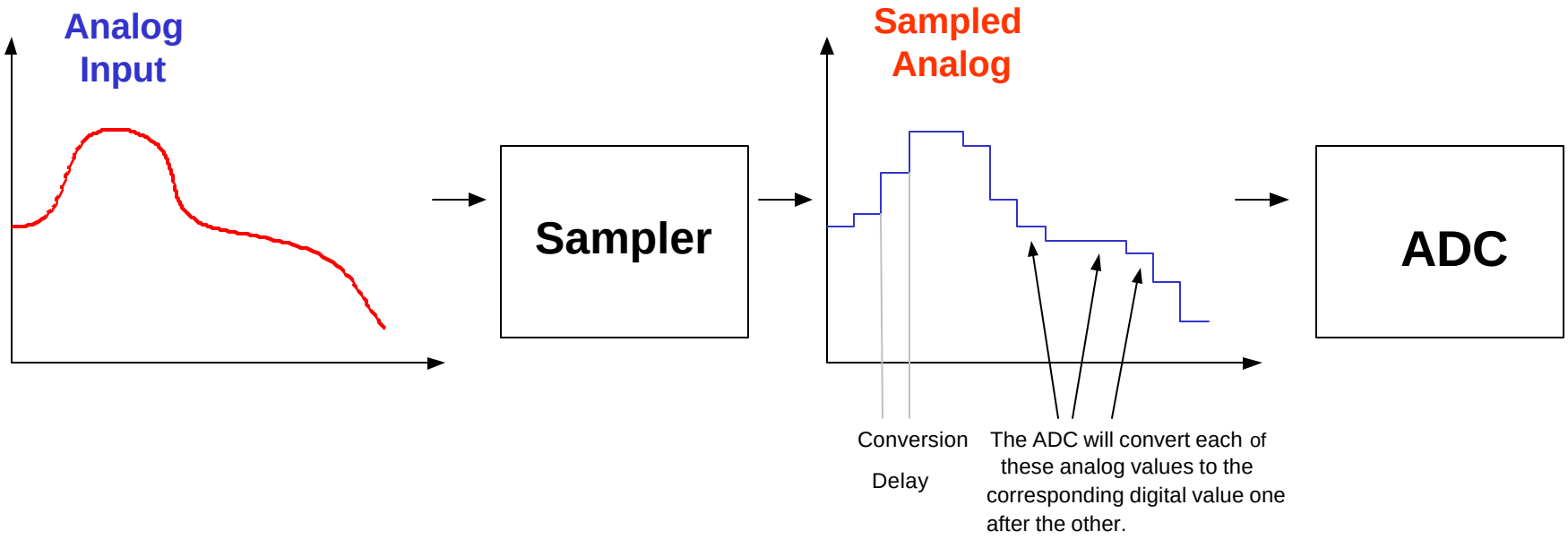
$$s_e^2 = d^2/12$$

K: # Quantizer levels

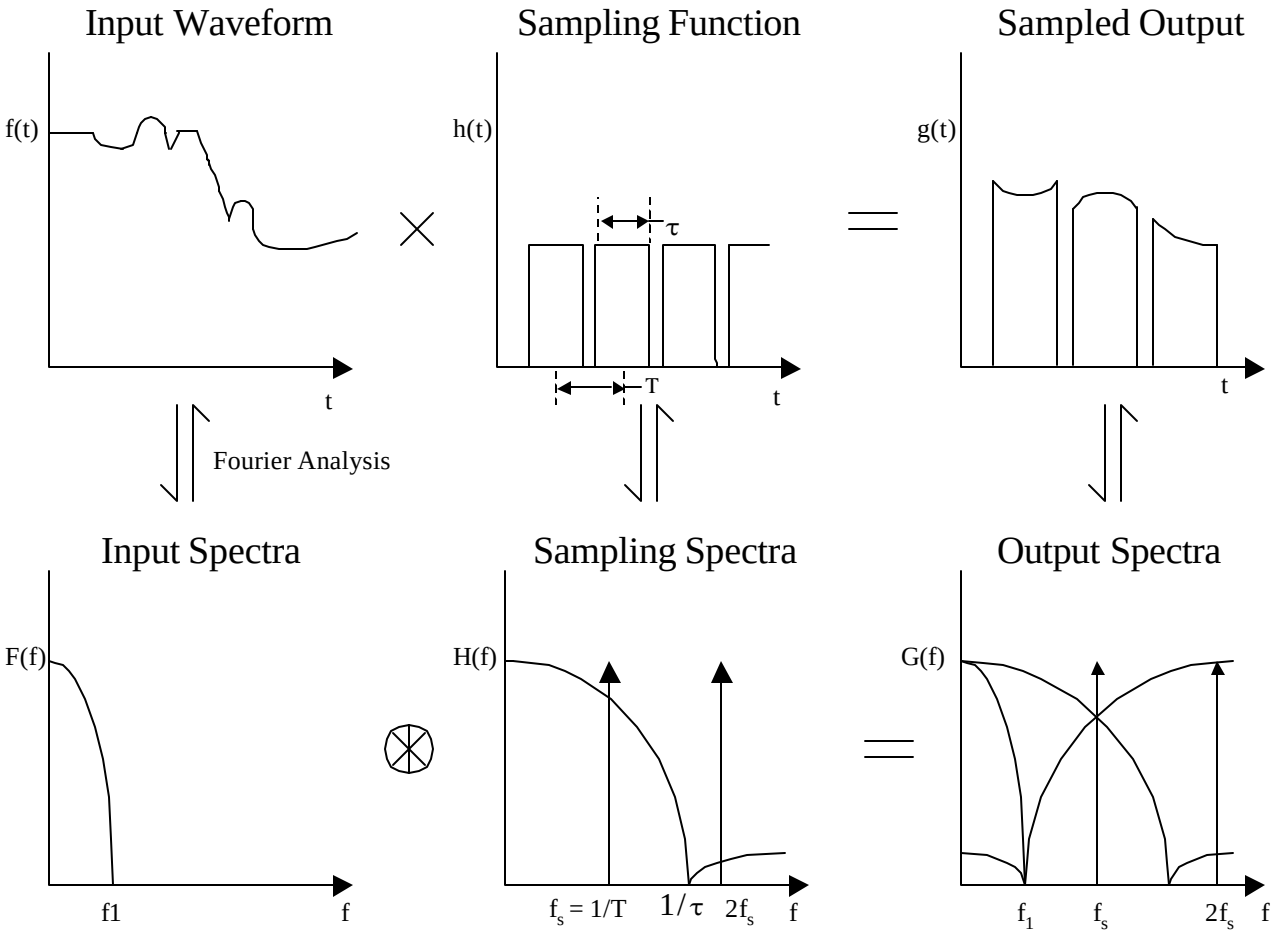
n: Equivalent # Bits

Sampling

- The process of converting to digital can not be instantaneous
- The input has to be stabilized while a conversion is performed.



REAL SAMPLING



Input signals are not truly band limited

$$f(s) \gtrless 2f_1$$

Sampling cannot be done with impulses so, amplitude of signal is modulated by

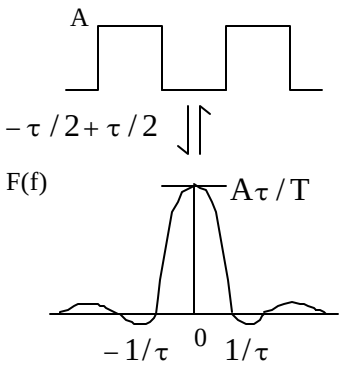
$$\frac{\sin x}{x}$$ envelope

Because of input spectra and sampling there is aliasing and distortion

Square Wave $\rightleftharpoons \frac{\sin x}{x}$

f(t)

Period T



Envelope has the form

$$E = \frac{A\tau}{T}\left(\frac{\sin \pi f \tau}{\pi f \tau}\right)$$

Performance Metrics

Since real Data Converters have a number of non-idealities we need to use a Performance Metrics to evaluate and compare them. In what follows we will attempt to define it.

The number of bits of the digital code is finite: for n-bit we have 2^n codes and each code represents a given *quantization level*.
The error due to the quantization is called quantization error and ranges between plus or minus half quantization level (LSB). This error is a consequence (and a measure) of the finite A/D converter resolution.
Furthermore, the quantization error can be considered as a noise if all quantization levels are exercised with equal probability, the quantization steps are uniform; a large number of quantization levels are used, and thev quantization error is not correlated with the input signal

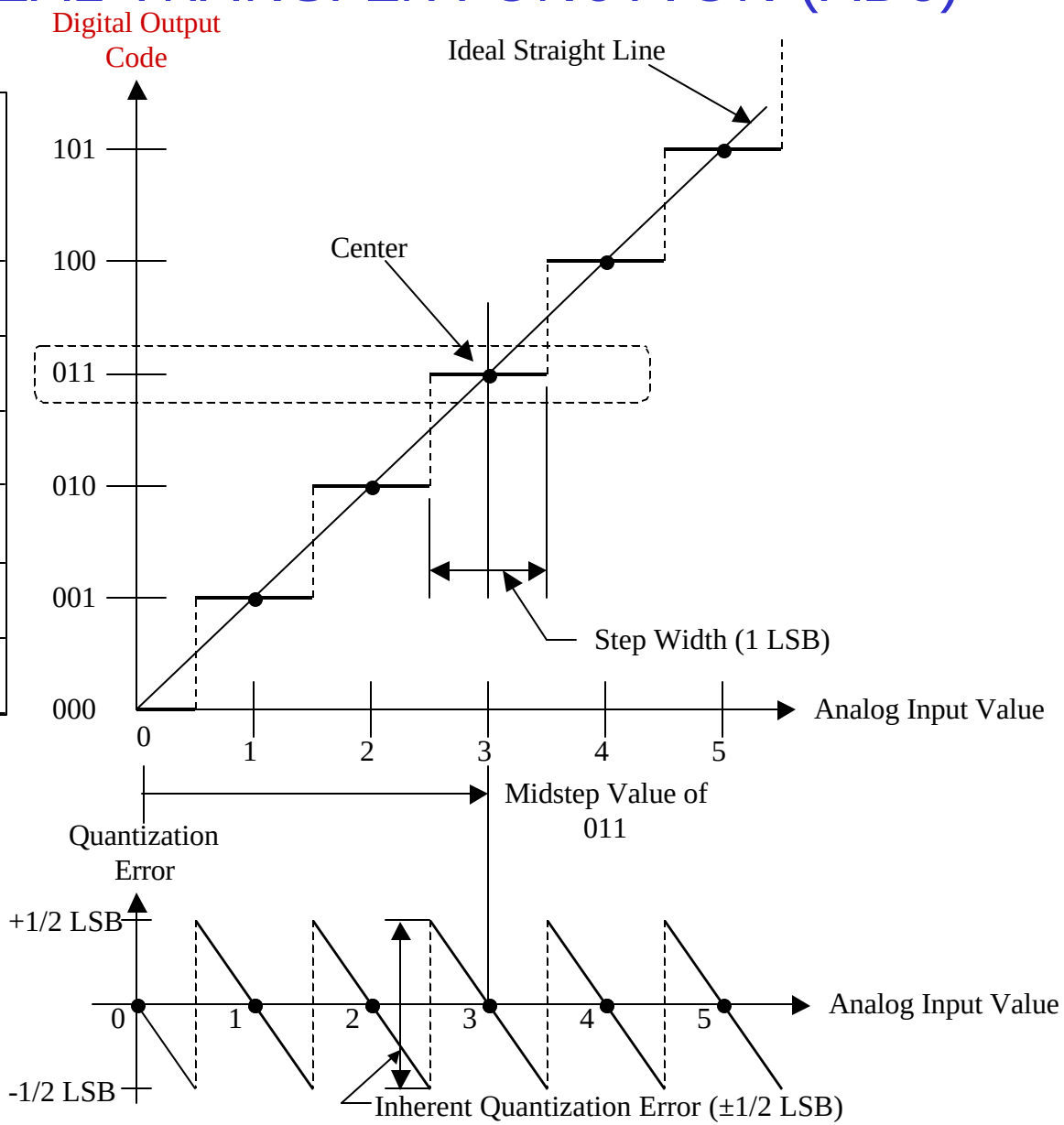
Definitions

- Differential Nonlinearity:
  Deviation in the width of a certain code from the value of 1LSB.
- Integral Non-Linearity:
  Deviation in the midpoint of the code from the best straight line in LSBs.

THE IDEAL TRANSFER FUNCTION (ADC)

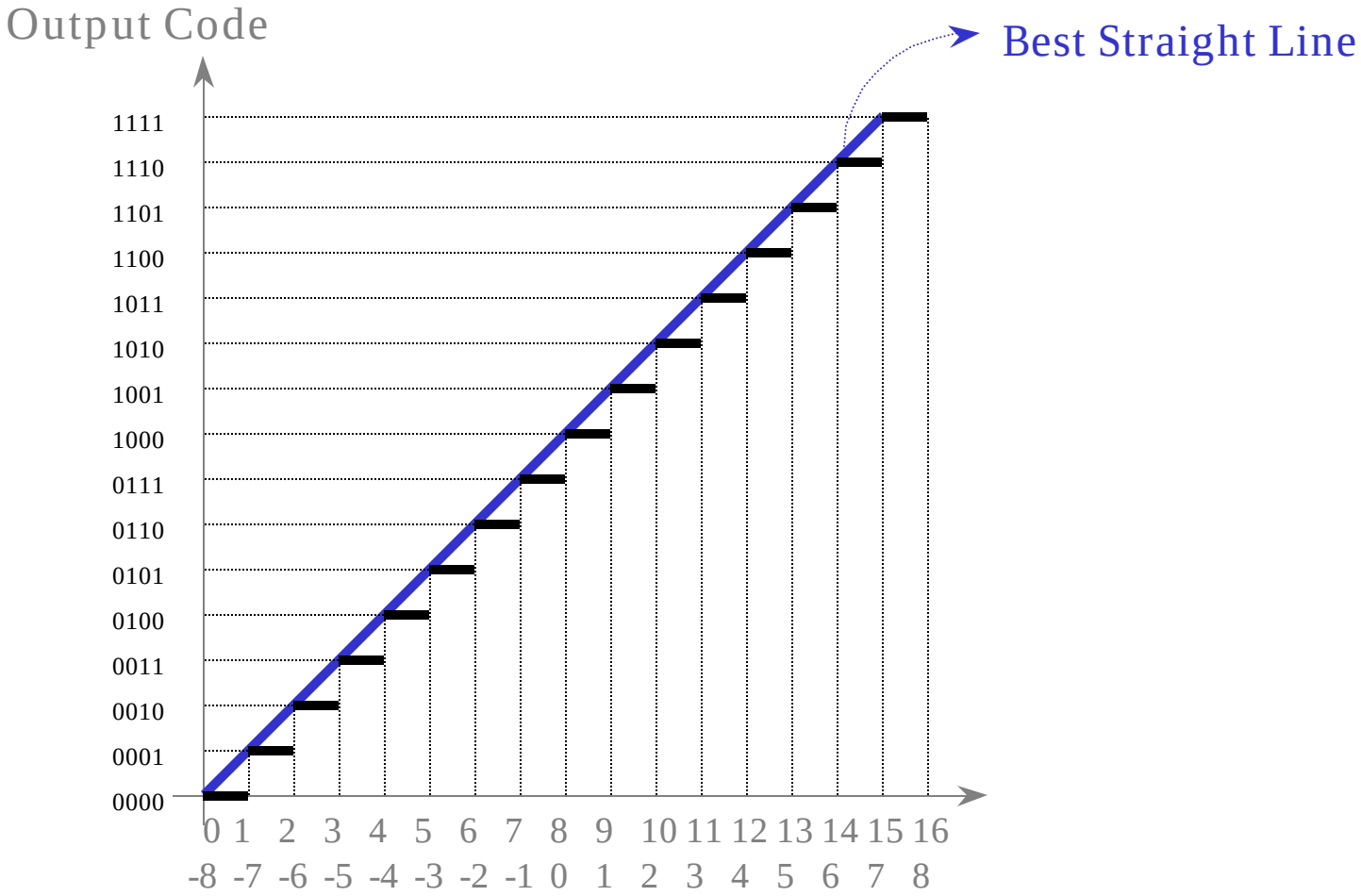
Conversion Code

Range of Analog Input Values	Digital Output Code
4.5 • 5.5	101
3.5 • 4.5	100
2.5 • 3.5	011
1.5 • 2.5	010
0.5 • 1.5	001
0 • 0.5	000

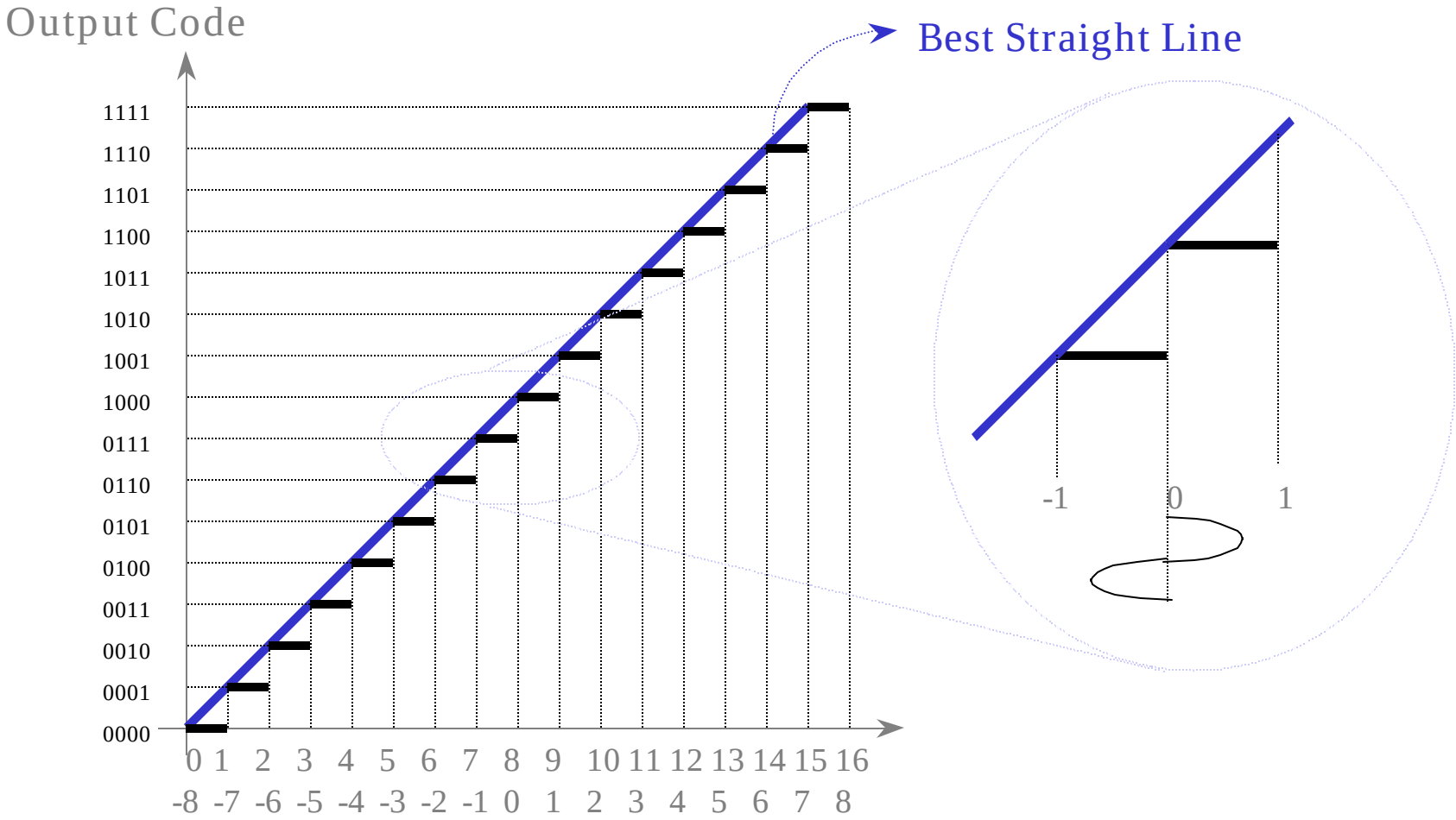


Elements of Transfer Diagram for an Ideal Linear ADC

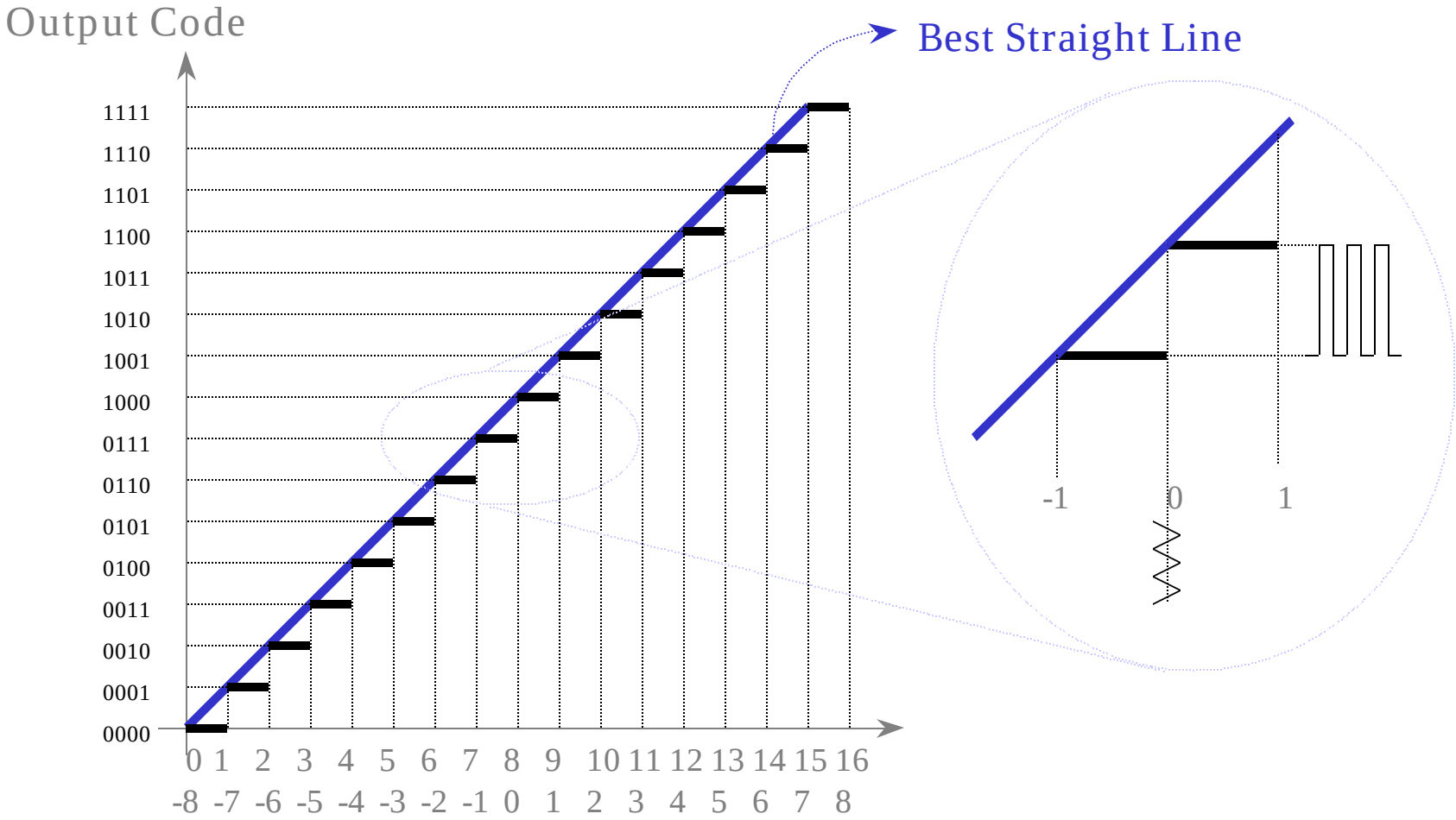
Ideal Transfer Characteristic



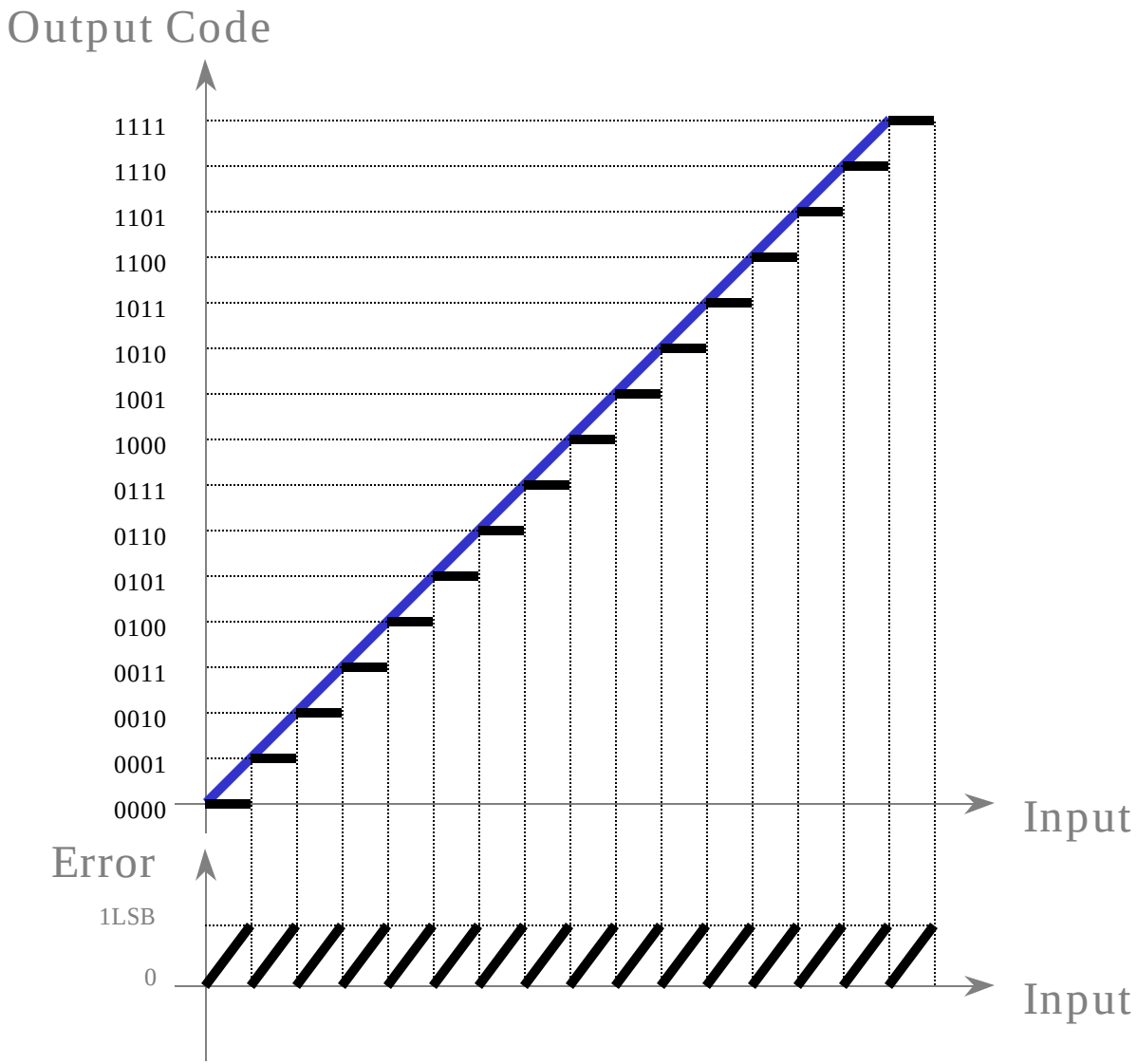
Ideal Transfer Characteristic



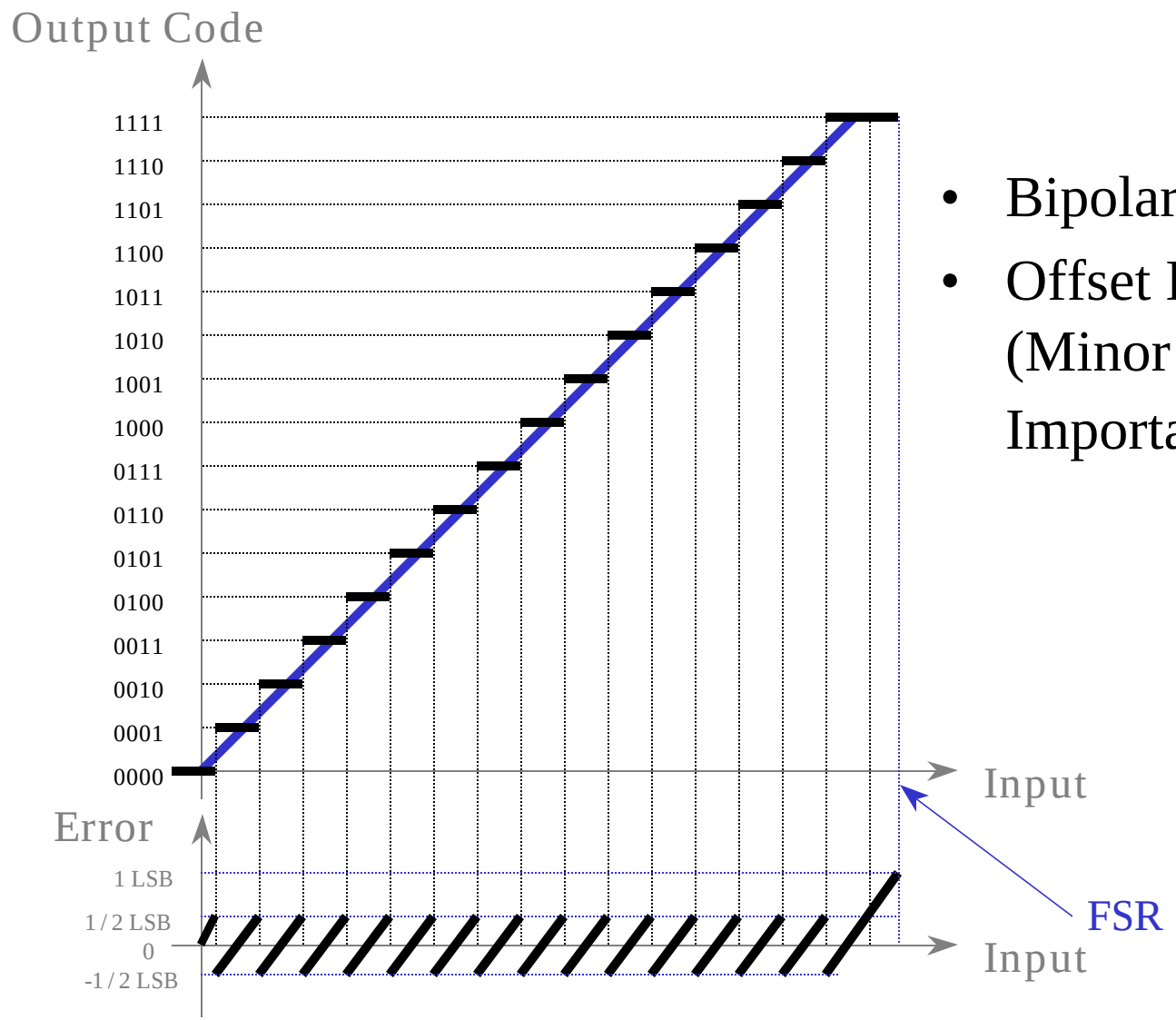
Ideal Transfer Characteristic



Unipolar Quantization Error



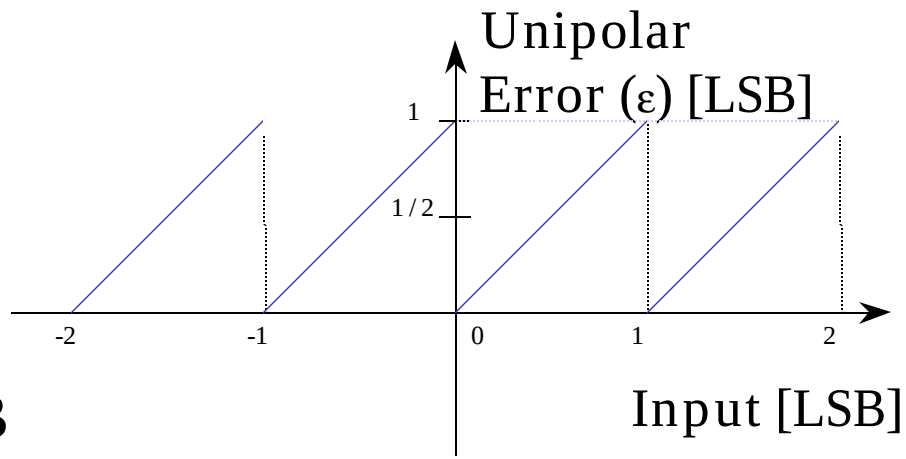
Bipolar Quantization Error



- Bipolar Error
- Offset Error (Minor Importance)

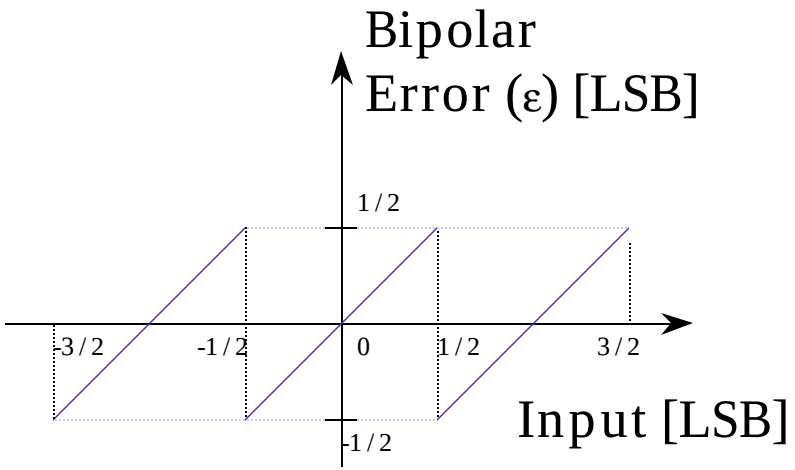
Unipolar vs. Bipolar

- Quantization Noise Power:
  $LSB^2/3$
- RMS Value of Quantization Noise Power:
  $LSB/1.73$
- More Than Half an LSB error.



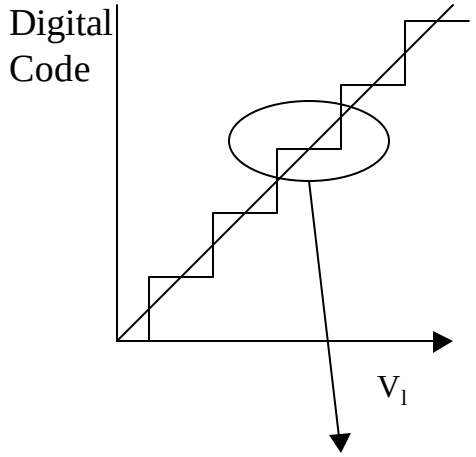
Unipolar vs. Bipolar

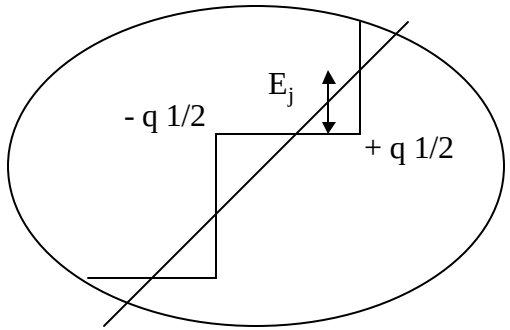
- Quantization Noise Power:
  $LSB^2/12$
- RMS Value of Quantization Noise Power:
  $LSB/3.46$
- Approximately One Third of an LSB.

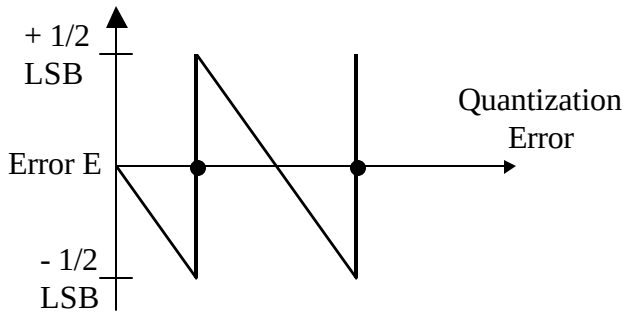


Reference: Spectra of Quantized Signals, W.R.Bennett, BSTJ, July 1948.

QUANTIZATION EFFECTS







Error at the jth step:

$$E_j = (V_j - V_l)$$

The mean square error over the step is:

$$\overline{E_j}^2 = \frac{1}{q_1}\int_{-q/2}^{+q/2} E_j^2 dE = \frac{q^2}{12}$$

Assuming equal steps, the
total error is:

$$\overline{N}^2 = q^2/12$$

(Mean square quantization noise)

QUANTIZATION EFFECTS

Considering a sine wave input F(t) of amplitude A so that $F(t) = A \sin \omega t$

which has a mean square value of $F^2(t)$, where $F^2(t) = \frac{1}{2\pi} \int_0^{2\pi} A^2 \sin^2(\omega t) dt$

which is the signal power. Therefore the signal to noise ratio SNR is given by

$$SNR(dB) = 10 Log \left[\left(\frac{A^2}{2} \right) \Big/ \left(\frac{q^2}{12} \right) \right] \quad \text{but} \quad q = 1\,LSB = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$$

Substituting for q gives

$$SNR(dB) = 10\ Log \left[\left(\frac{A^2}{2} \right) \Big/ \left(\frac{A^2}{3 * 2^{2n}} \right) \right] = 10\ Log \left(\frac{3 * 2^{2n}}{2} \right)$$

$$\Rightarrow \underline{\underline{6.02n + 1.76dB}}$$

This gives the ideal value for an n bit converter and shows that each extra 1 bit of resolution provide approximately 6 dB improvement in the SNR.

In practice, integral and differential non-linearity (discussed later in this presentation) introduce errors that lead to a reduction of this value. The limit of a 1/2 LSB differential linearity error is a missing code condition which is equivalent to a reduction of 1 bit of resolution and hence a reduction of 6 dB in the SNR. This then gives a worst case value of SNR for an n-bit converter with 1/2 LSB linearity error

$$SNR\ (\text{worst case}) = 6.02n + 1.76 - 6 = 6.02n - 4.24dB$$

Thus, *we can established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR.*

Signal to Noise Ratio (SNR)

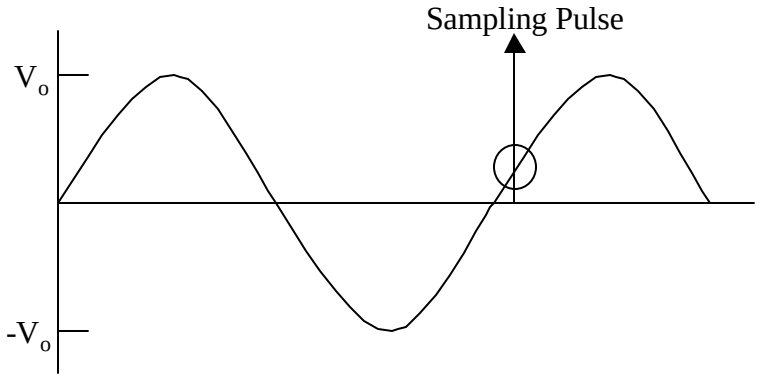
- $V_{in}=A\ \mathrm{Sin}(\omega T)$; $A = V_{FSR} / 2$
- Signal Power:

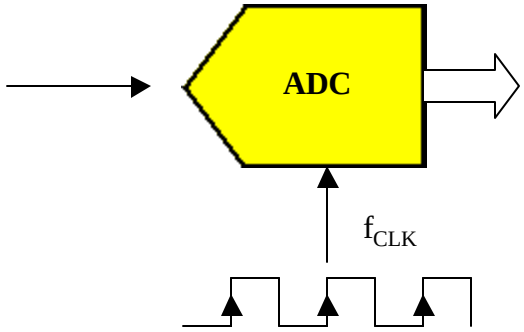
  $V_S^2 = (V_{FSR} / 2.8)^2 = V_{FSR}^2/8$
- Noise Power:

  $V_N^2 = LSB^2/12$
- SNR = $(1.5)2^{2N}$

  $1.8 + 6.02\ N\ [dB]$
- Example: SNR(10bit) = 62dB

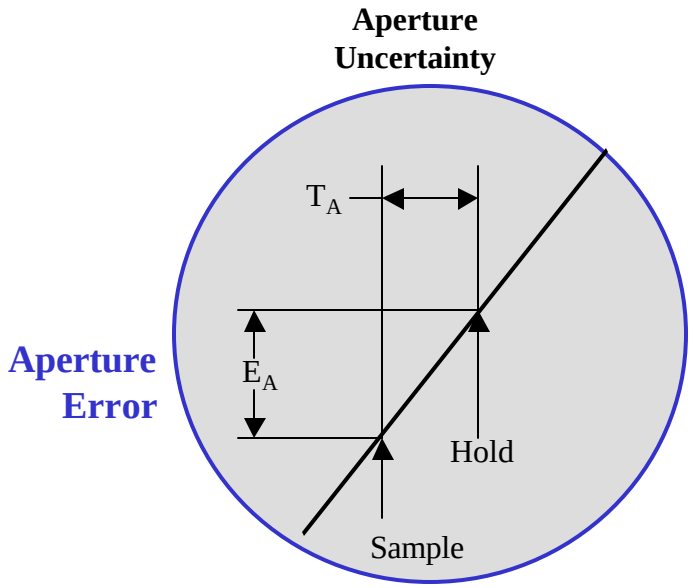
APERTURE ERROR





The aperture error comes from the fact that there is a delay between the clock signal and the effective holding time.

$$V = V_O \sin 2\pi ft$$



$$\frac{dV}{dt} = 2\pi fV_O \cos 2\pi ft \qquad \left.\frac{dV}{dt}\right|_{max} = 2\pi fV_O$$

$$E_A = T_A \frac{dV}{dt} = 1/2\ LSB = \frac{2V_O}{2^{n+1}}$$

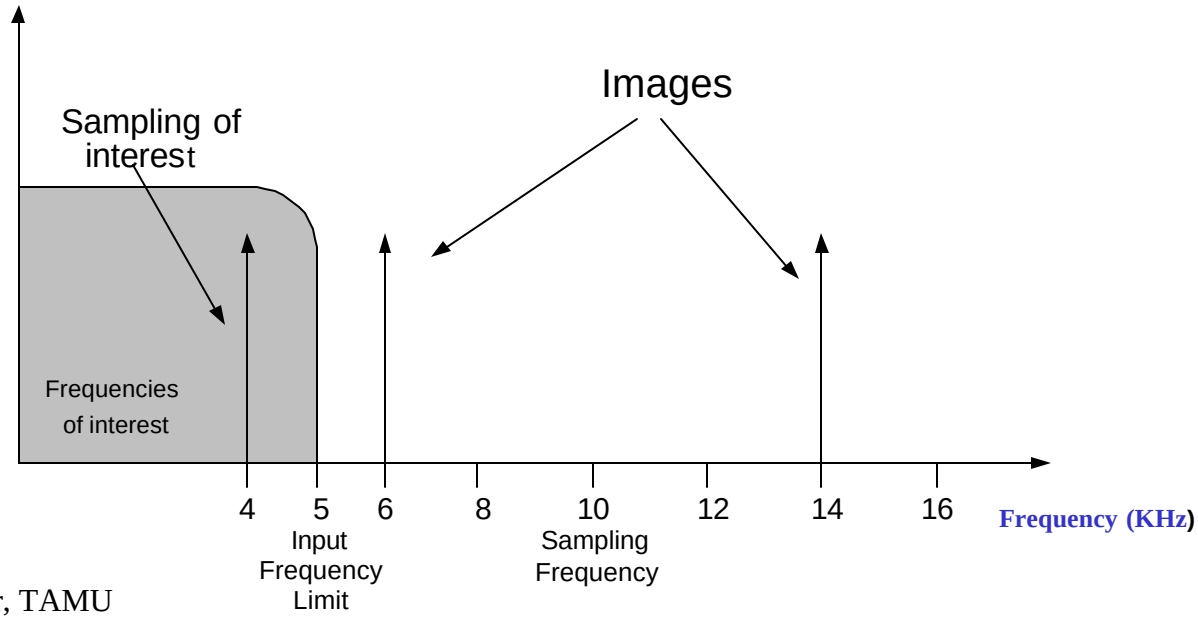
$$\frac{2V_O}{2^{n+1}} = 2\pi fV_O T_A \Rightarrow$$

$$T_A < \frac{V_{LSB}}{\pi f V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

Nyquist Rate

- According to signal processing theory, the sampling process generates images of the input signal around the sampling frequency

- It can be seen that if the input frequency is higher than half the sampling frequency, there will be corruption of the information by the image.



Oversampling

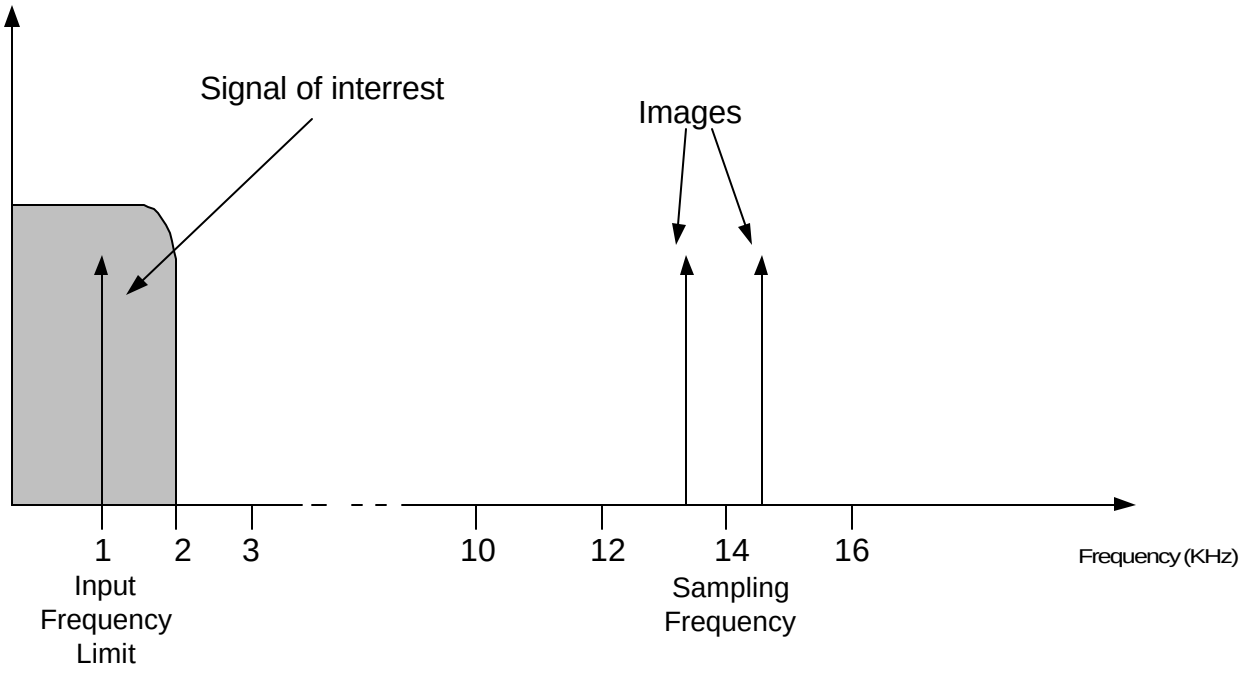
- As we have seen earlier, the SNR of a typical ADC is:

$$6.02n + 1.76dB$$

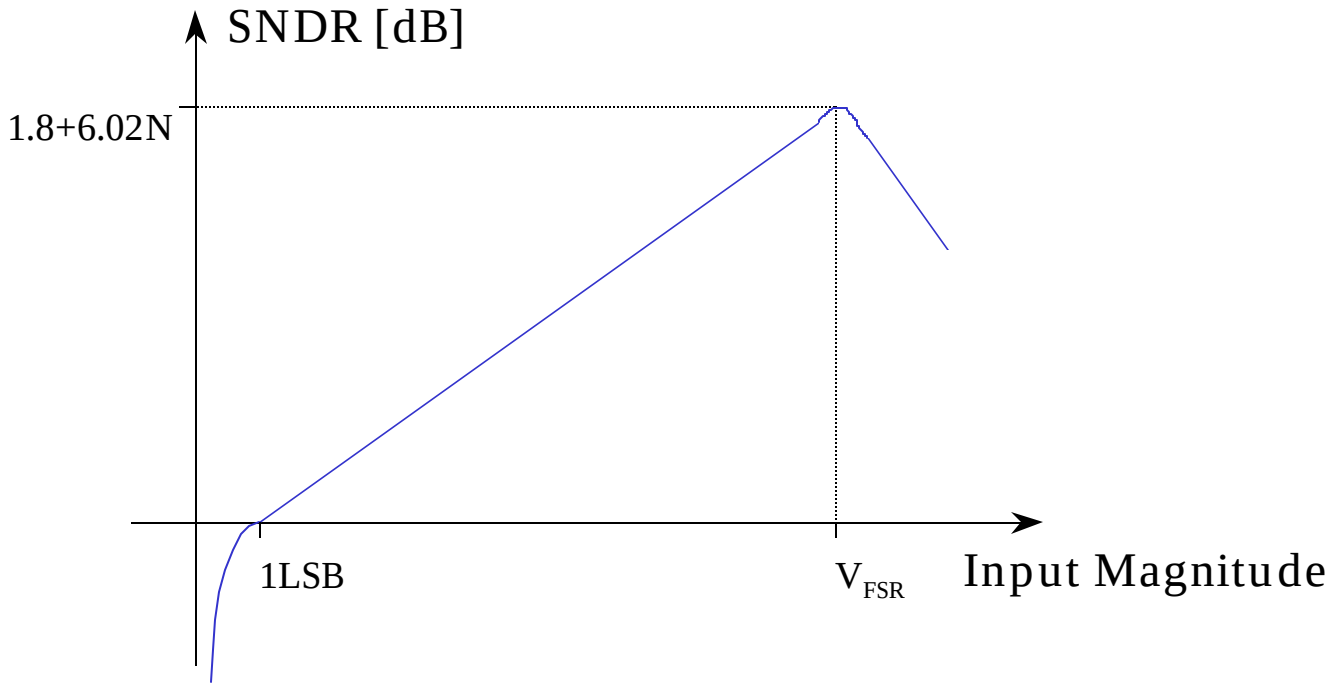
- If the sampling rate is increased, we get the following SNR:

$$6.02n+1.76dB+10\log(OSR)$$

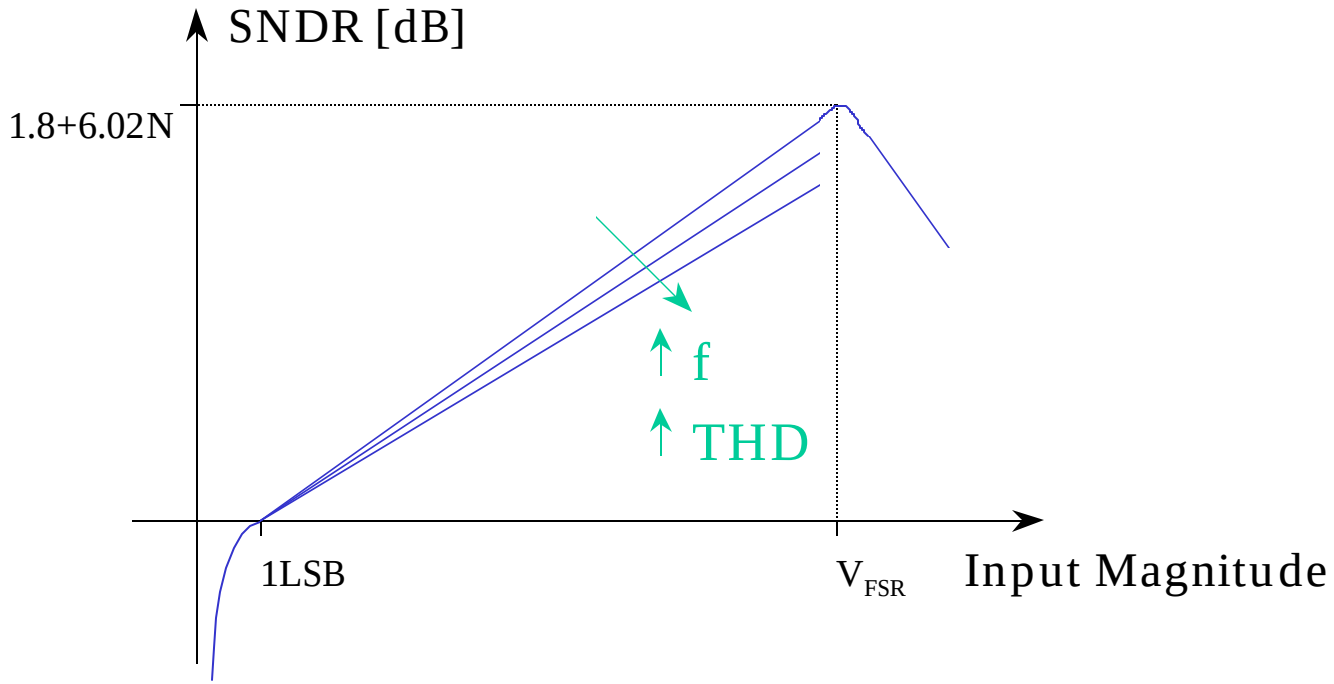
where OSR stands for "***oversampling ratio***".



Signal to Noise + Distortion Ratio (SNDR)

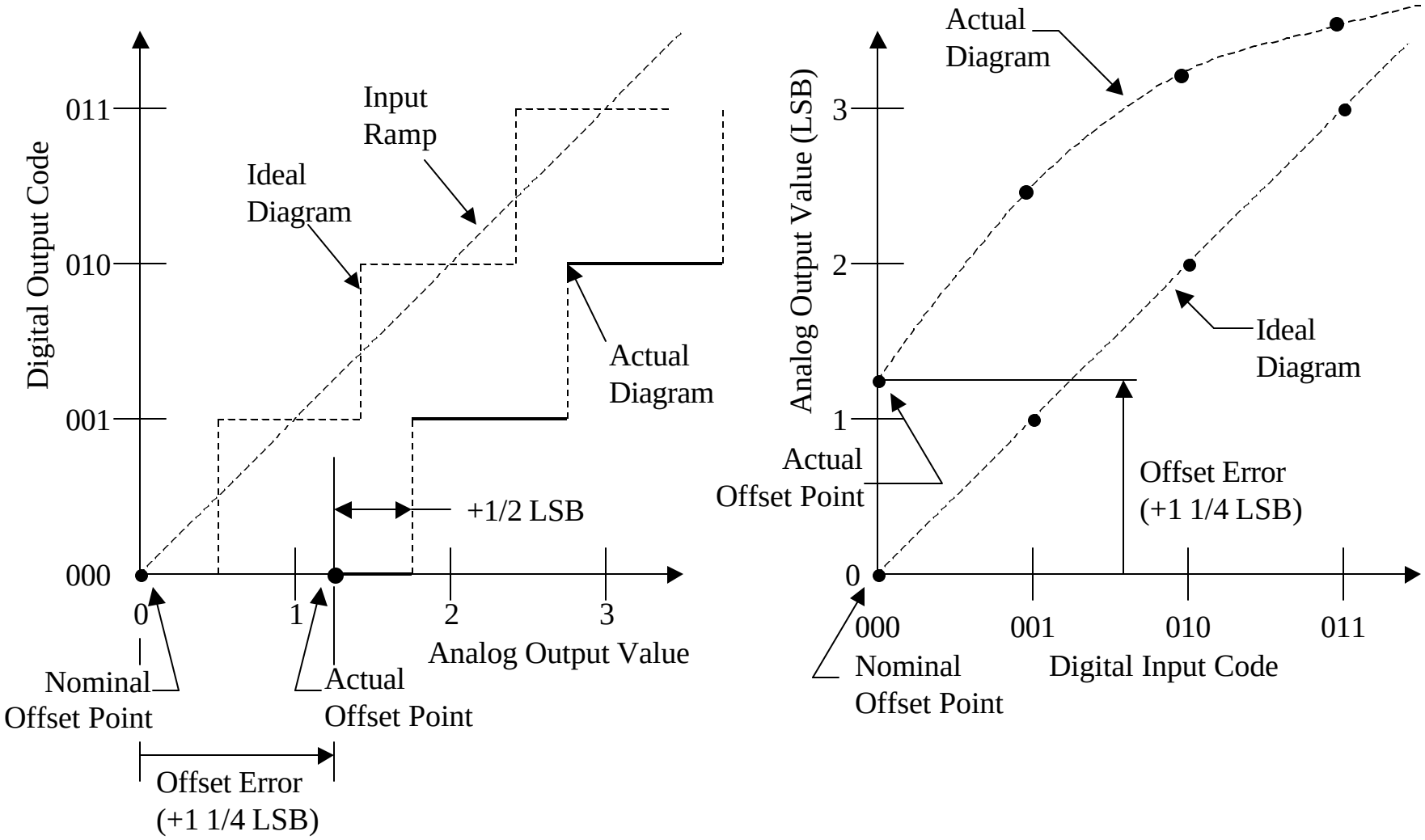


Signal to Noise + Distortion Ratio (SNDR)



Performance Evaluation of ADCs

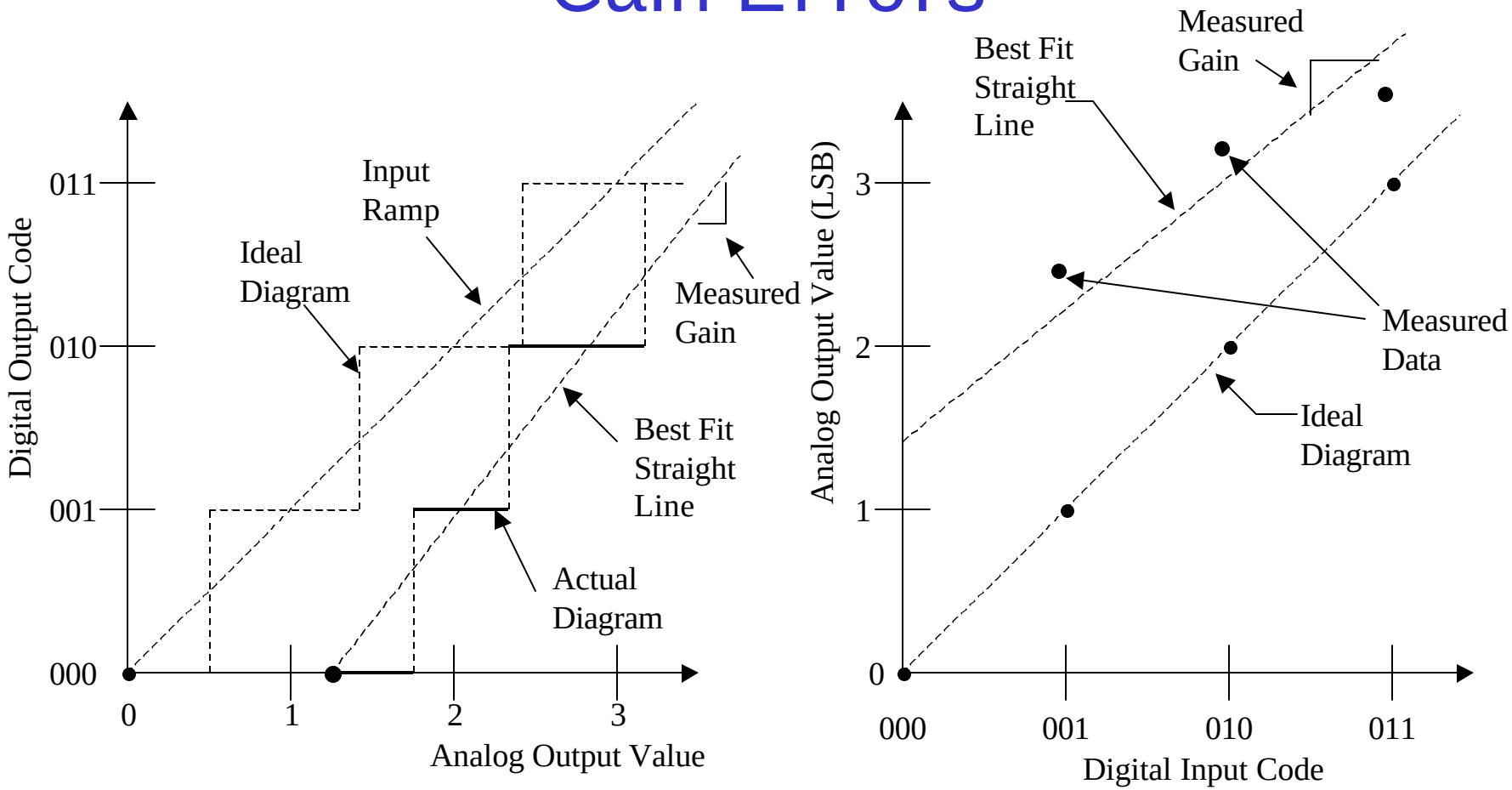
Offset Errors



(a) ADC

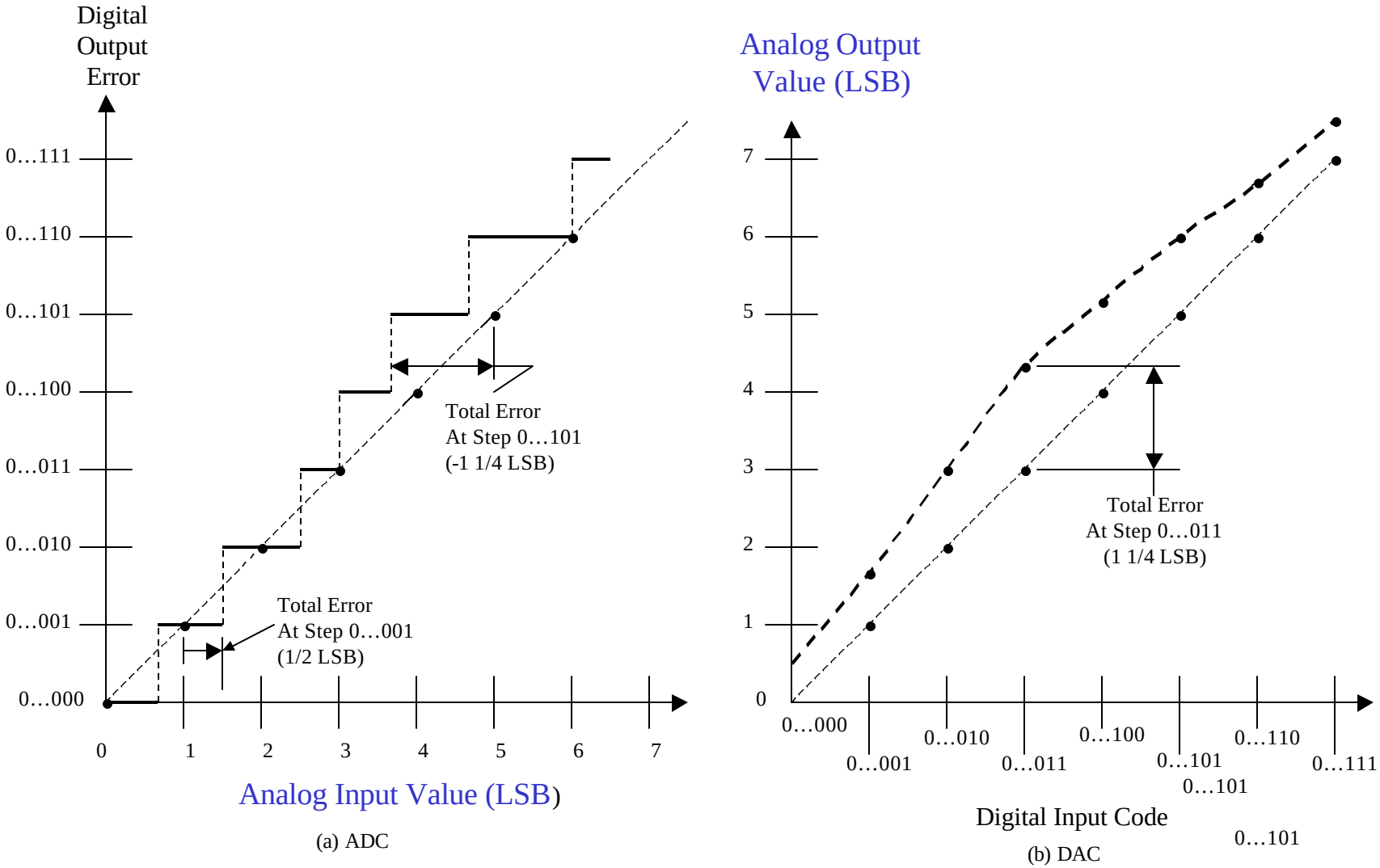
(b) *DAC*

Gain Errors



(a) ADC (b) *DAC*

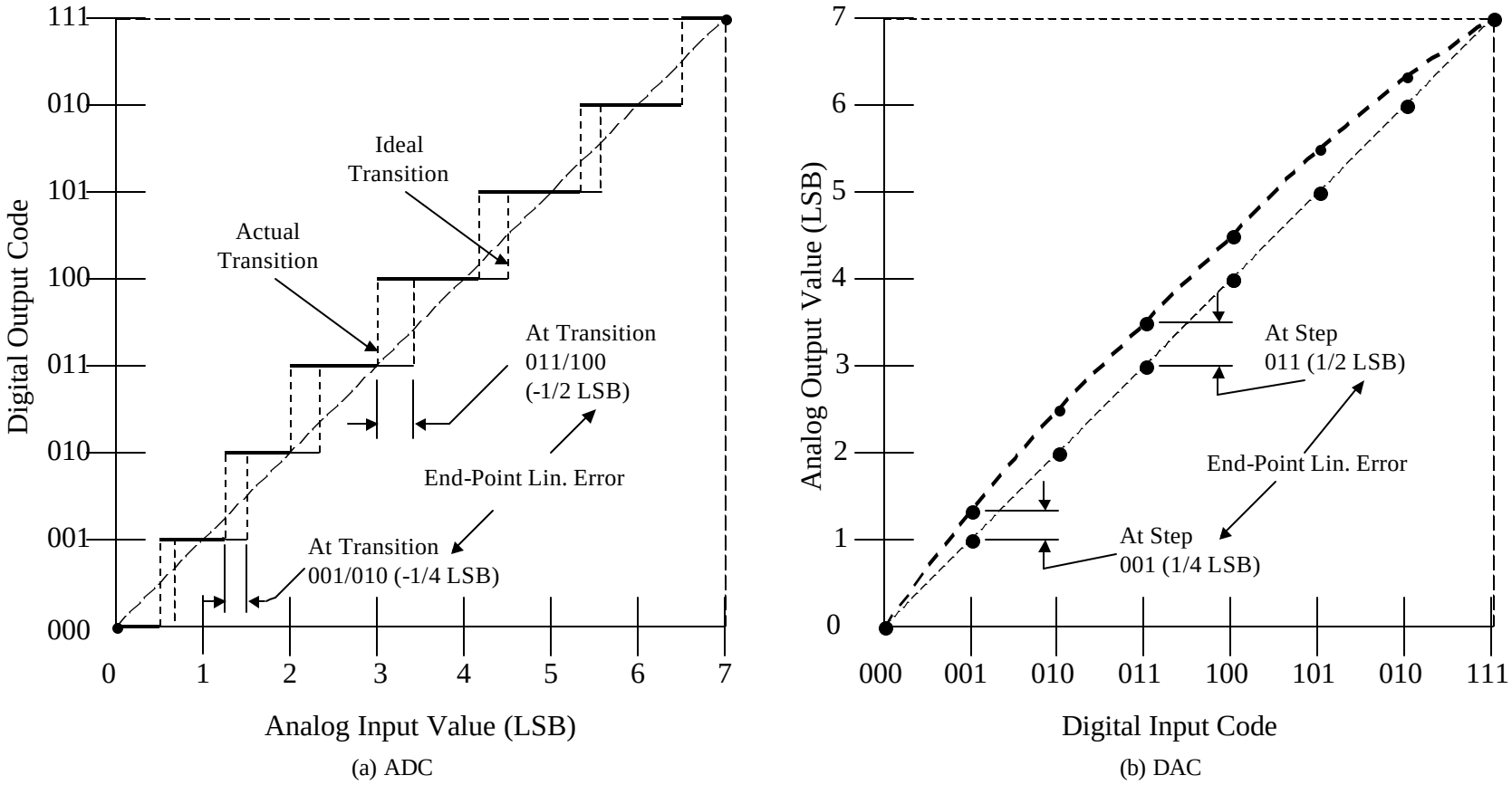
Absolute Accuracy (Total) Error



The absolute accuracy or total error of an ADC as shown in Figure is the maximum value of the difference between an analog value and the ideal midstep value. It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC.

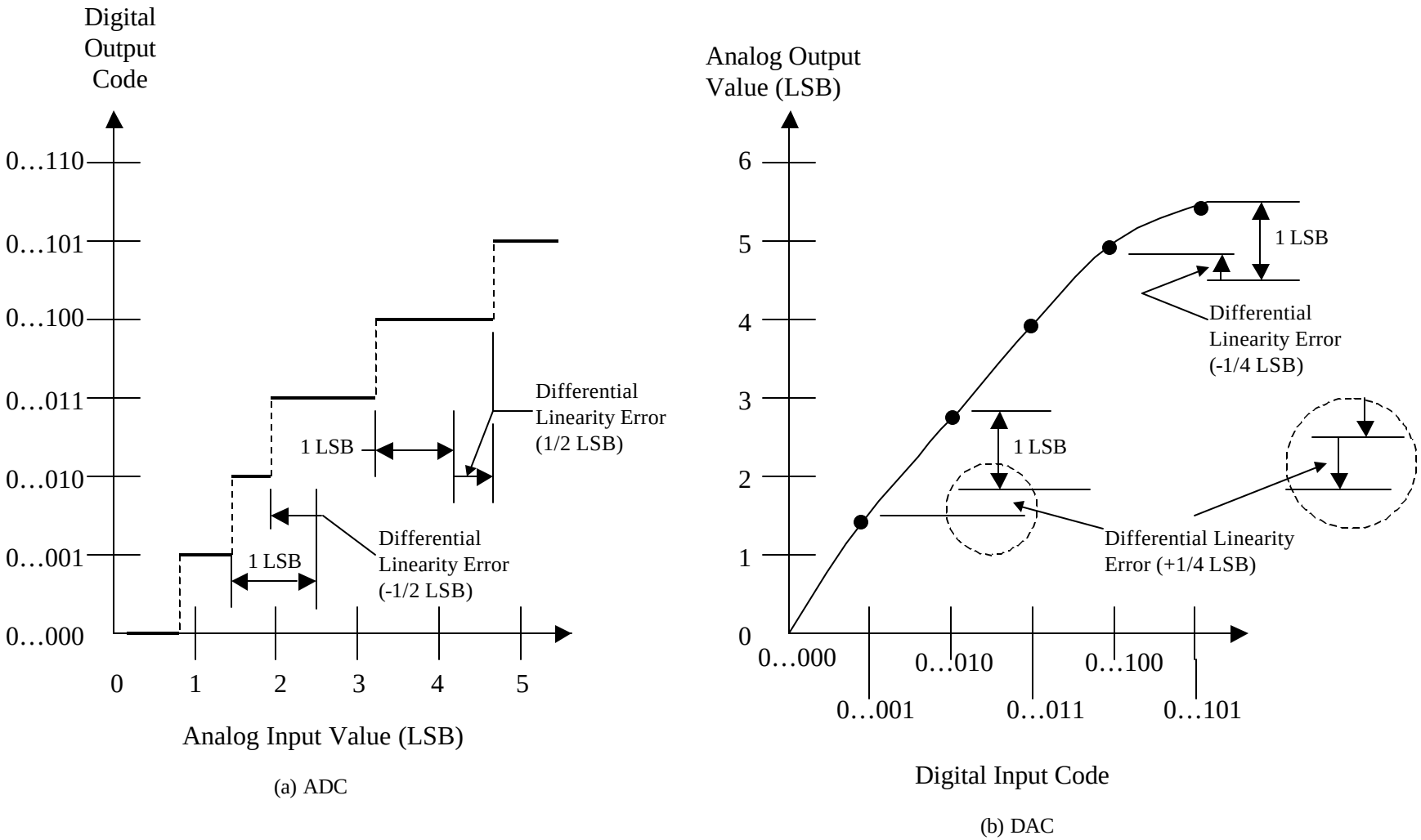
Integral Nonlinearity (INL) Error

The integral non-linearity depicts a possible distortion of the input-output transfer characteristic and leads to harmonic distortion.



End-Point Linearity Error of a Linear 3-bit Natural Binary-Coded ADC or DAC
(Offset Error and Gain Error are Adjusted to the Value Zero)

Differential Nonlinearity (DNL)



Differential Linearity Error of a Linear ADC or DAC

Numerical Examples [1]

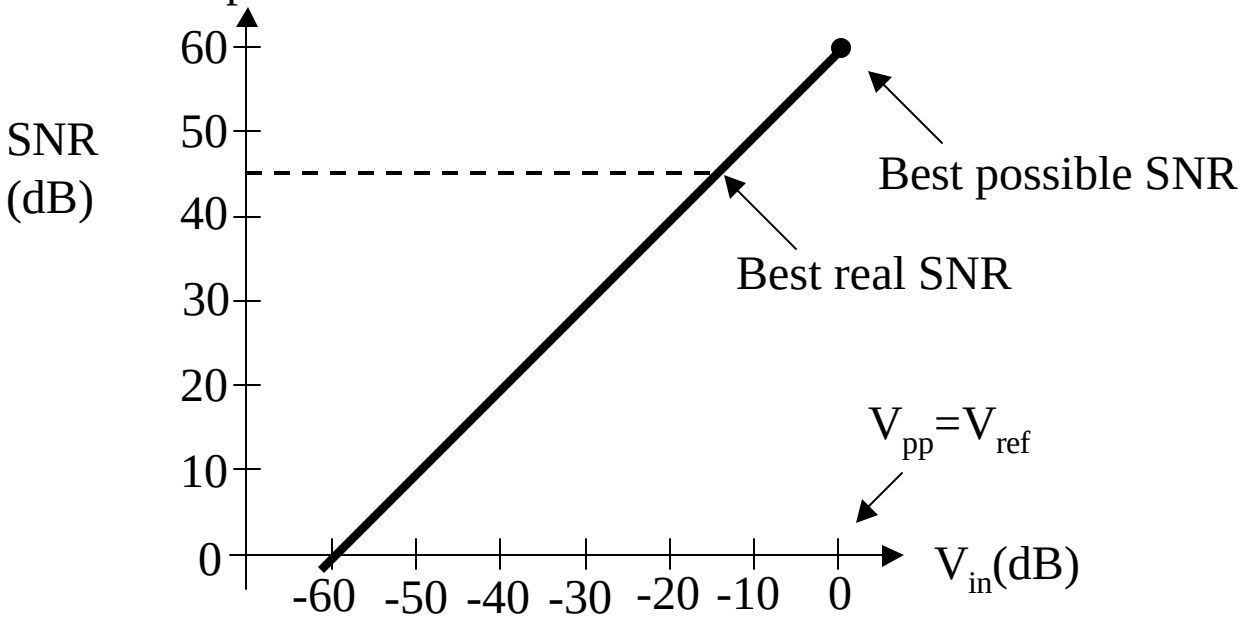
Example 1.

A 100-mV_{pp} sinusoidal signal is applied to an ideal 12-bit A/D converter for which V_{ref}= 5 V. Find the SNR of the digitized output signal.

$$\text{SNR} = 20\log\left(\frac{V_{in}(\text{rms})}{V_Q(\text{rms})}\right) = 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(\sqrt{\frac{3}{2}}2^N\right)\pm$$

Solution

First, we use to find the maximum SNR if a full-scale sinusoidal wave-form of 2.5 V were applied to the input.



Idealized SNR versus sinusoidal input signal amplitude for a 10-bit A/D converter. The 0-dB input signal amplitude corresponds to a peak-to-peak voltage equaling V_{ref}.

$$\text{SNR}_{max} = 6.02N + 1.76\,\text{dB} = 6.02\times 12 + 1.76 = 74\,\text{dB}$$

However, since the input is only a $\pm$100-mV sinusoidal waveform that is 28 dB below full scale, the SNR of the digitized output is

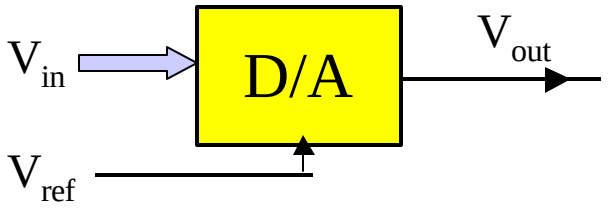
$$\text{SNR} = 74 - 28 = 46\,\text{dB}$$

Example 2. $V_{LSB} = \frac{V_{ref}}{2^N}$, $1\,\text{LSB} = \frac{1}{2^N}$

Consider a 3-bit D/A converter in which V_{ref} = 4 V, with the following measured voltage values:

{ 0.011 : 0.507 : 1.002 : 1.501 : 1.996 : 2.495 : 2.996 : 3.491 }

1. Find the offset and gain errors in units of LSBs.
2. Find the INL (endpoint) and DNL errors (in units of LSBs).
3. Find the effective number of bits of absolute accuracy.
4. Find the effective number of bits of relative accuracy.



Solution

We first note that 1 LSB corresponds to $V_{ref}/2^3 = 0.5$ V.

1. Since that offset voltage is 11 mV, and since 0.5 V corresponds to 1 LSB, we see that the offset error is given by

$$E_{off\ (D/A)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0} = \frac{0.011}{0.5} = 0.022\ \text{LSB}$$

For the gain error, from (11.25) we have

$$E_{gain\,(D/A)} = \left(\left.\frac{V_{out}}{V_{LSB}}\right|_{1\ldots1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0}\right) - (2^N - 1) = \left(\frac{3.491 - 0.011}{0.5}\right) - (2^3 - 1) = -0.04\ \text{LSB}$$

2. For INL and DNL errors, we first need to remove both offset and gain errors in the measured D/A values. The offset error is removed by subtracting 0.022 LSB off each value, whereas the gain error is eliminated by subtracting off scaled values of the gain error. For example, the new value for 1.002 (scaled to 1 LSB) is given by

$$\frac{1.002}{0.5} - 0.022 + \left(\frac{2}{7}\right)(0.04) = 1.993$$

Thus, the offset-free, gain-free, scaled values are given by

{ 0.0 : 0.998 : 1.993 : 2.997 : 3.993 : 4.997 : 6.004 : 7.0 }

Since these results are in units of LSBs, we calculate the INL errors as the difference between these values and the ideal values, giving us

INL errors : { 0 : -0.002 : -0.007 : -0.003 : -0.007 : -0.003 : 0.004 : 0 }

For DNL errors, we find the difference between adjacent offset-free, gain-free, scaled values to give

DNL errors: { -0.002 : -0.005 : 0.004 : -0.004 : 0.004 : 0.007 : -0.004 }

3. For absolute accuracy, we find the largest deviation between the measured values and the ideal values, which, in this case, occurs at 0 V and is 11 mV. To relate this 11-mV value to effective bits, 11 mV should correspond to 1 LSB when V_{ref} = 4 V. In other words, we have the relationship

$$\frac{4\text{V}}{2^{N_{eff}}} = 11\text{mV}$$

which results in an absolute accuracy of N_{abs} = 8.5 bits.

4. For relative accuracy, we use the INL errors found in part 2, whose maximum magnitude is 0.007 LSB, or equivalently, 3.5 mV. We relate this 3.5-mV value to effective bits in the same manner as in part 3, resulting in a relative accuracy of N_{rel} = 10.2 nits.

Example 3 [Johns & Martin]

A full-scale sinusoidal waveform is applied to a 12-bit A/D converter, and the output is digitally analyzed. If the fundamental has a normalized power of 1 W while the remaining power is 0.5 μW, what is the effective number of bits for the converter?

Solution

Using the expression for the SNR, we have

$$\text{SNR} = 6.02\,\text{N}_{\text{eff}} + 1.76$$

In this case, the signal-to-noise ration is found to be

$$\text{SNR} = 10\log\left(\frac{\text{P}_{\text{fund.}}}{\text{P}_{\text{rema}}}\right) = 10\log\left(\frac{1}{0.5\times 10^{-6}}\right) = 63\,\text{dB}$$

Substituting this SNR value into the SNR expression yields

$$\text{N}_{\text{eff}} = \frac{63 - 1.76}{6.02} = 10.2 \;\; \text{effective} \;\; \text{bits}$$

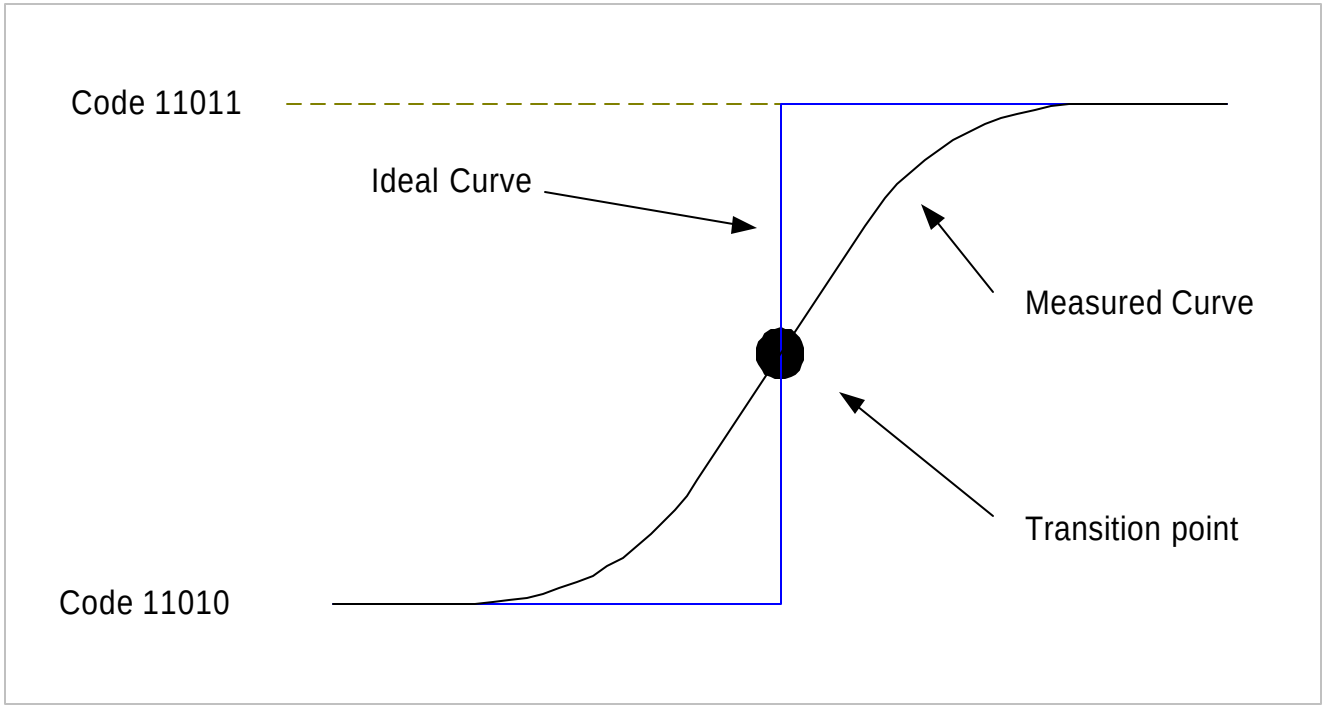
Measure Static Performance

The first step is to find each transition point;

- The real transition is not instantaneous. The transition point is half way between 2 consecutive codes
- Once all the transition points are recorded, the static parameters can be computed by a set of equations
- three different static performance measurement methods are described

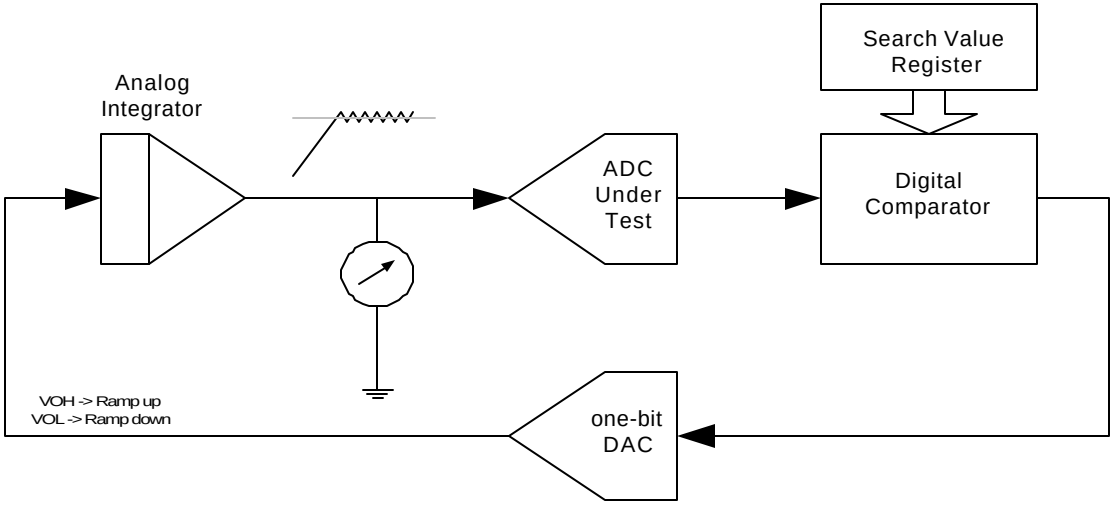
Method 1:manual measurement

- Increase the analog input to the ADC slowly until we can make the digital output 1 LSB more,from 11010 to 11011
- write down the correspond analog input value V1
- decrease the analog input to the ADC slowly until we can make the digital output return to the 11010
- write down the correspond analog input value V2
- The transition point between 11010 and 11011 is 0.5(V1+V2)



Method 2:The Servo Method

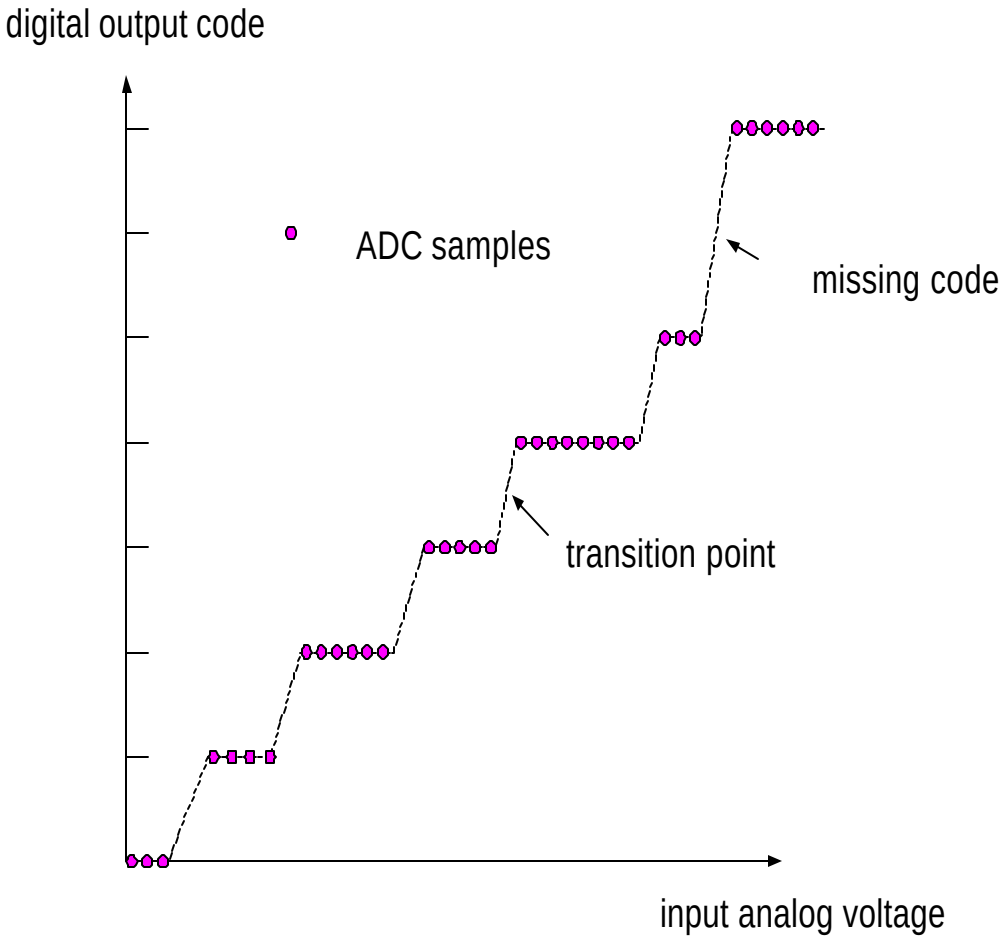
- The Servo method is an automated technique to easily find the transition points
- for example,we need the transition point between 11010 and 11011.We should set search value register as 11010
- close the loop;when the circuit is stable,use a DC voltmeter to measure the analog value at the output of the integrator.It is the transition point between 11010 and 11011



Method 3:The Linear Ramp Histogram

- The histogram is best suited for automated testing of ADCs in the industry
- A linear ramp is sent to the ADC under test and the output codes are sampled and recorded
- The input ramp must be very slow, such that we get at least 16 samples per output code
- This allows a precise evaluation of the static performances.

Method 3:The linear Ramp Histogram (continued)



- Record the samples per digital code
- use the recorded values to compute the transition point one by one

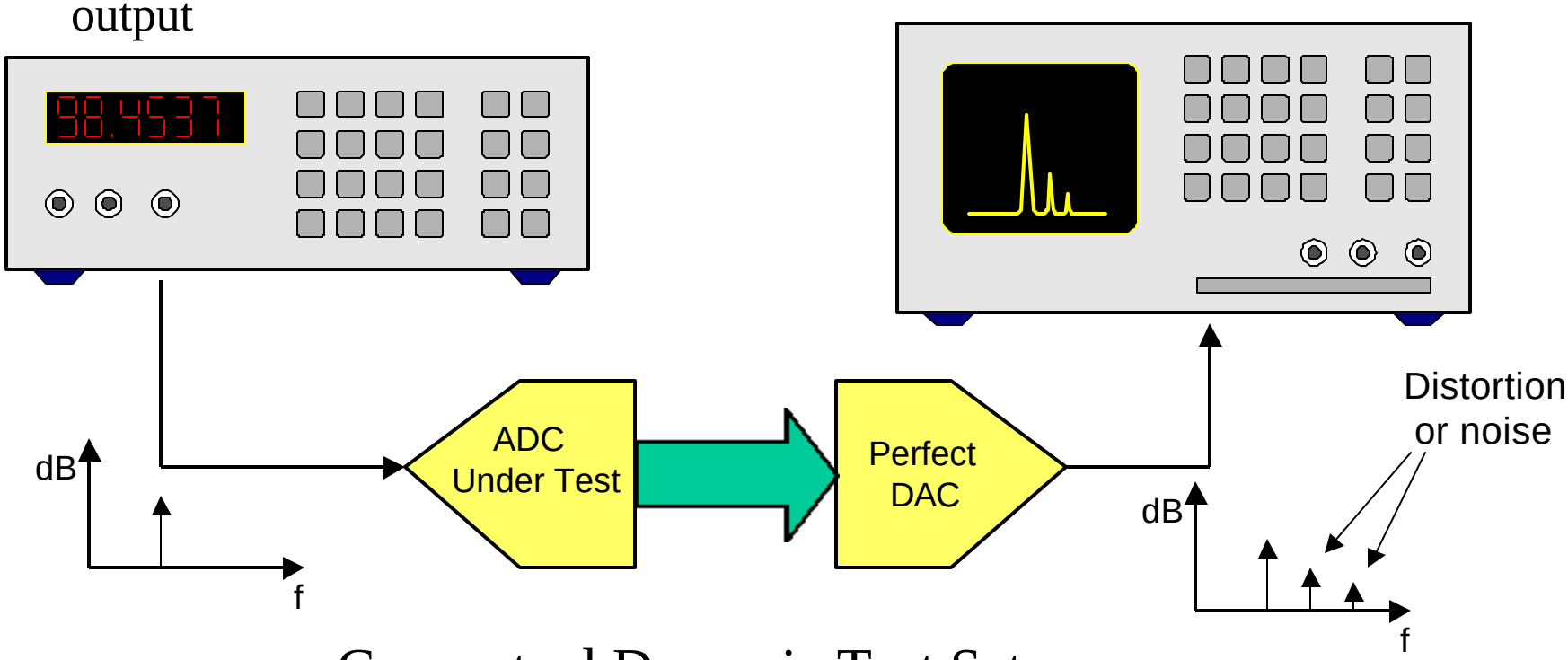
Calculate static parameters from transition points

- Use TP as the symbol of the transition point,and assume TP[i] is the transition point between code i-1 and code I
- Offset = TP[1]-0.5 $\left(\frac{FSR}{2^N}\right)$ FSR is the full scale input range; N is ADC resolution
- Gain Error= $\left|\left(\frac{TP[2\text{^}N-1]-TP[1]}{FSR\times\left[\frac{2\text{^}N-2}{2\text{^}N}\right]}\right)-1\right|\times 100$
- Differential Non-linearity
- DNL[i]= $\frac{TP[i+1]-TP[i]}{LSB}$ -1
- Integral Non-linearity

INL[i]= $\frac{TP[i]-(LSB\times(i-1)+TP[1])}{LSB}$

Dynamic Performance Measurement

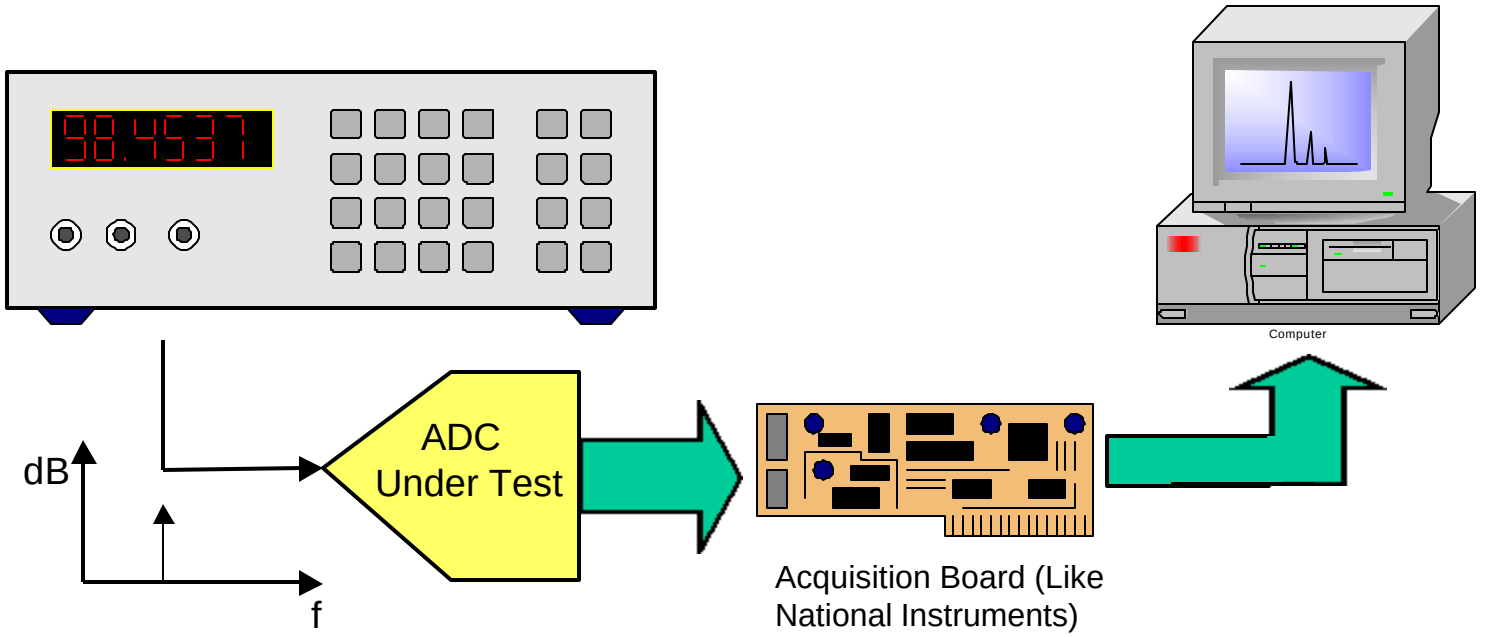
- The most typical dynamic performance measurement consists of looking for distortion in the frequency domain
- This is done by sending a pure sinusoidal input and looking at the output



Conceptual Dynamic Test Setup

Real Measurement of Dynamic Performance

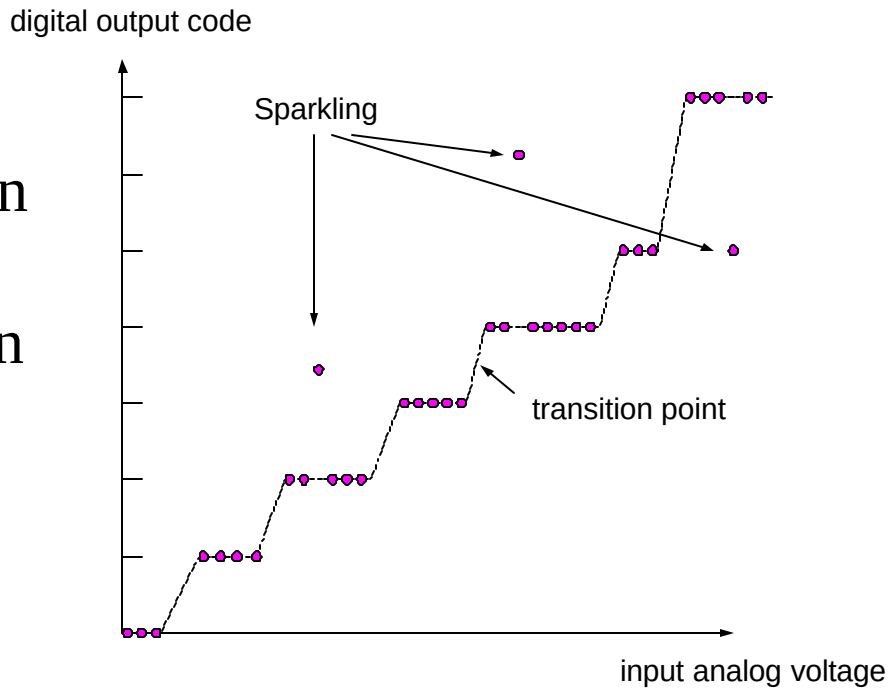
- There is no such thing as a perfect DAC…
- To improve the precision and simplify the post-processing, all the spectrum analysis is done in digital form and in software.



Other Dynamic Measurements

- All the timing and control signals (i.e. Convert, Data_Ready, Read, Data, …) must be tested at full speed to ensure their functionality,

- The output from a sinewave input can also be observed in time-domain to make sure there is no sparkling (sudden out-of-range samples).



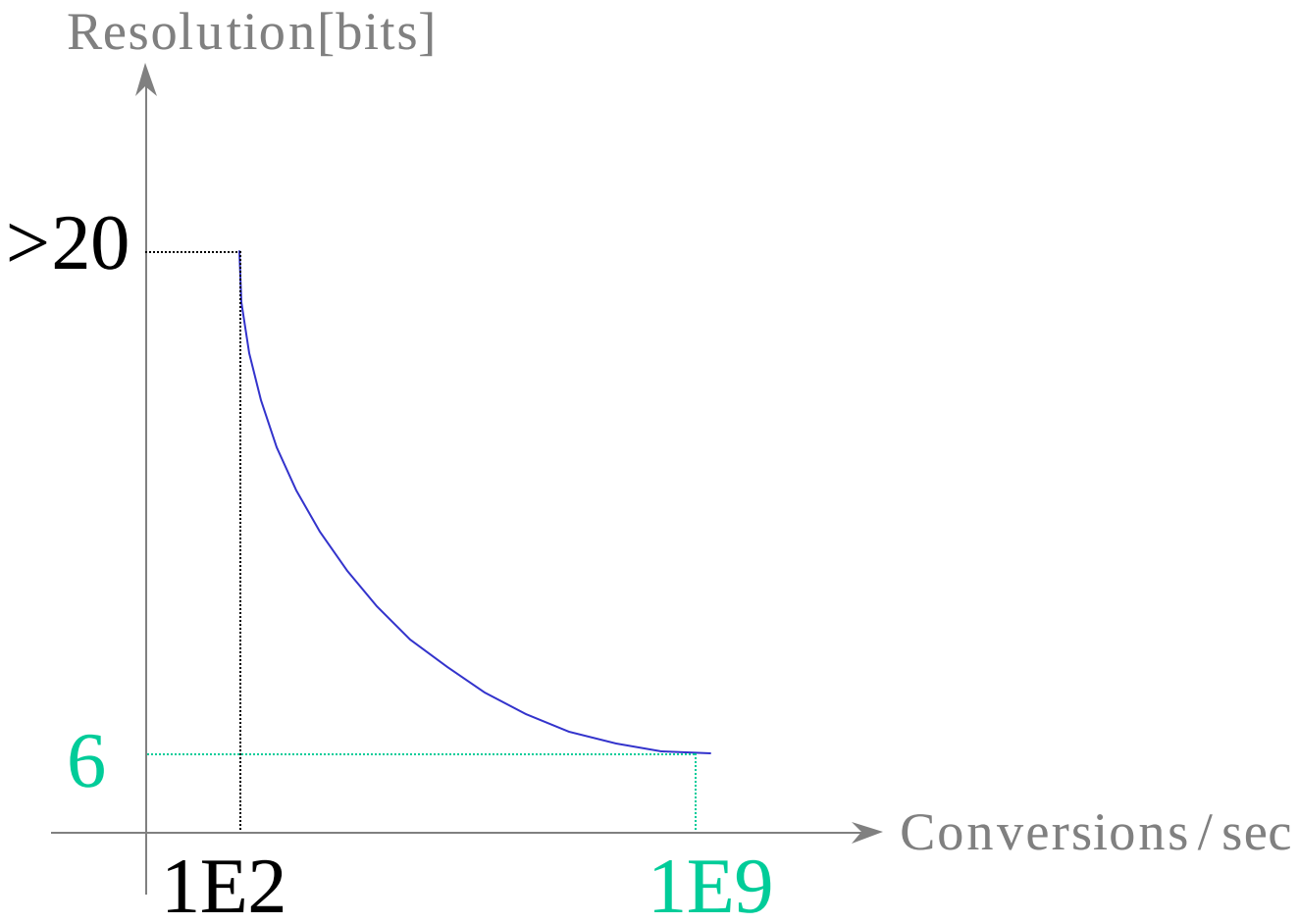
An illustrative example/comparison:

A/D Conversion : Practical Techniques

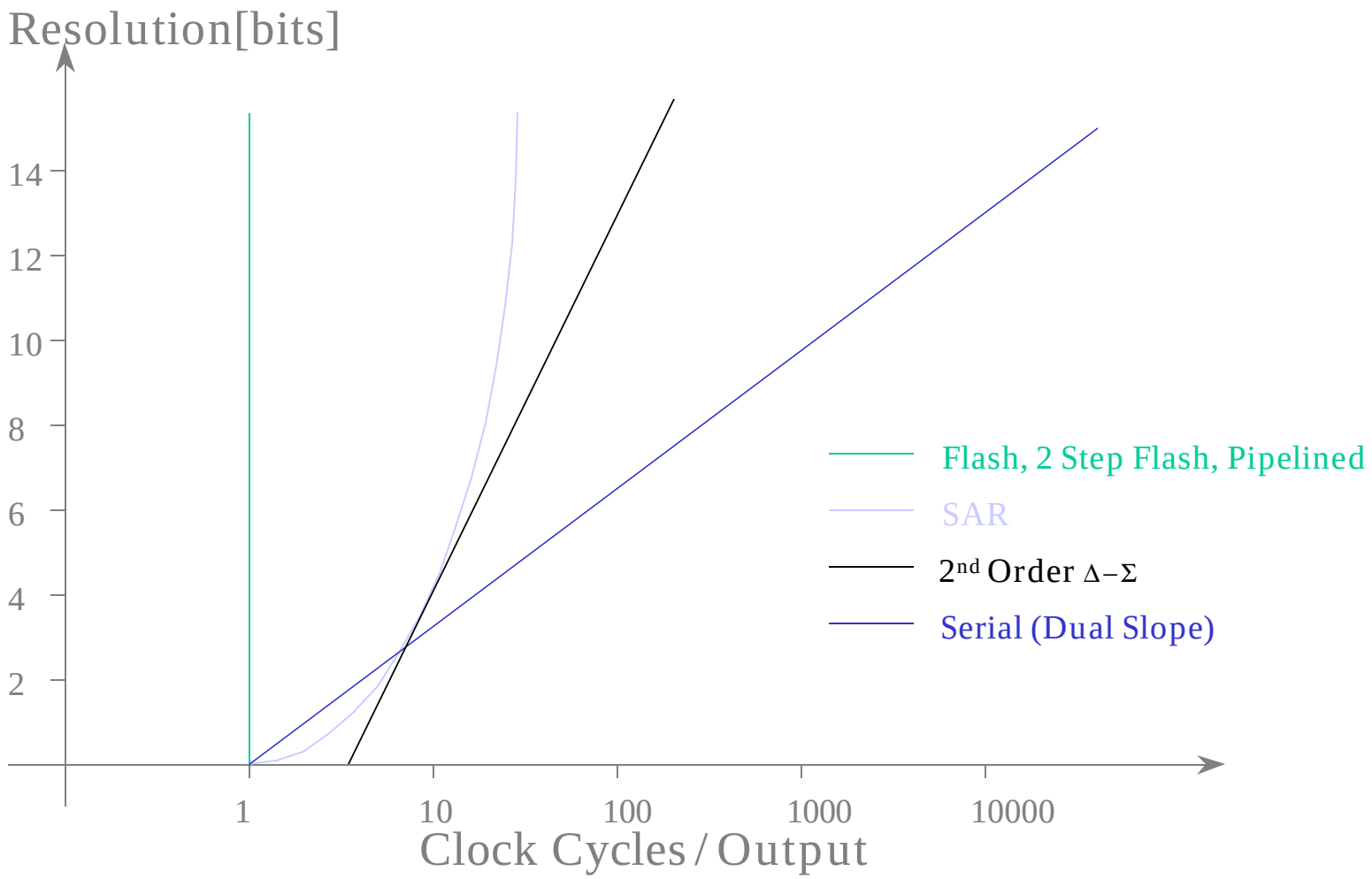
- Serial Conversion:
  Dual Slope
- Successive
  Approximation

- Parallel Conversion:
  Flash
- Quantized Feedforward:
  Pipelined
- Quantized Feedback:
  Delta-Sigma

Speed vs. Resolution



Throughput Rate Comparison of ADCs



An A/D Conversion Classification

Multiplexing

- Time Interweave
- Pipeline

Parallel

- Flash
- Stacking Flash
- Neural Network

Series-Parallel

- Subranging
- Subranging with Folding Amps
- Ripple

Serial

- Non-Algorithmic
  - Successive Approximation
  - Charge Redistribution
  - Variable Ref. Serial Ripple
- Algorithmic Iterative
  - Cyclic
  - Sample/Hold
- Algorithmic Replicative
  - Straight Binary
  - Gray

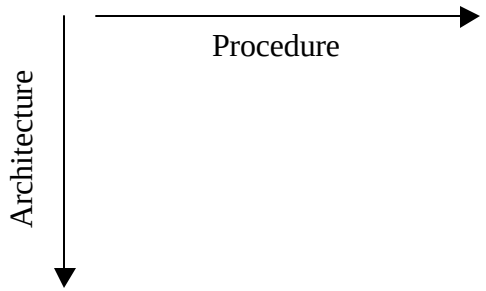
Coarse-Fine

- Coarse-Fine

Counting

- Pulse Width
  - Ramp Comparison
  - Dual Slopes
  - Constant Slope
- Pulse Rate
  - Ramp Comparison
  - Quantized Feedback
- Tracking Feedback
  - Servo
  - Delta Modulation

Note: The procedure and architecture are shown as



Coarse List of A/D Converter Architectures

Low-to-Medium Speed High-Accuracy	Medium Speed Medium Accuracy	High-Speed Low-to-Medium Accuracy
Integrating	Successive Approximation	Flash
Oversampling	Algorithmic	Two-Step
		Interpolating
		Folding
		Pipelined
		Time-Interleaved

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