Abstract

This application note presents practical design considerations for battery chargers employing Green Mode FPS (Fairchild Power Switch). It includes designing the transformer and output filter, selecting the components and implementing constant current / constant voltage control.

The step-by-step design procedure described in this paper will help engineers design battery chargers more easily. In order to make the design process more efficient, a software design tool, FPS design assistant that contains all the equations described in this paper is also provided. The design procedure is verified through an experimental prototype converter.

1. Introduction

As penetration rates of portable electronics devices such as cellular phones, digital cameras or PDAs have increased significantly, the demands for low cost battery chargers are rising these days. Fairchild Power Switch (FPS) reduces total component count, design size, weight and, at the same time increases efficiency, productivity, and system reliability when compared to a discrete MOSFET and controller or RCC switching converter solution. Table 1 shows the FPS lineup for a battery charger application. Figure 1 shows the schematic of the basic battery charger using FPS, which also serves as the reference circuit for the design process described in this paper. An experimental flyback converter from the design example has been built and tested to show the validity of the design procedure.

<table>
<thead>
<tr>
<th>Device</th>
<th>Switching frequency</th>
<th>Current limit</th>
<th>R_{dson} (typ.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSDH0165</td>
<td>100 kHz</td>
<td>0.35 A</td>
<td>15.6 Ω</td>
</tr>
<tr>
<td>FSD311</td>
<td>67 kHz</td>
<td>0.55 A</td>
<td>14 Ω</td>
</tr>
<tr>
<td>FSD200</td>
<td>134 kHz</td>
<td>0.32 A</td>
<td>28 Ω</td>
</tr>
<tr>
<td>FSD210</td>
<td>134 kHz</td>
<td>0.32 A</td>
<td>28 Ω</td>
</tr>
</tbody>
</table>

Table 1. FPS lineup for a battery charger
2. Step-by-step Design Procedure

1. Determine the system specifications
   \((V_{line min}, V_{line max}, f_L, P_o, E_ff)\)

2. Determine DC link capacitor \((C_{DC})\) and DC link voltage range

3. Determine the reflected output voltage \((V_{ref})\)

4. Determine the transformer primary side inductance \((L_{sw})\) and maximum duty \((D_{max})\)

5. Choose proper FPS considering input power and \(I_{ds peak}\)

6. Determine the proper core and the minimum primary turns \((N_{p min})\)

7. Determine the number of turns for each output

8. Determine the wire diameter for each winding

   Is the winding window area \((A_w)\) enough ?

   Y

   Is it possible to change the core?

   Y

9. Choose the proper rectifier diode for each output

10. Determine the output capacitor

11. Design the RCD snubber

12. Control Circuit design

   Design finished

Figure 2. Flow chart of design procedure

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. Figure 2 illustrates the design flow chart. The detailed design procedures are as follows:

(1) STEP-1 : Define the system specifications
- Line voltage range \((V_{line min} \text{ and } V_{line max})\).
- Line frequency \((f_L)\).
- Maximum output power \((P_o)\).
- Estimated efficiency \((E_ff)\) : It is required to estimate the power conversion efficiency to calculate the maximum input power. In the case of a battery charger, the efficiency is relatively low due to the low output voltage and loss in the output current sense resistor. The typical efficiency is about 0.65-0.7.

With the estimated efficiency, the maximum input power is given by

\[ P_{in} = \frac{P_o}{E_{ff}} \]  

(1)

(2) STEP-2 : Determine DC link capacitor \((C_{DC})\) and the DC link voltage range.

It is typical to select the DC link capacitor as 2-3uF per watt of input power for universal input range (85-265Vrms) and 1uF per watt of input power for European input range (195V-265Vrms). With the DC link capacitor chosen, the minimum link voltage is obtained as

\[ V_{DC min} = \frac{2 \cdot (V_{line min})^2 \cdot (1 - D_{ch})}{C_{DC} \cdot f_L} \]  

(2)

where \(D_{ch}\) is the DC link capacitor charging duty ratio defined as shown in Figure 3, which is typically about 0.2 and \(P_{in}, V_{line min}\) and \(f_L\) are specified in step-1.

The maximum DC link voltage is given as

\[ V_{DC max} = \sqrt{2} V_{line max} \]  

(3)

where \(V_{line max}\) is specified in step-1.

Figure 3. DC Link Voltage Waveform
(3) STEP-3 : Determine the reflected output voltage (V_{RO}).

When the MOSFET in the FPS is turned off, the input voltage (V_{DC}) together with the output voltage reflected to the primary (V_{RO}) are imposed on the MOSFET as shown in Figure 4. After determining V_{RO}, the maximum nominal MOSFET voltage (V_{ds,\text{nom}}) is obtained as

\[ V_{ds,\text{nom}} = V_{DC,\text{max}} + V_{RO} \]  

(4)

where \(V_{DC,\text{max}}\) is specified in equation (3). The typical value for \(V_{RO}\) is 65-85V.

(4) STEP-4 : Determine the transformer primary side inductance (L_m) and the maximum duty ratio (D_{max}).

A Flyback converter has two kinds of operation modes; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The operation changes between CCM and DCM as the load condition and input voltage vary and each operation mode has its own advantages and disadvantages, respectively. The transformer size can be reduced using DCM because the average energy stored is lower compared to CCM. However, DCM inherently causes higher RMS current, which increases the conduction loss of the MOSFET and the current stress on the output capacitors. For low power applications under 10W where the MOSFET conduction loss is not so severe, it is typical to design the converter to operate in DCM for the entire operating range, or to operate in CCM only for low input voltage conditions in order to minimize the transformer size.

The design procedures for CCM and DCM are slightly different. Once the reflected output voltage (V_{RO}) is determined in step-3, the flyback converter can be simplified as shown in Figure 5 by neglecting the voltage drops in MOSFET and diode.

For CCM operation, the maximum duty ratio is given by

\[ D_{\text{max}} = \frac{V_{RO}}{V_{RO} + V_{DC,\text{min}}} \]  

(5)

where \(V_{DC,\text{min}}\) and \(V_{RO}\) are specified in equations (2) and step-3, respectively.

For DCM operation, the maximum duty ratio should be determined as smaller than the value obtained in equation (5). By reducing \(D_{\text{max}}\), the transformer size can be reduced. However, this increases the RMS value of the MOSFET drain current and \(D_{\text{max}}\) should be determined by trade-off between the transformer size and MOSFET conduction loss.

With the maximum duty ratio, the primary side inductance (L_m) of the transformer is obtained. The worst case in designing L_m is full load and minimum input voltage.
condition. Therefore, \( L_m \) is obtained in this condition as

\[
L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2P_{in}^2 \cdot K_{RF}}  \tag{6}
\]

where \( V_{DC}^{min} \) is specified in equation (2), \( D_{max} \) is specified in equation (5), \( P_{in} \) is specified in step-1, \( f_s \) is the switching frequency of the FPS device and \( K_{RF} \) is the ripple factor in full load and minimum input voltage condition, defined as shown in Figure 6. For DCM operation, \( K_{RF} = 1 \) and for CCM operation \( K_{RF} < 1 \). The ripple factor is closely related to the transformer size and the RMS value of the MOSFET current. In the case of low power applications such as battery chargers, a relatively large ripple factor is used in order to minimize the transformer size. It is typical to set \( K_{RF} = 0.5-0.7 \) for the universal input range and \( K_{RF} = 1.0 \) for the European input range.

Once \( L_m \) is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as

\[
I_{ds}^{peak} = I_{EDC} + \frac{\Delta I}{2}  \tag{7}
\]

\[
I_{ds}^{rms} = \sqrt{3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2 \cdot D_{max}} / 3  \tag{8}
\]

\[
I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \tag{9}
\]

\[
\Delta I = \frac{V_{DC}^{min} \cdot D_{max}}{L_m f_s}  \tag{10}
\]

where \( P_{in}, V_{DC}^{min}, D_{max} \) and \( L_m \) are specified in equations (1), (2), (5) and (6) respectively and \( f_s \) is the FPS switching frequency.

(5) STEP-5 : Choose the proper FPS considering input power and peak drain current.

With the resulting maximum peak drain current of the MOSFET \((I_{ds}^{peak})\) from equation (7), choose the proper FPS of which the pulse-by-pulse current limit level \((I_{over})\) is higher than \(I_{ds}^{peak}\). Since FPS has ±12% tolerance of \(I_{over}\), there should be some margin in choosing the proper FPS device.

(6) STEP-6 : Determine the proper core and the minimum primary turns.

Table 2 shows the commonly used cores for battery chargers with output power under 10W. The cores recommended in table 2 are typical for the universal input range and 100kHz switching frequency. With the chosen core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by

\[
N_P^{min} = \frac{L_m I_{over}}{B_{sat} A_e} \times 10^6 \text{ (turns)}  \tag{11}
\]

where \( L_m \) is specified in equation (6), \( I_{over} \) is the FPS pulse-by-pulse current limit level, \( A_e \) is the cross-sectional area of the core as shown in Figure 7 and \( B_{sat} \) is the saturation flux density in tesla. Figure 8 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density \( (B_{sat}) \) decreases as the temperature goes high, the high temperature characteristics should be considered. If there is no reference data, use \( B_{sat} = 0.3-0.35 \) T. Since the MOSFET drain current exceeds \( I_{ds}^{peak} \) and reaches \( I_{over} \) in a transition or fault condition, \( I_{over} \) is used in equation (11) instead of \( I_{ds}^{peak} \) to prevent core saturation during transition.
Figure 8. Typical B-H characteristics of ferrite core (TDK/PC40)

![Typical B-H characteristics of ferrite core (TDK/PC40)](image)

Table 2. Typical cores for battery charger (For universal input range, 5V output and fs=100kHz)

<table>
<thead>
<tr>
<th>Core</th>
<th>Cross sectional area</th>
<th>Window area</th>
<th>Output power range</th>
</tr>
</thead>
<tbody>
<tr>
<td>EE13-Z</td>
<td>17.1 mm²</td>
<td>33.4 mm²</td>
<td>3-5W</td>
</tr>
<tr>
<td>EI16-Z</td>
<td>19.8 mm²</td>
<td>38.8 mm²</td>
<td>3-5W</td>
</tr>
<tr>
<td>EE16-Z</td>
<td>21.7 mm²</td>
<td>51.3 mm²</td>
<td>5-10W</td>
</tr>
<tr>
<td>EI19-Z</td>
<td>24.0 mm²</td>
<td>54.4 mm²</td>
<td>5-10W</td>
</tr>
</tbody>
</table>

(7) STEP-7 : Determine the number of turns for each output

Figure 9 shows the simplified diagram of the transformer. First, determine the turns ratio (n) between the primary side and the secondary side.

\[ n = \frac{N_p}{N_s} = \frac{V_{RO}}{V_o + V_F + V_{sense}} \]  

(12)

where \( N_p \) and \( N_s \) are the number of turns for primary side and reference output, respectively, \( V_o \) is the output voltage, \( V_F \) is the diode \( (D_R) \) forward voltage drop and \( V_{sense} \) is the maximum voltage drop in the output current sensing resistor.

Then, determine the proper integer for \( N_s \) so that the resulting \( N_p \) is larger than \( N_p^{\text{min}} \) obtained from equation (11).

The number of turns for Vcc winding is determined as

\[ N_a = \frac{V_{cc^*} + V_{Fa}}{V_o + V_F} \cdot N_s \] (turns)  

(13)

where \( V_{cc^*} \) is the nominal value of the supply voltage of the FPS device, and \( V_{Fa} \) is the forward voltage drop of \( D_a \) as defined in Figure 9. Since \( V_{cc} \) increases as the output load increases, it is proper to set \( V_{cc^*} \) as \( V_{cc} \) start voltage (refer to the data sheet) to avoid triggering the over voltage protection during normal operation.

![Simplified diagram of the transformer](image)

Figure 9. Simplified diagram of the transformer

With the determined turns of the primary side, the gap length of the core is obtained as

\[ G = 40\pi A_e \left( \frac{N_p^2}{1000L_m} - \frac{1}{A_L} \right) \] (mm)  

(14)

where \( A_L \) is the AL-value with no gap in nH/turns², \( A_e \) is the cross sectional area of the core as shown in Figure 8, \( L_m \) is specified in equation (6) and \( N_p \) is the number of turns for the primary side of the transformer.

(8) STEP-8 : Determine the wire diameter for each winding based on the rms current of each output.

The rms current of the n-th secondary winding is obtained as

\[ I_{s}^{\text{rms}} = I_{ds}^{\text{rms}} \left( \frac{1 - D_{\text{max}}}{D_{\text{max}}} \right) \frac{V_{RO}}{(V_o + V_F)} \]  

(15)

where \( V_{RO} \) and \( I_{ds}^{\text{rms}} \) are specified in step-3 and equations (8), \( V_o \) is the output voltage, \( V_F \) is the diode \( (D_R) \) forward voltage drop and \( D_{\text{max}} \) is specified in equation (5).

The current density is typically 5A/mm² when the wire is
long (>1 m). When the wire is short with a small number of turns, a current density of 6-10 A/mm² is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier. For high current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core, \( A_w \) (refer to Figure 8) is enough to accommodate the wires. Because bobbin, insulation tape and gaps between wires, the wire cannot fill the entire winding window area. Typically the fill factor is about 0.15-0.2 for a battery charger. When additional dummy windings are employed for EMI shielding, the fill factor is reduced. The required winding window area \( (A_{wr}) \) is given by

\[
A_{wr} = A_c/K_F
\]

where \( A_c \) is the actual conductor area and \( K_F \) is the fill factor. If the required window \( (A_{wr}) \) is larger than the actual window area \( (A_w) \), go back to the step-6 and change the core to a bigger one. Sometimes it is impossible to change the core due to cost or size constraints. If so, go back to step-4 and reduce \( L_m \) by increasing the ripple factor \( (K_{RF}) \) or reducing the maximum duty ratio. Then, the minimum number of turns for the primary \( (N_{p_{\text{min}}}) \) of the equation (11) will decrease, which results in the reduced required winding window area \( (A_{wr}) \).

(9) STEP-9 : Choose the rectifier diode in the secondary side based on the voltage and current ratings.

The maximum reverse voltage and the rms current of the output rectifier diode \( (D_R) \) are obtained as

\[
V_D = V_o + V_{DC_{\text{max}}} = \frac{V_o + V_F + V_{\text{sense}}}{V_{RO}}
\]

\[
I_{D_{\text{rms}}} = I_{ds_{\text{rms}}} = \sqrt{\frac{V_{DC_{\text{min}}}}{V_{RO}}} = \sqrt{\frac{(V_o + V_F + V_{\text{sense}})}{V_{RO}}}
\]

where \( V_{DC_{\text{max}}} \), \( D_{\text{max}} \) and \( I_{ds_{\text{rms}}} \) are specified in equations (3), (5) and (8), respectively, \( V_o \) is the output voltage, \( V_F \) is the diode \( (D_R) \) forward voltage and \( V_{\text{sense}} \) is the maximum voltage drop in the output current sensing resistor.

The typical voltage and current margins for the rectifier diode are as follows

\[
V_{\text{RRM}} > 1.3 \cdot V_D
\]

\[
I_F > 1.5 \cdot I_{D_{\text{rms}}}
\]

where \( V_{\text{RRM}} \) is the maximum reverse voltage and \( I_F \) is the average forward current of the diode.

A quick selection guide for Fairchild Semiconductor rectifier diodes is given in table 3.

<table>
<thead>
<tr>
<th>Products</th>
<th>( V_{\text{RRM}} )</th>
<th>( I_F )</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB340</td>
<td>40 V</td>
<td>3 A</td>
<td>TO-210AD</td>
</tr>
<tr>
<td>SB350</td>
<td>50 V</td>
<td>3 A</td>
<td>TO-210AD</td>
</tr>
<tr>
<td>SB360</td>
<td>60 V</td>
<td>3 A</td>
<td>TO-210AD</td>
</tr>
</tbody>
</table>

Table 3. Fairchild Diode quick selection table

(10) STEP-10 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the output capacitor \( (C_o) \) is obtained as

\[
I_{\text{cap}_{\text{rms}}} = \sqrt{(I_{D_{\text{rms}}}^2 - I_o^2)}
\]

where \( I_o \) is the load current and \( I_{D_{\text{rms}}} \) is specified in equation (18). The ripple current should be smaller than the ripple current specification of the capacitor. The voltage ripple on the n-th output is given by

\[
\Delta V_o = \frac{I_o D_{\text{max}}}{C_o I_s} \cdot \frac{I_{ds_{\text{peak}}} V_{RO} R_L}{(V_o + V_F + V_{\text{sense}})}
\]

where \( C_o \) is the output capacitance, \( R_L \) is the effective series resistance (ESR) of the output capacitor, \( D_{\text{max}} \) and \( I_{ds_{\text{peak}}} \) are specified in equations (5) and (7), respectively, \( I_o \) and \( V_o \) are the load current and output voltage, respectively. \( V_F \) is the diode \( (D_R) \) forward voltage and \( V_{\text{sense}} \) is the maximum voltage drop in the output current sensing resistor.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10-1/5 of the switching frequency.

(11) STEP-11 : Design the RCD snubber.

When the power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of the FPS. Therefore, it is necessary to use an additional network to clamp the voltage.

The RCD snubber circuit and MOSFET drain voltage waveform are shown in Figure 10 and 11, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode \( (D_{sn}) \) once the MOSFET drain voltage exceeds the voltage of node X as depicted in Figure 10. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching
cycle. The snubber capacitor used should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable due to these reasons.

The first step in designing the snubber circuit is to determine the snubber capacitor voltage at the minimum input voltage and full load condition ($V_{sn}$). Once $V_{sn}$ is determined, the power dissipated in the snubber network at the minimum input voltage and full load condition is obtained as

$$P_{sn} = \frac{(V_{sn})^2}{R_{sn}} = \frac{1}{2} f_s L_{lk} (I_{ds_{peak}})^2 \frac{V_{sn}}{V_{sn} - V_{RO}}$$

(23)

where $I_{ds_{peak}}$ is specified in equation (8), $f_s$ is the FPS switching frequency, $L_{lk}$ is the leakage inductance, $V_{sn}$ is the snubber capacitor voltage at the minimum input voltage and full load condition, $V_{RO}$ is the reflected output voltage and $R_{sn}$ is the snubber resistor. $V_{sn}$ should be larger than $V_{RO}$ and it is typical to set $V_{sn}$ to be 2~2.5 times $V_{RO}$. Too small a $V_{sn}$ results in a severe loss in the snubber network as shown in equation (23). The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted.

Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as

$$AV_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_s}$$

(24)

where $f_s$ is the FPS switching frequency. In general, 5~10% ripple of the selected capacitor voltage is reasonable.

The snubber capacitor voltage ($V_{sn}$) of equation (26) is for the minimum input voltage and full load condition. When the converter is designed to operate in CCM under this condition, the peak drain current together with the snubber capacitor voltage decrease as the input voltage increases as shown in Figure 11. The peak drain current at the maximum input voltage and full load condition ($I_{ds_{peak}}$) is obtained as

$$I_{ds_{peak}} = \frac{2 \cdot P_{in}}{L_{sn} f_s}$$

(25)

where $P_{in}$ and $L_{sn}$ are specified in equations (1) and (6), respectively and $f_s$ is the FPS switching frequency.

The snubber capacitor voltage under maximum input voltage and full load condition is obtained as

$$V_{sn2} = \frac{V_{RO} + \sqrt{(V_{RO})^2 + 2 R_{sn} L_{sn} f_s (I_{ds_{peak}})^2}}{2}$$

(26)

where $f_s$ is the FPS switching frequency, $L_{lk}$ is the primary side leakage inductance, $V_{RO}$ is the reflected output voltage and $R_{sn}$ is the snubber resistor.

From equation (26), the maximum voltage stress on the internal MOSFET is given by

$$V_{ds_{max}} = V_{DC_{max}} + V_{sn2}$$

(27)

where $V_{DC_{max}}$ is specified in equation (3).

Check if $V_{ds_{max}}$ is below 85% of the rated voltage of the MOSFET ($BV_{dss}$) as shown in Figure 12. The voltage rating of the snubber diode should be higher than $BV_{dss}$. Usually, an ultra fast diode with 1A current rating is used for the snubber network.
In the snubber design in this section, neither the lossy discharge of the inductor nor stray capacitance is considered. In the actual converter, the loss in the snubber network is less than the designed value due to these effects.

\[ V_{sn2} \quad V_{RO} \]

**Figure 12. MOSFET drain voltage and snubber capacitor voltage**

**Figure 13. Transistor and KA431 CC/CV control**

**Constant voltage (CV) control**: The voltage divider network of \( R_1 \) and \( R_2 \) should be designed to provide 2.5V to the reference pin of the KA431. The relationship between \( R_1 \) and \( R_2 \) is given by

\[
R_2 = \frac{2.5 \cdot R_1}{V_o - 2.5} \quad (28)
\]

where \( V_o \) is the output voltage. By choosing \( R_1 \) to be 2.2k\( \Omega \), \( R_2 \) is obtained as

\[
R_2 = \frac{2.5 \cdot 2.2k\Omega}{5.2V - 2.5V} = 2k\Omega
\]

The feedback capacitor \( C_F \) introduces an integrator for CV control. To guarantee stable operation, \( C_F \) of 470nF is chosen.

The resistors \( R_{bias} \) and \( R_d \) should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage for the FPS device chosen. In general, the minimum cathode voltage and current for the KA431 are 2.5V and 1mA, respectively. Therefore, \( R_{bias} \) and \( R_d \) should be designed to satisfy the following conditions.

\[
\frac{V_o - V_{OP} - 2.5}{R_d} > I_{FB} \quad (29)
\]

\[
\frac{V_{OP}}{R_{bias}} > 1mA \quad (30)
\]
where \( V_o \) is the output voltage, \( V_{OP} \) is opto-diode forward voltage drop, which is typically 1V and \( I_{FB} \) is the feedback current of FPS. With \( I_{FB}=0.25\,mA \) (FSD210), \( R_d \) and \( R_{bias} \) are determined as 56\,Ω and 510\,Ω, respectively.

**Constant Current (CC) control** : The current control circuit is shown in detail in Figure 14. The CC control is implemented using a transistor. Because the transistor base-emitter voltage drop varies with the temperature, negative thermal coefficient (NTC) thermistor is used for a temperature compensation.

![Figure 14. Current control circuit in detail](image)

When the voltage across the sensing resistor is sufficient to turn on the transistor, CC controller is enabled while CV controller is disabled. Then, the KA431 consumes very small current and most of the currents through \( R_d \) and \( R_{bias} \) flow into the collector of the transistor \( Q \). By assuming that the feedback voltage of FPS (\( V_{FB} \)) is in the middle of its operating range, half of the FPS feedback current (\( I_{FB} \)) sinks into the opto-coupler transistor. Since it is also assumed that the CTR of the opto-coupler is 100\%, the transistor collector current is given by

\[
I_C = \frac{(I_{FB} \cdot R_d) / 2 + V_{OP}}{R_{bias}} + \frac{1}{2} \cdot I_{FB} \quad (31)
\]

where \( I_{FB} \) is the feedback current of FPS, \( V_{OP} \) is opto-diode forward voltage drop, which is typically 1V.

From the circuit in Figure 14, \( I_C \) is obtained as

\[
I_C = \frac{(250\,\mu A \cdot 56\,\Omega) / 2 + 1V}{510\,\Omega} + \frac{1}{2} \cdot 250\,\mu A = 2.1\,mA
\]

By assuming that the current gain (\( \beta \)) of \( Q \) is 100, the transistor base current is obtained as

\[
I_B = I_C / \beta = \frac{2.1\,mA}{100} = 21\,\mu A \quad (32)
\]

The voltage drop in the sensing resistor (\( V_{sense} \)) should be set to be 40-100mV higher than the transistor base-emitter voltage (\( V_{BE} \)) at room temperature (25\(^\circ\)C). The actual transistor base-emitter voltage (\( V_{BE} \)) is measured at room temperature as 0.608V with \( I_C \) of 2.1mA and \( V_{sense} \) is determined to be 0.650V.

With the \( V_{sense} \) chosen, the sensing resistor (\( R_{sense} \)) is obtained as

\[
R_{sense} = \frac{V_{sense}}{I_o} = \frac{0.65V}{0.65A} = 1\,\Omega
\]

The resistance of the thermistor at room temperature (\( R_{TH} \)) is determined as 10\,k\,Ω. The current through the thermistor is obtained as

\[
I_{RTH} = \frac{V_{BE}}{R_{TH}} = \frac{0.608V}{10k\,\Omega} = 61\,\mu A \quad (34)
\]

The base resistor is determined by

\[
R_{base} = \frac{V_{sense} - V_{BE}}{I_B} = \frac{0.65V - 0.608V}{21\,\mu A} = 513\,\Omega \quad (35)
\]

Variations in the junction temperature of \( Q \) will cause variations in the value of controlled output current (\( I_o \)). The base-emitter voltage decreases with increasing temperature at a rate of approximately 2mV/\(^\circ\)C. When the base-emitter voltage is changed to \( V_{BE}^T \) as the temperature changes to \( T \) \(^\circ\)C, the thermistor resistance at \( T \) \(^\circ\)C required to compensate this variation is given by

\[
R_{TH}^T = \frac{V_{BE}^T}{R_{base}} \frac{V_{sense} - V_{BE}^T}{I_B} = \frac{V_{BE}^T}{R_{base} \cdot \frac{V_{sense} - V_{BE}^T}{I_B}} \quad (36)
\]

With -2mV/\(^\circ\)C, \( V_{BE} \) reduces to 0.508V from 0.608V as temperature increases from 25\(^\circ\)C to 75\(^\circ\)C. From equation
(36), the resistance of the thermistor at 75°C to keep the same output current is given by

\[
\frac{0.508V}{0.65V - 0.508V} = 1.99k
\]

NTC thermistor 103X2 from DSC is chosen for the compensation, whose resistance is 10kΩ at 25°C and 1.92kΩ at 75°C.

(b) OP amp and shunt regulator (KA431) scheme

Figure 15 shows a 4.2 V, 0.8A CC/CV control circuit using the LM358 dual op amp shunt regulator (KA431). This circuit provides higher accuracy compared with the simple transistor circuit. Power loss is lower and efficiency is better because smaller resistance values can be used for sense resistor Rsense. The shunt regulator (KA431) is used as a voltage reference for an accurate control.

**Constant voltage (CV) control**: The Output voltage is sensed by R1 and R2 and then compared by OP amp LM358B to reference of 2.5V. The output of the OP amp drives current through D2 and R д into the LED of the optocoupler. The voltage divider network of R1 and R2 should be designed to provide 2.5V to the reference pin of the KA431. The relationship between R1 and R2 is given by

\[
\frac{2.5 \cdot R_1}{V_o - 2.5} = R_2
\]

where \(V_o\) is the output voltage.

By choosing \(R_1\) to be 680Ω, \(R_2\) is obtained as

\[
R_2 = \frac{2.5 \cdot 680}{4.2V - 2.5V} = 1kΩ
\]

C\(_{F2}\), R\(_{F2}\), and R\(_6\) compensate the voltage control loop.

**Constant Current (CC) control**: The voltage drop across the sensing resistor (R\(_{sense}\)) is given by

\[
V_{sense} = I_o \cdot R_{sense}
\]

It is typical to set \(V_{sense}\) as 0.1-0.2V.

Since the inverting input of OP amp is virtually grounded, the relationship between R4 and R5 is given by

\[
R_4 = \frac{V_{sense} \cdot R_5}{2.5}
\]

By choosing R5 as 33kΩ, R4 is obtained as 2.1kΩ. C\(_{F2}\), R\(_{F2}\), and R\(_6\) compensate the current control loop.
Figure 15. CC/CV control using OP amp and shunt regulator
- Summary of symbols -

\( A_w \) : Winding window area of the core in mm²

\( A_e \) : Cross sectional area of the core in mm²

\( B_{sat} \) : Saturation flux density in tesla.

\( C_o \) : Output capacitor

\( D_{max} \) : Maximum duty cycle ratio

\( E_{ff} \) : Estimated efficiency

\( f_L \) : Line frequency

\( f_s \) : Switching frequency of FPS

\( I_{ds}^{\text{peak}} \) : Maximum value of peak current through MOSFET at the minimum input voltage condition

\( I_{ds2}^{\text{peak}} \) : Maximum value of peak current through MOSFET at the maximum input voltage condition

\( I_{ds}^{\text{rms}} \) : RMS current of MOSFET

\( I_{ds2} \) : Maximum peak drain current at the maximum input voltage condition.

\( I_{\text{over}} \) : FPS current limit level.

\( I_{se}^{\text{rms}} \) : RMS current of the secondary winding

\( I_{D}^{\text{rms}} \) : Maximum rms current of the output rectifier diode

\( I_{\text{cap}}^{\text{rms}} \) : RMS Ripple current of the output capacitor

\( I_o \) : Output load current

\( K_{RF} \) : Current ripple factor

\( L_m \) : Transformer primary side inductance

\( L_{lk} \) : Transformer primary side leakage inductance

\( L_{\text{loss,sn}} \) : Maximum power loss of the snubber network in normal operation

\( N_p^{\text{min}} \) : The minimum number of turns for the transformer primary side to avoid saturation

\( N_p \) : Number of turns for primary side winding

\( N_s \) : Number of turns for the output winding

\( N_a \) : Number of turns for the Vcc winding

\( P_o \) : Maximum output power

\( P_{in} \) : Maximum input power

\( R_c \) : Effective series resistance (ESR) of the output capacitor.

\( R_{sn} \) : Snubber resistor

\( R_L \) : Effective total output load resistor of the controlled output

\( V_{\text{line}}^{\text{min}} \) : Minimum line voltage

\( V_{\text{line}}^{\text{max}} \) : Maximum line voltage

\( V_{DC}^{\text{min}} \) : Minimum DC link voltage

\( V_{DC}^{\text{max}} \) : Maximum DC line voltage

\( V_{ds}^{\text{nom}} \) : Maximum nominal MOSFET voltage

\( V_o \) : Output voltage

\( V_F \) : Forward voltage drop of the output rectifier diode.

\( V_{cc}^{+} \) : Nominal voltage for Vcc

\( V_{Fa} \) : Diode forward voltage drop of Vcc winding

\( V_D \) : Maximum voltage of the output rectifier diode

\( V_{RO} \) : Output voltage reflected to the primary

\( V_{sn} \) : Snubber capacitor voltage under minimum input voltage and full load condition

\( V_{sn2} \) : Snubber capacitor voltage under maximum input voltage and full load condition

\( V_{ds}^{\text{max}} \) : Maximum voltage stress of the MOSFET
**Design example using FPS Design Assistant**

<table>
<thead>
<tr>
<th>Application</th>
<th>Device</th>
<th>Output Power</th>
<th>Input voltage</th>
<th>Output voltage (Max Current)</th>
<th>Ripple spec</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery charger</td>
<td>FSD210</td>
<td>3.4W</td>
<td>85V-265VAC</td>
<td>5.2V (0.65A)</td>
<td>± 5%</td>
</tr>
</tbody>
</table>

1. **Define the system specifications**

- Minimum Line voltage ($V_{\text{line min}}$) = 85 V.rms
- Maximum Line voltage ($V_{\text{line max}}$) = 265 V.rms
- Line frequency ($f_l$) = 60 Hz

<table>
<thead>
<tr>
<th>Output</th>
<th>$V_{\text{in}}$</th>
<th>$I_{\text{in}}$</th>
<th>$P_{\text{in}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5.2 V</td>
<td>0.65 A</td>
<td>3.4 W</td>
</tr>
</tbody>
</table>

Maximum output power ($P_o$) = 3.4 W
Estimated efficiency ($E_f$) = 65 %
Maximum input power ($P_{in}$) = 5.2 W

☞ The estimated efficiency ($E_f$) is set to be 0.65, considering the low output voltage and the loss in the current sensing resistor.

2. **Determine DC link capacitor and DC link voltage range**

- DC link capacitor ($C_{DC}$) = 9.4 uF
- Minimum DC link voltage ($V_{DC,\text{min}}$) = 84 V
- Maximum DC link voltage ($V_{DC,\text{max}}$) = 375 V

☞ Since the input power is 5.2 W, the DC link capacitor is set to be 9.4uF by 2uF/Watt. (4.7uF × 2)

3. **Determine Maximum duty ratio ($D_{\text{max}}$)**

- Output voltage reflected to primary ($V_{\text{RO}}$) = 70 V
- Maximum duty ratio ($D_{\text{max}}$) = 0.456
- Max nominal MOSFET voltage ($V_{ds,\text{nom}}$) = 445 V

☞ $V_{\text{RO}}$ is set to be 70V so that $V_{ds,\text{nom}}$ would be about 70% of 650V.

4. **Determine transformer primary inductance ($L_m$)**

- Switching frequency of FPS ($f_s$) = 134 kHz
- Ripple factor ($K_{RF}$) = 0.66
- Primary side inductance ($L_m$) = 1597 uH
- Maximum peak drain current ($I_{ds,\text{peak}}$) = 0.23 A
- RMS drain current ($I_{ds,\text{rms}}$) = 0.10 A
- Maximum DC link voltage in CCM ($V_{DC,\text{CM}}$) = 143 V

$$K_{RF} = \frac{\Delta I}{I_{\text{DC}}}, \quad \Delta I = \frac{2I_{\text{DC}}}{K_{RF}}$$
5. Choose the proper FPS considering the input power and current limit

<table>
<thead>
<tr>
<th>Typical current limit of FPS (I_{over})</th>
<th>0.32 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum I_{over} considering tolerance of 12%</td>
<td>0.28 A</td>
</tr>
</tbody>
</table>

$\Rightarrow$ O.K.

6. Determine the proper core and the minimum primary turns

<table>
<thead>
<tr>
<th>Saturation flux density ($B_{sat}$)</th>
<th>0.30 T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cross sectional area of core ($A_e$)</td>
<td>19.4 mm²</td>
</tr>
<tr>
<td>Minimum primary turns ($N_p^{\text{min}}$)</td>
<td>87.8 T</td>
</tr>
</tbody>
</table>

☞ Ferrite core EE1616 is chosen ($A_e=19.4$ mm²)

7. Determine the number of turns for each output

<table>
<thead>
<tr>
<th>Vcc (Use Vcc start voltage)</th>
<th>V_{F(n)}</th>
<th># of turns</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st output for feedback</td>
<td>12 V</td>
<td>0.6 V</td>
</tr>
<tr>
<td></td>
<td>5.2 V</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>

VF: Forward voltage drop of rectifier diode

Primary turns ($N_p$) = 99 T

$\Rightarrow$ enough turns

Ungapped AL value (AL)

Gap length (G): center pole gap = 1150 nH/T²

The voltage drop in the sensing resistor (0.7V) is included in the diode voltage drop of the output diode.

(0.7V + 0.5V = 1.2V)

8. Determine the wire diameter for each winding

<table>
<thead>
<tr>
<th>Diameter</th>
<th>Parallel</th>
<th>$I_{(n)\text{rms}}$</th>
<th>(A/mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary winding</td>
<td>0.16 mm</td>
<td>1 T</td>
<td>0.1 A</td>
</tr>
<tr>
<td>Vcc winding</td>
<td>0.16 mm</td>
<td>2 T</td>
<td>0.1 A</td>
</tr>
<tr>
<td>Output winding</td>
<td>0.4 mm</td>
<td>1 T</td>
<td>1.2 A</td>
</tr>
</tbody>
</table>

Copper area ($A_c$) = 3.84 mm²

Fill factor ($K_C$) = 0.15

Required window area ($A_{ww}$) = 25.62 mm²

☞ Since the winding for 5.2V is short with small number of turns, relatively large current density ($>5$A/mm²) is allowed.

9. Choose the rectifier diode in the secondary side

<table>
<thead>
<tr>
<th>Vcc diode</th>
<th>$V_{D(n)}$</th>
<th>$I_{(n)\text{rms}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc winding</td>
<td>80 V</td>
<td>0.10 A</td>
</tr>
<tr>
<td>1st output diode</td>
<td>39 V</td>
<td>1.18 A</td>
</tr>
</tbody>
</table>

Vcc winding: UF4003 (200V/1A, VF=1V) Ultra Fast Recovery Diode

Output (5.2V): SB260 (60V/2A, VF=0.55V) Schottky Barrier Diode
10. Determine the output capacitor

<table>
<thead>
<tr>
<th>1st output capacitor</th>
<th>$C_o(n)$</th>
<th>$R_o(n)$</th>
<th>$I_{cap(n)}$</th>
<th>$\Delta V_o(n)$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>330 uF</td>
<td>200 mΩ</td>
<td>1.0 A</td>
<td>0.50 V</td>
</tr>
</tbody>
</table>

Since the output voltage ripple exceeds the ripple spec of ±5%, additional LC filter stage should be used. 330uF capacitor together with 3.9uH inductor are used for the post filter.

11. Design RCD snubber

- Primary side leakage inductance ($L_{li}$): 50 uH
- Maximum Voltage of snubber capacitor ($V_{sn}$): 170 V
- Maximum snubber capacitor voltage ripple: 9%
- Snubber resistor ($R_{sn}$): 99.6 kΩ
- Snubber capacitor ($C_{sn}$): 0.8 nF
- Power loss in snubber resistor ($P_{sn}$): 0.3 W (In Normal Operation)
- Peak drain current at $V_{DC}^{max}$ ($I_{ds2}$): 0.22 A
- Max Voltage of Csn at $V_{DC}^{max}$ ($V_{sn2}$): 167 V
- Max Voltage stress of MOSFET ($V_{ds}^{max}$): 542 V

☞ The snubber capacitor and snubber resistor are chosen as 1nF and 94kΩ (47kΩ × 2), respectively. The maximum voltage stress on the MOSFET is below 80% of BVdss (700V).
Design Summary

Features
- High efficiency (>60% at Universal Input)
- Low power consumption (<100mW at 240Vac) with no load
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (3ms)
- Frequency Modulation for low EMI

Key Design Notes
- The constant voltage (CV) mode control is implemented with resistors, R8, R9, R10 and R12, shunt regulator, U2, feedback capacitor, C9 and opto-coupler, U3.
- Even though FSD210 has an internal soft start, C10 is employed to provide longer soft start time. Since C10 reduces the feedback gain, a relatively small resistor is used for R9 in order to compensate it.
- The constant current (CC) mode control is realized with resistors, R8, R9, R15, R16, R17 and R19, npn transistor, Q1 and NTC, TH1. When the voltage across current sensing resistors, R15, R16 and R17 is 0.7V, the npn transistor turns on and the current through the opto coupler LED increases. This reduces the feedback voltage and duty ratio. Therefore, the output voltage decreases and the output current is kept constant.
- The NTC (negative thermal coefficient) is used to compensate the temperature characteristics of the transistor Q1.

Figure 16. The final schematic of the flyback converter
Experimental Verification

In order to show the validity of the design procedure presented in this paper, the converter of the design example has been built and tested. All the circuit components are used as designed in the design example and the detailed transformer structure is shown in Figure 17. The winding specifications and measured transformer characteristics are shown in table 4 and 5, respectively. The dummy winding (W3) is used as an EMI shield. This winding improves EMI characteristics by screening the radiation noise generated from the primary winding.

Figure 17. Transformer structure

Table 4. Winding specifications

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin (S → F)</th>
<th>Wire</th>
<th>Turns</th>
<th>Winding Method</th>
<th>Winding Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>1 → 2</td>
<td>0.160 X 1</td>
<td>99 Ts</td>
<td>SOLENOID WINDING</td>
<td>SOLENOID WINDING</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PRIMARY SIDE INDUCTANCE</td>
<td>PRIMARY SIDE INDUCTANCE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LEAKAGE INDUCTANCE</td>
<td>LEAKAGE INDUCTANCE</td>
</tr>
<tr>
<td>W2</td>
<td>4 → 3</td>
<td>0.160 X 1</td>
<td>18 Ts</td>
<td>CENTER SOLENOID WINDING</td>
<td>CENTER SOLENOID WINDING</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PRIMARY SIDE INDUCTANCE</td>
<td>PRIMARY SIDE INDUCTANCE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LEAKAGE INDUCTANCE</td>
<td>LEAKAGE INDUCTANCE</td>
</tr>
<tr>
<td>W3</td>
<td>OPEN</td>
<td>0.160 X 1</td>
<td>50 Ts</td>
<td>SOLENOID WINDING</td>
<td>SOLENOID WINDING</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PRIMARY SIDE INDUCTANCE</td>
<td>PRIMARY SIDE INDUCTANCE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LEAKAGE INDUCTANCE</td>
<td>LEAKAGE INDUCTANCE</td>
</tr>
<tr>
<td>W4</td>
<td>8 → 7</td>
<td>0.160 X 1</td>
<td>9 Ts</td>
<td>SOLENOID WINDING</td>
<td>SOLENOID WINDING</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PRIMARY SIDE INDUCTANCE</td>
<td>PRIMARY SIDE INDUCTANCE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LEAKAGE INDUCTANCE</td>
<td>LEAKAGE INDUCTANCE</td>
</tr>
</tbody>
</table>

Table 5. The measured transformer characteristics

<table>
<thead>
<tr>
<th>Core</th>
<th>EE1616 (ISU Ceramics)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary side inductance</td>
<td>1.6 mH @ 100kHz</td>
</tr>
<tr>
<td>Leakage inductance</td>
<td>50 uH @ 100kHz with all other windings shorted.</td>
</tr>
</tbody>
</table>

Figure 18 shows the FPS drain current and voltage waveforms at the minimum input voltage and full load condition. As designed, the maximum peak drain current ($I_{ds, peak}$) is about 0.23A. Figure 19 shows the FPS drain current and voltage waveforms at the maximum input voltage and full load condition. The maximum voltage stress on the MOSFET is about 520V, which is lower than the designed value (542V). This is because of the lossy discharge of the inductor or the stray capacitance. The measured efficiencies at full load for different input voltages are shown in Figure 20. The minimum efficiency is 61% at 265V input voltage. The efficiencies are a little bit low due to the power loss in the current sensing resistor in the output.

The components for CC/CV control circuit are chosen as designed in design procedure of step-12. Figure 21 and 22 show the output voltage vs. output current characteristics at 25°C and 75°C, respectively. As designed, the output voltage is 5.2V and the output current is 0.65A. The output current variation with temperature is very small due to the temperature compensation circuit with thermistor.

Table 6 shows the power consumption in the standby mode. Through the burst mode operation, the power consumption is minimized. The power consumption at 240V input is under 100 mW. The detailed burst operation waveforms are shown in Figure 23 and 24. By disabling and enabling the switching operation according to the feedback voltage, the effective switching frequency is reduced, which also reduces the power consumption in the standby mode.
Figure 19. Waveforms of drain current and voltage at 265Vac and full load condition

Figure 20. Measured efficiency at full load for different input voltage

Figure 21. Output voltage (Vo) vs. output current (Io) Characteristics @ 25 °C

Figure 22. Output voltage (Vo) vs. output current (Io) Characteristics @ 75 °C

Table 6. Standby power consumption

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>Input power</th>
</tr>
</thead>
<tbody>
<tr>
<td>85Vac</td>
<td>54 mW</td>
</tr>
<tr>
<td>240Vac</td>
<td>92 mW</td>
</tr>
<tr>
<td>265Vac</td>
<td>110 mW</td>
</tr>
</tbody>
</table>

Figure 23. Burst mode Waveforms at 85Vac and full load condition
Figure 24. Burst mode Waveforms at 265Vac and full load condition
by Hang-Seok Choi / Ph. D
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E-mail: hschoi@fairchildsemi.co.kr

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