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Fairchild Semiconductor
Application Note
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Using BGA Packages

Introduction

Demanding space and weight requirements of personal computing and portable electronic equipment has led to many innovations in IC packaging. Combining the right interface and logic products with new package technology can have a significant impact on the capabilities and form-factor of the end product. Leaded surface mount devices are constantly pushing the manufacturing capabilities of leading board manufacturers to finer and finer lead pitch geometry's to increase I/O density and reduce board space.

This requirement has lead to significant interest in the JEDEC (Joint Electron Device Engineering Council) registered Fine-Pitch Ball Grid Array (FBGA) package. These packages are ideally suited to low cost, high volume applications, where package size and performance is of major importance. Typical BGA applications include:

1. Notebook computers
2. Personal Digital Assistants (PDA's)
3. Mobile telephone handsets
4. High density disk drives
5. Camcorders
6. Digital cameras

BGA advantages compared to fine pitch QFP or TSSOP packages:

1. BGAs are usually smaller.
2. BGAs have larger pitch.
3. BGAs have no fragile leads, that causes yield and rework problems.
4. Board assembly yields are significantly improved.
5. Board inspection can be reduced.
6. BGAs have better thermal and electrical properties.
7. In many applications, the use of BGA results in significant system level cost savings.

Surface Mount vs. BGA

At 0.4 to 0.5mm pin pitch, the race to finer surface mount lead pitches has hit several technical and economic walls. Manufacturing anything smaller will significantly impact PCB yield and push board costs above acceptable levels for the highly competitive and cost conscious electronics industry. Avoiding problems such as bent leads and solder bridging become significant manufacturing challenges. Additionally, electrical problems such as crosstalk become a major issue due to the length and close pitch of the leads on surface mount packages.

Alternatively, BGA packaging uses relatively wide "pad to pad" pitch rules and when coupled with existing PCB manufacturing processes result in high yields. The "array" approach improves I/O density and reduces the board space consumed by the device. Table 1 and Figure 1 show examples of space savings of BGA over surface mount packages.

TABLE 1. BGA Space Savings Compared to Surface Mount Packages

Number of Bits	TSSOP	TVSOP	QVSOP BQSOP
36 to 48	> 66%	> 47%	> 59%
32 to 40	> 67%	61%	49%
18 to 24	65.50%	40%	NA
16 to 20	61%	39%	37%

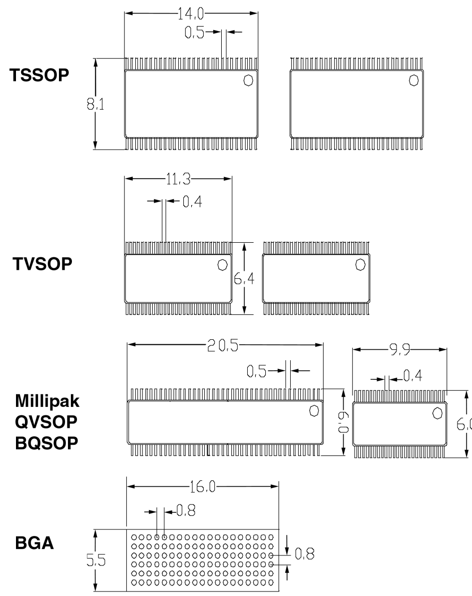

FIGURE 1. 114 Ball BGA vs. Surface Mount

BGA Routing

Fairchild Semiconductor BGA products are all designed around the JEDEC standard 0.8mm ball pitch and large 0.5mm ball size. This allows for economical 0.15mm (6 mil) line and space PCB manufacturing processes as well as optimized reliability. Figure 2 shows two 0.15mm (6 mil) line routing techniques.

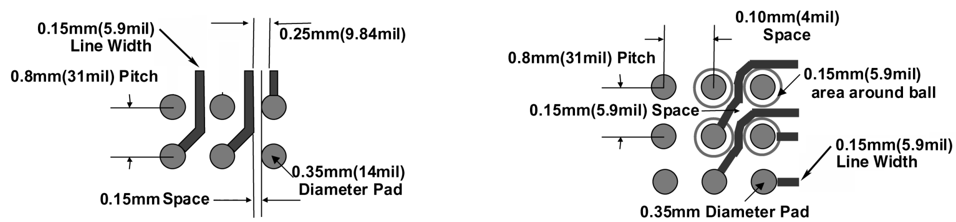

FIGURE 2. BGA Routing

Figure 3 through Figure 7 illustrate the basic routing techniques of the different bit-count devices.

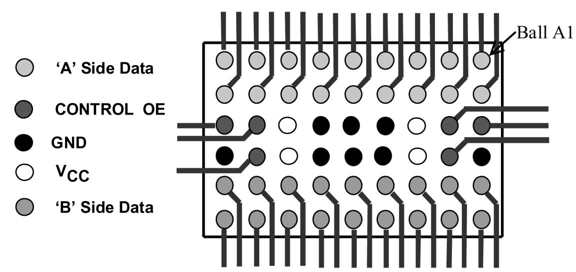

FIGURE 3. 54-Ball 18-Bit BGA Routing (74LCX16500)

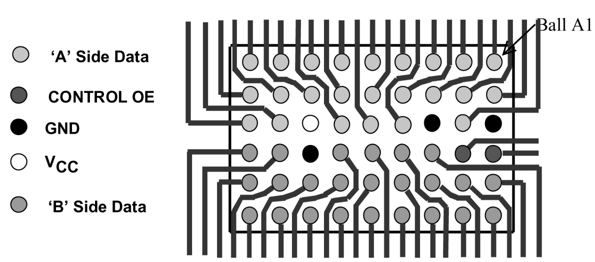

FIGURE 4. 54-Ball 24-Bit BGA Routing (FST16211)

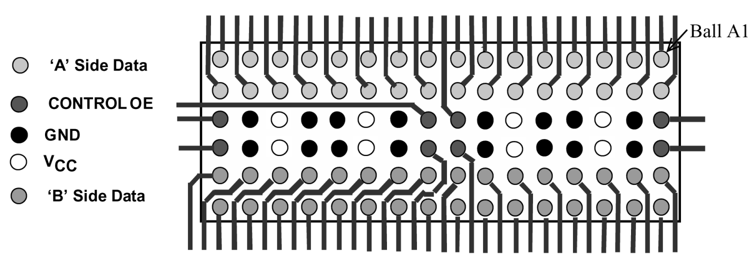

FIGURE 5. 96-Ball 32-Bit BGA Routing (74VCX32374)
Note: Various techniques for routing internal control pins.

BGA Routing (Continued)

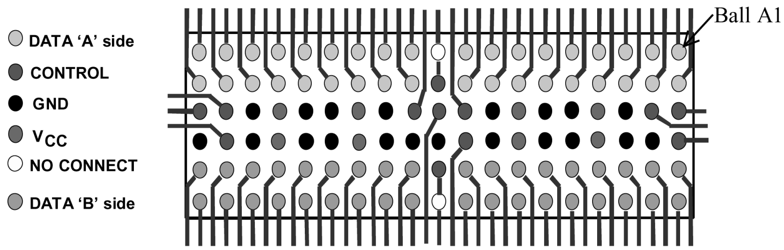

FIGURE 6. 114-Ball 36-Bit BGA Routing (74VCX32500)

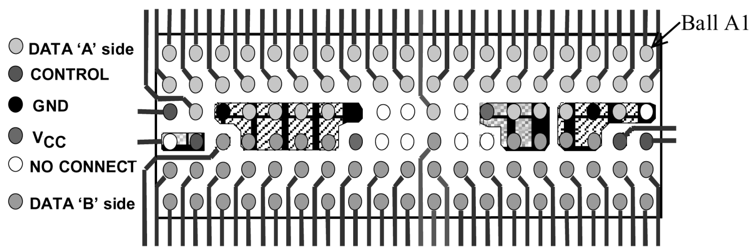

FIGURE 7. 114-Ball 40-Bit BGA Routing (FST32211)
Note: The FST32211 can also be routed as a 43-bit switch without the use of vias.

Routing Power and Ground:

Power and ground balls have not been routed in the illustrations above because of the designers multiple routing choices. There are generally two methods:

1. Supplying power and ground to the BGA by connecting vias to the V_{CC}/GND planes and traces under the BGA package. See Figure 8 for via placement.

   Pros: Better noise performance due to lower power inductance (shorter V_{CC}/GND trace length).

   Cons: Via size under the package is restricted to 0.56mm (22.0 mil) vias.

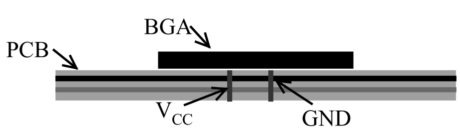

FIGURE 8. BGA Powered with Vias Under the Package

2. Supplying power and ground to the BGA by connecting vias to the V_{CC}/GND plains and traces outside the BGA package. See Figure 9.

   Pros: Allows for larger vias outside the package.

   Cons: Compromised noise performance through trace length added V_{CC}/GND trace length.

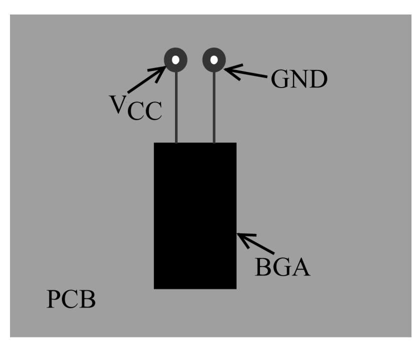

FIGURE 9. BGA Powered with Vias Outside the Package Land Area

BGA Via Design and Layout Options

When using vias in high bit-count devices such as the 48-bit FST32211 (see Figure 10), via density and placement become critical issues for the layout designer. The use of through-board vias allows access to all signal bits on the device; this helps contribute to maximum space integration. Additionally, the board backside vias can be used to connect components such as termination and decoupling devices if needed.

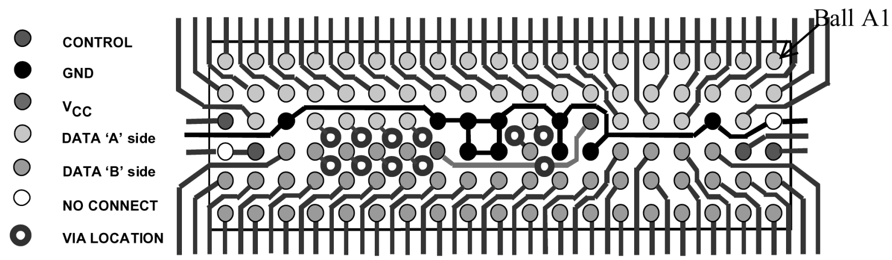

FIGURE 10. 114-Ball 48-Bit BGA with Vias (FST32211)
Note: For a via free 48-bit bus switch solution two FST16211 can be used with a minimal loss in space savings. (see Figure 4)

Figure 11 shows ball pads to via spacing with a BGA 0.8mm pitch and a 0.56mm via, which give a 0.11mm via to ball spacing. Figure 12 shows a board cross-section with non-solder mask defined pads-to-via spacing dimensions. Manufacturing technology and expense are the deciding factors in via size. Larger vias allow for more relaxed manufacturing rules and lower costs. Smaller vias are more costly due to the high end manufacturing equipment and higher drill bit breakage.

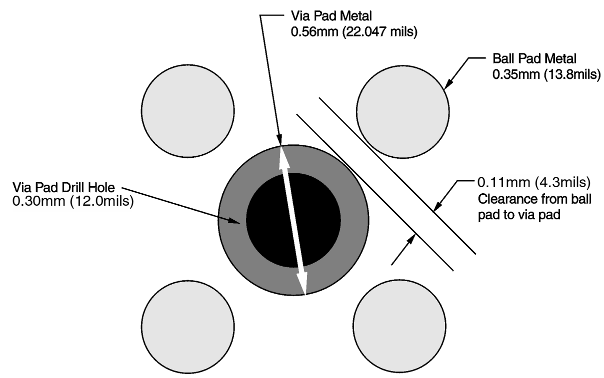

FIGURE 11. BGA Via to Ball Spacing Diagram

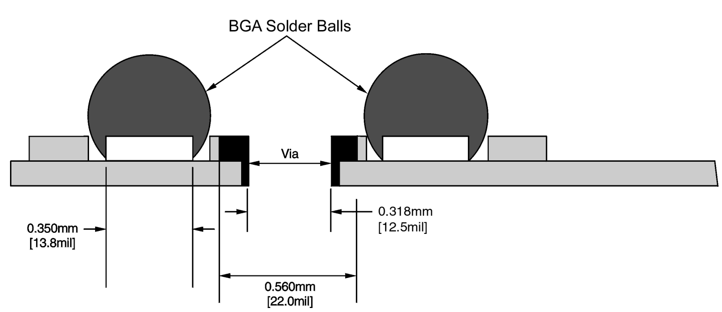

FIGURE 12. Board with Non-Solder Mask Defined Pads to Via Spacing

BGA Via Design and Layout Options (Continued)

Through-board vias are the most economical via type from a board manufacturing perspective. However, trade-offs in highly space-constrained designs may be required. Through-board vias create a matrix of vias on the board backside, limiting its use for traces and components. These vias can also disrupt the smooth layout of bus runs on internal board layers or limit their placement.

With the ever increasing demand for more compact systems and higher density layouts, three more advanced methods of via connections are being used, the blind via, the buried via, and the micro via. Figure 13 shows an example of these via types used in conjunction with a BGA.

Blind vias connect one side of the board to some inner layers, but do not run completely through to the other side. Buried vias connect internal board layers but do not extend to the exterior of the board.

Micro vias are very small vias (4µm is typical) and can be used for via in pad layouts. This can significantly reduce via density, increase routing options on the board, and conserve space. Laser technology is often used to drill micro vias. Lasers drill micro vias through a 4 millimeter thick dielectric layer, allowing connection to the first internal layer of the board. Two 4 millimeter layers can be drilled with a laser, allowing connection from the surface to the second board layer.

These three via types are more costly than through-board vias from a manufacturing standpoint. However, there are two significant advantages over through-board vias; the elimination of backside vias frees that layer for component placement, and some internal layers and the backside are freed up for traces and uninterrupted bus runs.

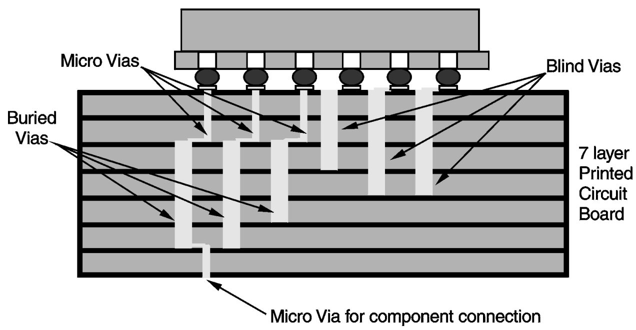

FIGURE 13. Multi Layer Board with BGA Connections to Micro Vias, Buried Vias and Blind Vias

BGA Board Design

To achieve maximum reliability, the design of the PCB on which the BGA is mounted should be considered. In particular, the diameter of package lands and board lands are very important. The actual sizes of these dimensions are key factors, but their ratio is also of critical importance. Figure 14 shows a BGA Board Layout with the optimum 1 to 1 ratio for package land to PCB land. This optimized ratio equalizes stresses, reducing the chances of a stress cracked solder ball, which will lead to premature system failure. Ratios other than 1 to 1 will lead to unequal distribution of stress loads. For example, solder lands that are larger than the package lands will place a greater amount of stress on the ball at the package land to ball interface. This can cause cracking and premature failure at the package land to ball interface.

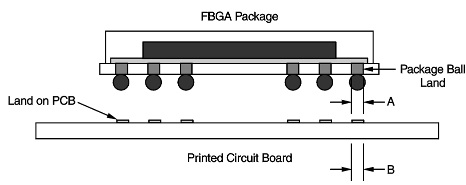

FIGURE 14. BGA Board Layout

A = Land diameter on package

B = Land diameter on printed circuit board

Ratio A/B = 1 for best case reliability

In practice optimum land diameters are as follows:

Solder Mask defined pads: 0.375mm

Non-Solder Mask defined pads: 0.350mm

Experience has shown that solder lands can be either solder mask defined, or non-solder mask defined. However, non-solder mask defined designs provide additional ball-to-land contact area, making them the favored option. The additional contact area is created from the solder ball to pad side connection made during the soldering process. As shown in Figure 15 this creates an improved mechanical connection.

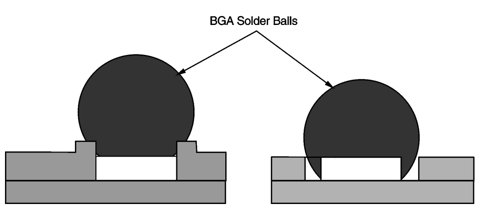

FIGURE 15. Cross-section Comparison of Solder Mask Defined Pad (left) to Non-Solder Mask Defined Pad (right) with BGA Solder Ball Connections

BGA Mounting Process

Replacing leaded packages with BGA's offers several board assembly advantages:

1. Improved device planarity
2. No chance to bend leads
3. Greater pad to pad spacing

With no chance to bend or deform leads, BGA products offer PCB manufacturers a significant yield improvement over similar lead count fine-pitch surface mount devices. Another important feature of BGA products is their ability to self-align over the PCB solder lands.

This feature is caused by the surface tension of the solder balls pulling the BGA over the pads.

The use of solder paste is recommended for mounting BGA devices, although it is possible to omit the paste, and only use a flux. The advantages of using paste are:

1. Paste acts as a flux, and aids wetting of the solder ball to the PCB land.
2. Paste, being sticky, helps hold the component in place during reflow.
3. Paste helps to overcome any minor variations in planarity of the solder balls.
4. Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

No-clean type pastes are recommended, due to difficulty in cleaning under the mounted component.

In order to produce the optimum solder joint, it is important to understand the amount of collapse of the solder balls, and the overall shape of the joint. These are a function of:

1. The diameter of the BGA solder ball vias.
2. The volume and type of solder paste screened onto the PCB.
3. The diameter of the PCB land.
4. The board assembly re-flow conditions.
5. The weight of the package.

As shown in Figure 16, the original ball height on the package is 0.40mm. The ball height typically drops to 0.35mm after the package is mounted.

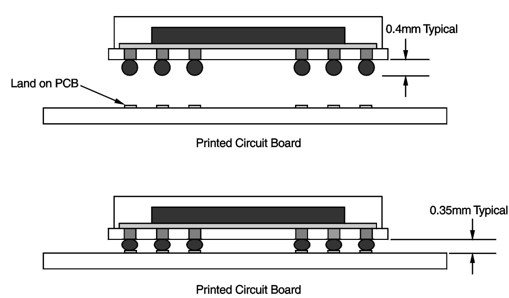

FIGURE 16. BGA Solder Ball Collapse

BGA Testing

During the prototype and engineering debug phase it may be necessary to access IC signals for testing purposes.

Several options exist depending on the specific needs of the system being developed.

1. Prototype socket for the BGA
2. Via fanout
3. PCB solder mask defined lands

Each of the methods offers advantages and disadvantages. The prototype socket gives the designer the ability to test multiple devices in the socketed connection. The via fan-out method, as shown in Figure 17, incorporates a mounted BGA routed through an array of vias for signal accessibility.

With form factor boards large via arrays remove all the board real estate advantage gained with the BGA packaging. Limited I/O access can still be gained using test points like those shown in Figure 18.

Minimum Size Via Defined Pattern for Prototype Testing

- 19 x 6 ARRAY 0.8mm pitch with package dimensions of 16.0mm x 5.5mm
- Overall dimensions (including TestVia's) 20.1mm x 8.8mm
- 22mil vias, 15mil holes; 6mil line and space PCB rules

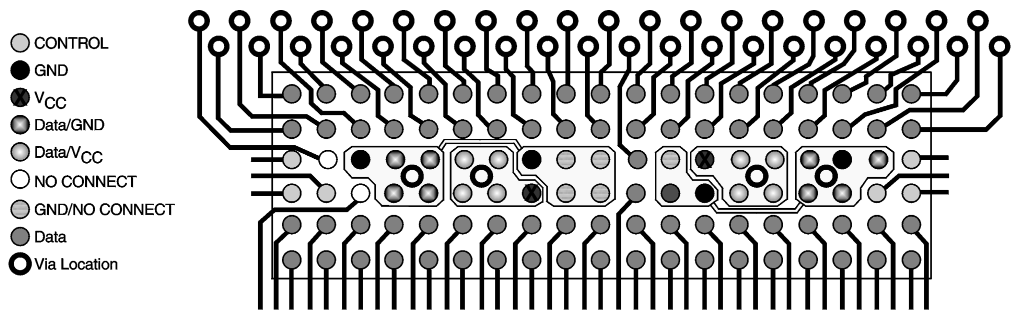

FIGURE 17. Via Fan-out for Prototype Testing

Solder Mask Defined Land Pattern for In-System Testing

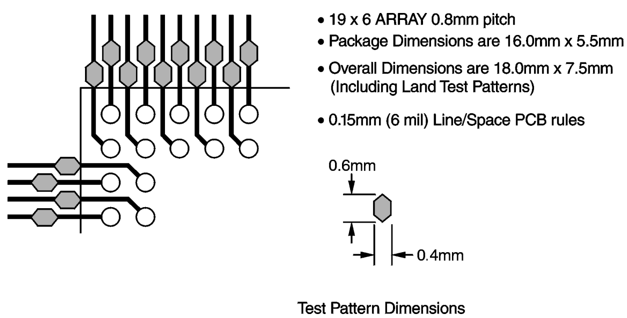

FIGURE 18. BGA In-System Testing

Notebook Docking Application

Routing the BGA into the hole pattern created by a typical 0.8mm docking connector can be achieved on a single PCB signal layer. By limiting the signal routing to a single layer, few if any vias are needed for the BGA. Eliminating all datapath vias allows for greater levels of backside usability and backside component placement.

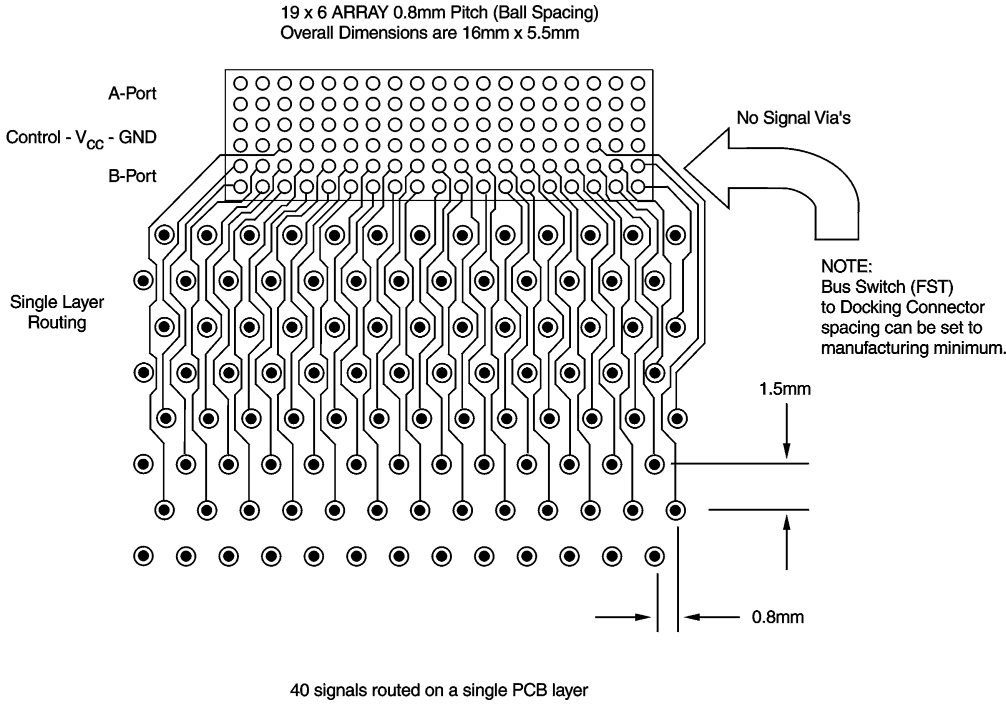

FIGURE 19. BGA Docking Application

Conclusion

FBGA's offer dramatic new levels of PCB layout and design possibilities. BGA's offer space savings of 60% or more vs. TSSOP and greater than 37% over comparable TVSOP and QVSOP packaging. By understanding how to effectively use these new packages, PCB and system designers can create electronic systems with greater component density, miniaturization and functionality. An additional benefit is system manufacturing with less re-work and more reliability. Continued innovations and cost reductions in PCB manufacturing technology will usher in advances in PCB design and further the usability and cost effectiveness of BGA's. With BGA packages already on par with leaded packages in cost per bit for large-scale designs, and the continued drive toward system size reduction, FBGA's of all types are the wave of the future and will soon be everywhere.