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Fairchild Semiconductor
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System Clock Distribution Example Using LVDS

Abstract

Noise within high-speed digital systems especially when dealing with critical signals such as the ones the in clock distribution circuits can be a concern for designers. Running single-ended clocks lines over long traces across a printed circuit board can introduce unwanted noise such as crosstalk that ultimately affects the performance and reliability of a digital system. This paper will discuss the benefits of using Low Voltage Differential Signaling (LVDS) for clock distribution and how this signaling technique addresses this problem. An application example will also be provided.

Why Use Differential Signaling?

System designers should consider using differential signaling circuits if there is a concern of introducing noise from clock line(s) across the circuit board and the requirement for critical clock line with a high level of noise immunity from the other adjacent PCB traces.

Differential signaling addresses both of these design concerns as the signaling technique uses traces between a driver and receiver with one trace carrying a positive signal and the other carrying the negative signal equal and opposite in polarity. With this technique the return current through the ground system cancels assuming they are exact opposites of each other. The return current from the positive signal is (+i) which is equal to the return current of the negative signal (–i) and their SUM is zero.

Benefits of Using LVDS

A differential receiver is designed to respond to the difference between a pair of inputs and have a common mode rejection capability. That means any noise such as EMI or crosstalk that is common to both traces will be rejected by the receiver. To illustrate this feature reference Figure 1 which is a scope capture of Fairchild's FIN1018 single bit Low Voltage Differential Signaling (LVDS) receiver. The differential signals driving 6-inch microstrip lines with ~400mV of noise injected equally on both the R– and R+ inputs of the FIN1018 receiver. Note the TTL output of the receiver remains in it's current low state simply ignoring the noise excursions on its inputs and toggles only after the differential signals cross over. This common-mode noise rejection also applies to sources such as power supply variations, substrate noise, and ground bounce.

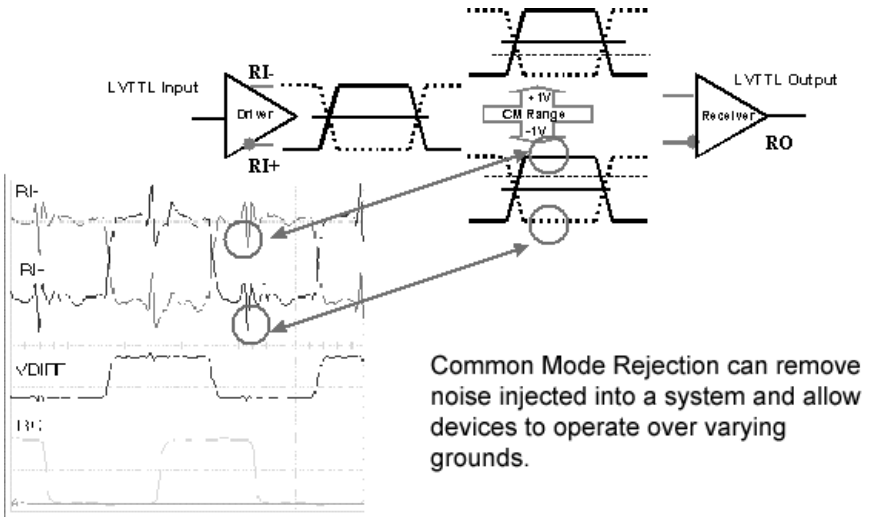

FIGURE 1. LVDS Common Noise Rejection Feature

Clock Distribution Application Example

In this particular application, differential lines on CLKA1 are used simply because the designer does not want to introduce the noise of a 133 MHz clock signal across the board. In addition, because of the critical nature of the clock line, the designer also does not want noise to be injected into the CLKA1 clock line.

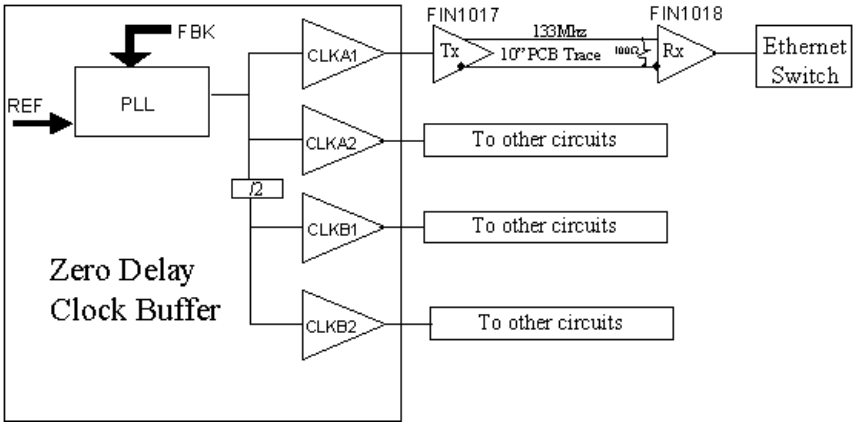

FIGURE 2. Block Diagram of a Clock Distribution Circuit using LVDS

Simulation Results

The question of whether or not the differential link between the clock buffer and the Ethernet switch will work in this particular application is answered below. Simulation of the point-to-point link with a 10" PCB trace a 133 MHz frequency was conducted and the results were as shown in Figure 3.

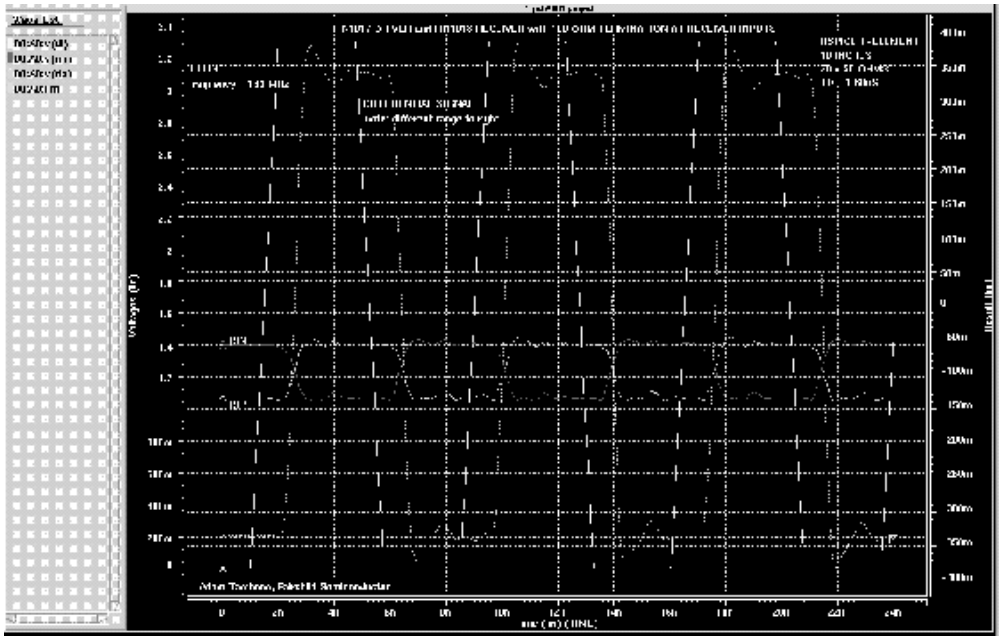

FIGURE 3. Simulation Results of FIN107 Transmitter and FIN1018 Receiver

Yellow Signal = TTL Input @ 133MHz with a 1ns edge

Red Signal = R_{in} - Single Ended Signal (~1.05V)

Peach Signal = R_{in} + Single Ended Signal (~1.4V)

Blue Signal = Differential Signal (~680mV)

Summary and Conclusions

LVDS differential lines have equal but opposite currents. When the fields created by these odd-mode signals are closely coupled, they will cancel each other and reduce interference with adjacent PCB traces. Because of this it is important to maintain a balanced and closely coupled differential transmission path to reduce EMI emissions. LVDS signals also have the advantage of tolerating interference from outside sources such as inductive radiation from electric motors or crosstalk from neighboring transmission lines. System designers who need to move high speed clock signals across cable or PCB with minimal EMI and a high level of noise immunity can benefit from LVDS technology.