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ECL Backplane Design

INTRODUCTION

Designers are constantly trying to improve the performance of their systems. In many applications, this can be accomplished by increasing the speed of the system backplane. As system bandwidth requirements exceed 50 MHz, ECL is the logic of choice over TTL. ECL devices are designed for transmission line applications which means that ringing, reflections, and noise are minimized. These problems are not easily handled with TTL devices. ECL devices are the fastest in common use today and have increased steadily in popularity over the past 10 years with the additional speed requirements of many systems. With this popularity have come improvements such as increased reliability, power reduction, and better ESD protection.

ECL devices today offer the flexibility of single-ended or differential backplanes. Fairchild Semiconductor has responded to the increasing need for ECL backplanes by introducing octal registers, latches and translators. The registers and latches offer the flexibility to drive a 25Ω (with cutoff) or 50Ω load impedance. The 25Ω drivers are intended to drive a 50Ω transmission line which is doubly terminated in its characteristic impedance, or a single low impedance 25Ω line. Considerations such as transmission line media (microstrip, stripline, coaxial, twisted pair, etc.) terminations, connectors, power planes and loading effects must all be understood to design the optimum system.

ECL/TTL PERFORMANCE PARAMETERS

There are several advantages associated with using ECL. ECL is a non-saturating logic, as opposed to TTL, which results in much faster switching speeds for drivers tied to the backplane. The ECL circuit contains a differential amplifier with its outputs being a function of the difference between two input voltages; where one is a reference voltage (V_{BB}) and the other (V_{IN}) is a logic HIGH or LOW (see Figure 1). The differential inputs determine which path the constant current (I_S) will flow. An internal reference circuit establishes a stable V_{BB} voltage of −1.32V. When a LOW level (−1.730V typical) signal is applied to V_{IN}, Q1 "cuts off". Transistor Q2 is turned on with collector current through the Q2 branch being supplied by the current source (I_S). This sets up a LOW level on **A** and a HIGH level on the compliment output as long as the output is properly terminated.

A HIGH level (−0.970V typical) applied to V_{IN} will then turn on Q1 and "cutoff" Q2. This will set up a HIGH voltage level on **A** and a LOW level on its compliment. Since the current is nearly constant at all times, even during switching, current spikes are minimized on the power supply. This is an important feature of ECL (unlike TTL) because the power requirement is unaffected by frequency. ECL becomes more favorable at frequencies above 50 MHz with a 50% duty cycle. The outputs of ECL devices typically require an external termination resistor and termination voltage (V_{TT}) to develop the proper output voltage levels.

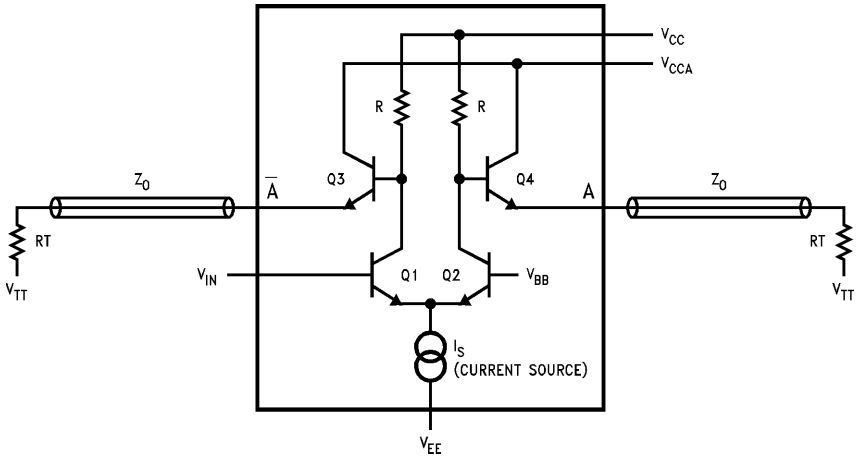


FIGURE 1. ECL Gate

ECL/TTL PERFORMANCE PARAMETERS (Continued)

ECL outputs are perfectly suited to drive transmission lines. With an output impedance of 6Ω to 8Ω and rise times less than 1 ns, reflections are minimized resulting in a clean signal.

A comparison of the approximate input and output capacitance values for non-I/O IC's shows that TTL devices generally run higher than ECL devices. These parameters are important because they in part determine the amount of loading that will be present on the backplane. With reduced loading on the backplane comes increased speed.

	ECL (PCC)	TTL (PDIP)
Input Capacitance	3.0 pF	5.0 pF
Output Capacitance	3.0 pF	5.0 pF

ECL also has the ability to drive low impedance transmission lines (i.e., 25Ω). As the transmission line impedance decreases, the speed of the transmitted signal increases. The lower impedance also reduces the effects of noise. The Fairchild Semiconductor F100K 300 Series octal devices were specifically designed for this type of application.

ECL TERMINATION SCHEMES

Parallel Termination

Termination of ECL outputs can be accomplished in several different ways. The most common way is to terminate the emitter follower output in the transmission line characteristic impedance (Z_O) to a V_{TT} voltage of −2.0V as shown in Figure 1. This method is used with $Z_O = 50\Omega$ to set specifications for most of the F100K 300 Series devices.

Thevenin Termination

The Thevenin equivalent termination method (shown in Figure 2) requires one resistor be connected between the end of the line to be terminated and the V_{CC} rail, with another placed between the end of the line and the V_{EE} supply. This method eliminates the need for a −2.0V V_{TT} supply, but the penalty is that the power dissipated will increase nearly eight times from the previous method. Several designers avoid this method for exactly that reason.

Series Termination

An alternate way to terminate the output is by a series termination scheme. With this arrangement, a resistor pair is placed directly at the output of the driver (shown in Figure 3). The series damping resistor (RS) should be chosen such that;

$Z_O = RS + R_{OUT}$

where:

Z_O = characteristic impedance of the transmission line
R_{OUT} = output resistance of the gate
RS = series damping resistor

The value of R_{OUT} for the F100K 300 Series devices is 6Ω when the output is conditioned to a HIGH level, and 8Ω when conditioned to a LOW level. An average value of 7Ω is used when calculating the value of RS. The RE resistor in this termination scheme is used to discharge the line when the driven output goes into a low condition. To ensure that the proper amount of current needed is available, RE is chosen by the formula:

$RE < Z_O [(V_{OH} - V_{EE})/0.49] - RS - Z_O$

The table (shown in Figure 3) gives the resistor values of RS and RE max for $V_{EE} = -4.5V$) needed for several different characteristic impedance transmission lines.

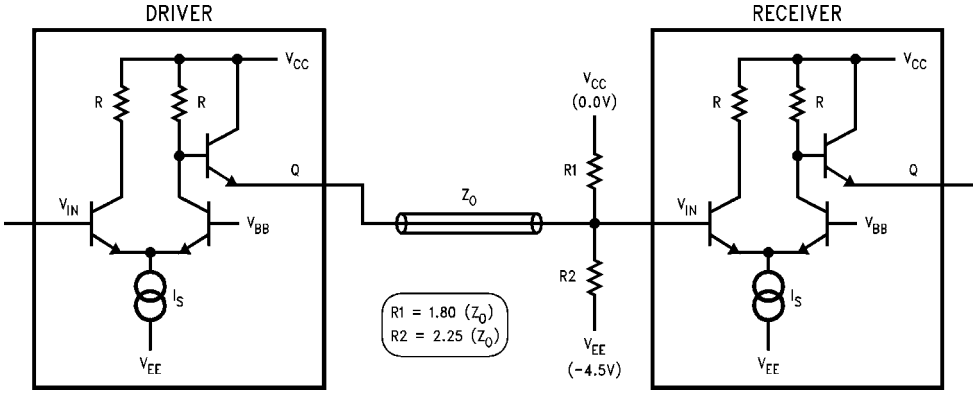
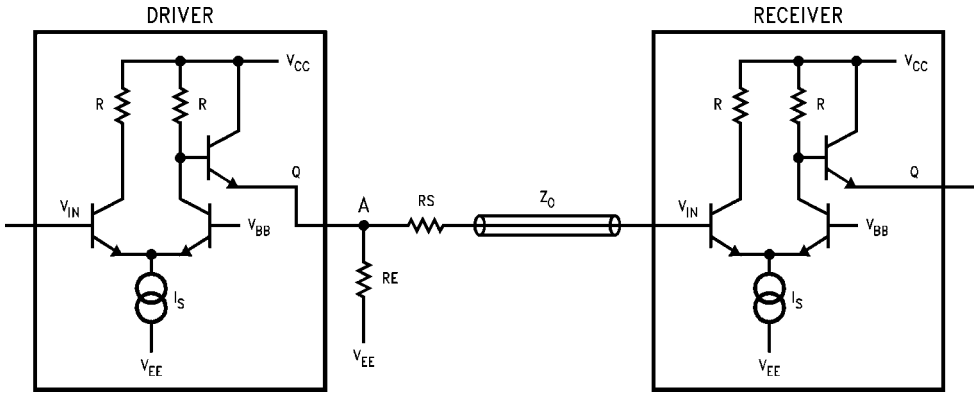


FIGURE 2. Thevenin Termination

Series Termination (Continued)



Z_O Ohms	RS Ohms	RE Ohms
50	43	269
75	68	404
100	93	542
120	113	661

FIGURE 3. Series Termination Scheme

The advantages of the series termination method is that an additional V_{TT} supply is not required (unlike parallel termination), and all reflections are absorbed by the series resistor (RS). This makes series termination ideal for situations in which ringing and overshoots are present on the transmission line. A voltage divider action occurs at the beginning of the transmission line (marked **A** in Figure 3) which means that only half the amplitude of the driver output will be present along the line until the signal reaches the end of the transmission line. For this reason, loads should not be distributed along the line. For parallel and thevenin terminations, the full amplitude is seen on the line at all times.

Although there are other termination schemes available, the ones discussed above are the easiest, cost effective and most popular.

BOARD DESIGN CONSIDERATIONS

As with any good design, transmission line media, power/ground distribution, connectors, board layout, decoupling, and thermal effects must all be considered.

When designing a backplane with F100K 300 Series ECL logic, a controlled impedance transmission line is recommended. If the transmission line characteristic impedance is not matched along the line, reflections will occur. Available transmission line media include microstrip, stripline, coax, ribbon cable, and twisted pair to name a few. The most popular transmission line media for ECL is microstrip and stripline. Stripline is embedded within the layers of the PC board between two ground layers, while microstrip is run on the top and/or bottom layers of the board. Microstrip and stripline enable the designer to have very accurate and controlled impedances. This becomes important when determining delays and terminations within a designed system. It is important to remember that all transmission line types mentioned have a distinct propagation delay/unit length associated with them. As an example, microstrip lines on G10/FR4 boards have a propagation delay of approximately 1.77 ns/ft.

In order to transfer ECL signals from one board to another, a connector is needed. In most cases, the connector will cause impedance discontinuities. In order to keep reflections and signal distortions at a minimum, the discontinuity should be as small as possible. Although impedance matched connectors are expensive, the distortions that result are nearly negligible. Connectors also have a capacitance associated with them on the order of 1 pF–3 pF. This capacitance will of course have a direct effect on the backplane loading. When using edge connectors to interface data from a motherboard and a daughter card, several pins (>10%) should be dedicated to power and ground in order to maintain signal and power fidelity from one board to another. An example of this is shown in Figure 4.

When using a PC board with ECL and TTL logic together, the most noise will generally be found at the TTL ground. Since ECL logic levels are referenced directly from the V_{CC} line, it is critical to have a dedicated ECL V_{CC} plane that is stable and noise free. For this reason, the TTL ground and ECL V_{CC} planes are placed as far from each other as possible. Variations on V_{TT} and V_{EE} are more tolerable. Figure 5 shows a typical layout for an eight layer TTL/ECL PC board. Signals are run on both sides of the board for ease of connecting signals.

BOARD DESIGN CONSIDERATIONS (Continued)

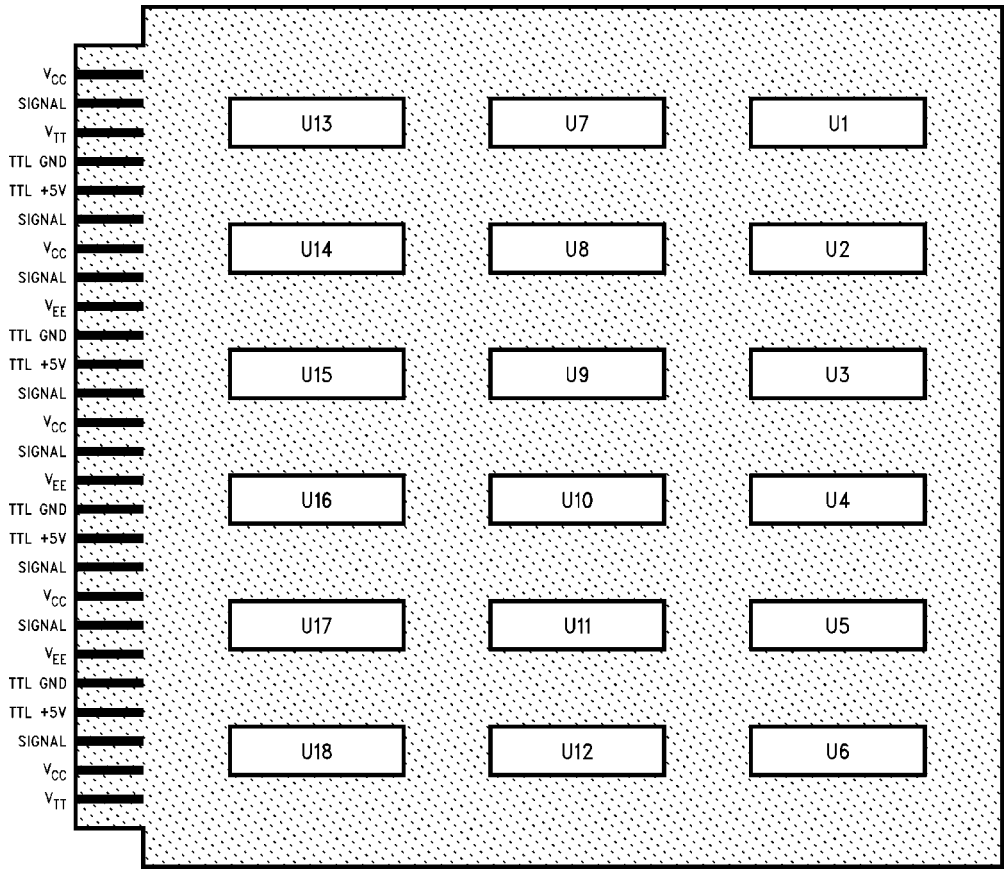


FIGURE 4. PC Board Pin Distribution

LAYER 1	Signal
LAYER 2	TTL Ground
LAYER 3	TTL +5V
LAYER 4	V_{TT}
LAYER 5	Signal/Thermal
LAYER 6	ECL –4.5V (V_{EE})
LAYER 7	ECL 0.0V (V_{CC})
LAYER 8	Signal

FIGURE 5. PC Board Power Planes

Inductance is always present in any conductor. As the rate of change in current through an inductor increases, the greater the induced voltage will be since V = L(di/dt). With digital systems changing logic levels, a change in current will inevitably occur and produce unwanted voltage drops. Oscillations are also connected with additional inductance present in digital circuits. This implies that inductance in board design should be kept at a minimum.

Inductance is very dependant on geometry, with solid sheet conductors being the best for keeping inductance at the lowest possible level. This is the reason why planes (as in Figure 5) instead of grids, combs, or traces are used for power and ground. It is best to mount IC's directly over ground planes and connect the device ground pins to it whenever possible. It is also recommended that decoupling capacitors of 0.01 µF to 0.1 µF be placed between V_{EE} and V_{CC}, and between V_{TT} and V_{CC}.

The power required for different IC's will vary, meaning that the heat dissipated by each will change. In order to maintain gate junction temperatures, cooling devices may be necessary. As an example, planes can be used as thermal mass resulting in an effective heat sink. Cooling is important because if junction temperatures exceed manufacturer specifications, circuits can fail, degrade, or function incorrectly.

SYSTEM DESIGN CONSIDERATIONS

Wired-OR Configuration

F100K 300 Series devices have an emitter follower configuration on each output. The open emitter outputs of several devices can be tied together to create a Wired-OR configuration. An example of this is shown in Figure 6. This configuration has the advantage of obtaining the OR operation without using an external gate, thus reducing the package count of the design. The Wired-OR also saves on power by

Wired-OR Configuration (Continued)

reducing the number of terminations needed (one termination for each Wired-OR grouping), and increases the speed of the system by removing the additional propagation delay that would have been inherent with an additional OR gate. Since ringing and undershoots are functions of the transmission line intrinsic capacitance and inductance, it is important to minimize these by using the shortest trace lengths possible.

Although the Wired-OR allows for additional levels of logic, there is a penalty. This penalty is a reduction in the LOW level noise margin. As the number of outputs tied together increases, the V_{OL} level rises significantly. With a single output in the LOW state of approximately −1.70V driving a 50Ω impedance terminated in −2.0V, a typical I_{OL} current of 6.0 mA flows. In the Wired-OR state with four outputs tied together (all in the LOW state), the I_{OL} current supplied by each output is nearly equal. The decreased current being supplied by each output transistor due to current sharing results in a reduction of the V_{BE} junction voltage which in turn raises the V_{OL} level. As a rule, the V_{OL} level will be raised approximately 25 mV for every two outputs that are tied together on a bus. It should also be mentioned that the V_{OH} levels will rise as the number of outputs tied together increases and thus the high level noise margin increases. This effect is usually ignored since V_{OH} is moving away from the threshold.

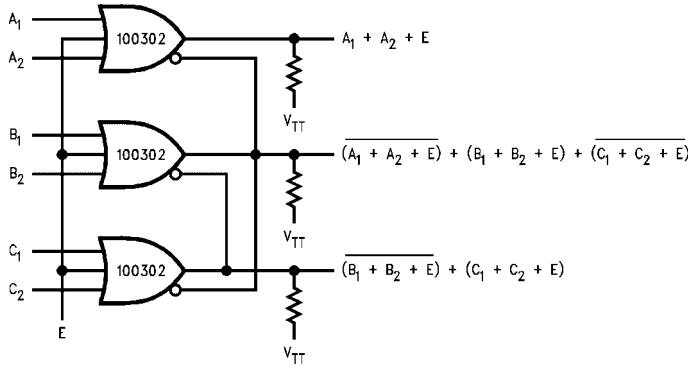


FIGURE 6. Wired-OR Configuration

Cutoff Drivers

The V_{OL} noise margin degradation found in Wired-OR networks can be avoided by using Fairchild octal cutoff driver devices. When the output enable (see Figure 7) of the cutoff driver is brought to a HIGH level, the base of the output transistor is biased to a level of −1.5V to −1.6V which in turn "cuts it off". This implies that a cutoff output will not source any current. With this, the HIGH and LOW level noise margins will not change from the non-Wired-OR situation. With the output in the cutoff state, an output capacitance of 3 pF is present on the backplane.

Loading Effects

As the number of devices tied to the backplane increases, distributed loading effects due to gate input and output capacitance need to be considered. The additional capacitance on the backplane reduces the effective characteristic impedance of the transmission line. This change indicates that in order to avoid reflections and terminate the line properly, a new terminating resistor needs to be calculated. The characteristic impedance for a lossless transmission line is calculated by:

$$Z_O = \sqrt{(L_O/C_O)}$$

Loading Effects (Continued)

Where:

L_O = intrinsic inductance/unit length

C_O = intrinsic capacitance/unit length

C_D = distributed capacitance

With the effects of distributed loading on the transmission line, the effective characteristic impedance becomes:

$$Z'_O = \sqrt{(L_O/(C_O + C_D)} = Z_O \div \sqrt{(1 + C_D/C_O)}$$

As an example, consider the distributed loading scheme shown in Figure 8. A 50Ω microstrip line, 10 inches long, on glass epoxy board (Er = 5.0), is used as the transmission line with five equally spaced distributed loads.

$C_O = t_{PD}/Z_O = 0.148$ ns/inch ÷ 50Ω = 2.96 pF/inch

With an input impedance of approximately 3.0 pF/gate (for PLCC devices);

$$C_D = Z_O \div \sqrt{(1 + C_D/C_O)} = 5\ (3.0\ pF)/10\ inches = 1.5\ pF/inch$$

This gives an effective transmission line impedance of

$$Z'_O = Z_O \div \sqrt{(C_O + C_D)} = 50 \div \sqrt{(1 + (1.5/2.96))} = 40.7\Omega$$

This implies that in order to terminate the transmission line properly, a terminating resistor (RT) of 40Ω is required.

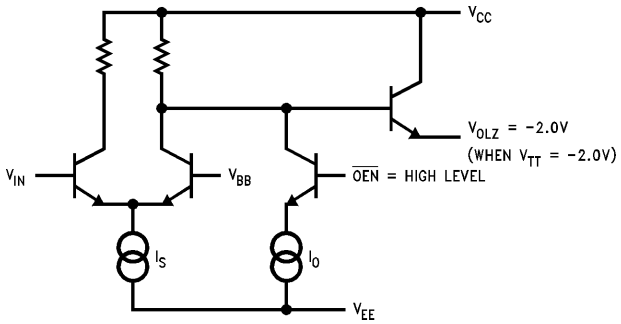


FIGURE 7. ECL Cutoff Driver

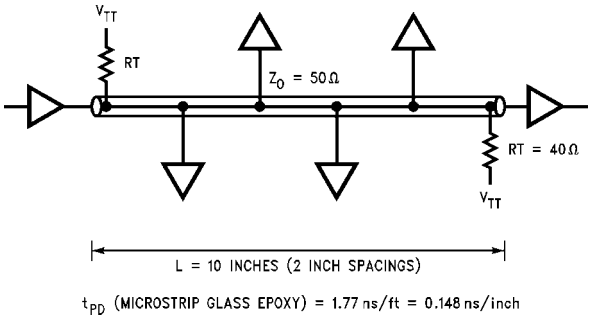


FIGURE 8. Distributed Loading Example

APPLICATION EXAMPLES

In order to transfer data efficiently on an ECL backplane, ECL drivers, receivers, translators, and transceivers are required. Single ended ECL backplane devices include the following:

100328	Octal ECL/TTL Bidirectional Translator with Latch
100329	Octal ECL/TTL Bidirectional Translator with Register
100343	Octal Latch (50Ω drive)
100344	Octal Latch with Cutoff Drivers (25Ω drive)
100352	Octal Buffer with Cutoff Drivers (25Ω drive)
100353	Octal Register (50Ω drive)
100354	Octal Register with Cutoff Drivers (25Ω drive)

Differential ECL backplane devices include the following:

100314	Quint Differential Line Receiver
100316	Quad Low Skew Differential Cutoff Driver (25Ω drive)
100319	Hex Single-Ended Input, Differential Output Cutoff Driver (25Ω drive)
100324	Hex TTL-to-ECL Translator
100325	Hex ECL-to-TTL Translator
100397	Quad Differential ECL/TTL Bidirectional Translator/Driver with Cutoff (25Ω drive)
100398	Quad Differential ECL/TTL Bidirectional Translator/Driver with Cutoff (25Ω drive), with TTL Control

Single-Ended ECL Backplane

A single-ended ECL backplane implies that signals are transmitted as a voltage on a single line referenced to AC ground. In the example shown in Figure 9, several listeners and talkers are tied to the common backplane. The 50Ω transmission line is terminated at both ends of the line in its characteristic impedance of 50Ω. This, in effect, requires a 25Ω driver. This need is satisfied with Fairchild Semiconductors 100344 octal latch with 25Ω cutoff drive, 100352 octal buffer with 25Ω cutoff drive, and the 100354 octal register with 25Ω cutoff drive. When designing such a system, the effects of connectors, transmission line delay, and load capacitance should all be considered as discussed previously.

Differential ECL Backplane

A single-ended backplane is susceptible to ground potential differences at the ends of the line thus creating distorted signals being transmitted or received. For this reason, a single-ended backplane is not recommended for noisy environments. Differential line driving (as shown in Figure 10) has a high noise rejection which results in a more reliable data transmission. Common mode voltages of ≤–2.0V are rejected with an input voltage differential of 150 mV required for full output swing. (Please refer to V_{CM} specification for the 100314 in the F100K ECL Databook.)

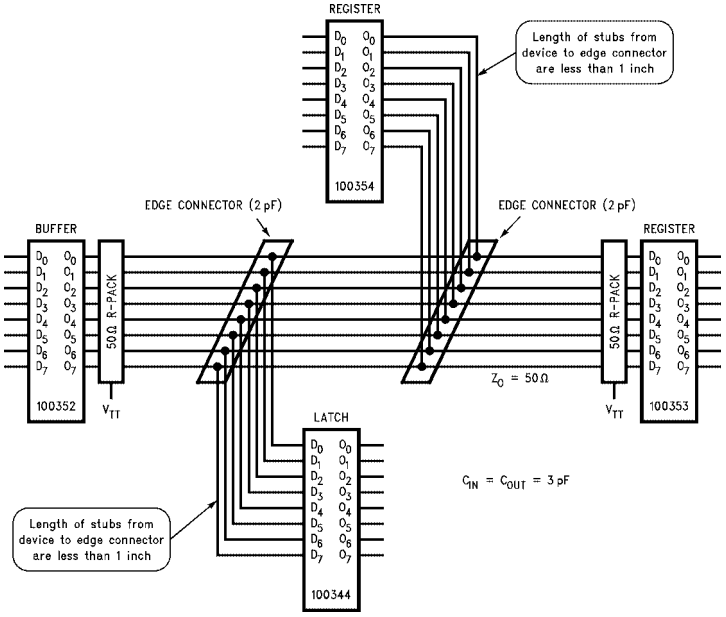


FIGURE 9. Single-Ended ECL Backplane

The differential line driver and receivers communicate over a pair of wires where one is a HIGH voltage level and the other must be a LOW. If external noise occurs near the differential line, both wires will obtain the same distortions. Since the noise present on both of the lines is the same, the signal received at the terminated end of the line will not be effected because it is obtained by the difference of the signals on the lines. The difference of two lines will be the same with or without the noise problem. The advantage of a differential line driving scheme is the clean transmission of signals in noisy or industrial environments. As the differential line driving application in Figure 10 shows, in order to isolate unused outputs from the line 25Ω cutoff drivers are required. With the introduction of Fairchild Semiconductors 100316 quad differential 25Ω cutoff driver, 100319 hex single-ended input, differential output 25Ω cutoff driver, and 100397/100398 ECL/TTL quad bidirectional translators/drivers with latch and ECL 25Ω cutoff drive, this type of application is now possible. The 100397 has ECL control pins while the 100398 offers TTL control pins.

ECL Transceiver

Although an ECL transceiver does not currently exist, creating one is rather simple when using 25Ω cutoff driver devices as shown in Figure 11. This device could be used to communicate between a single-ended or differential ECL bus and other circuitry. The circuit shown uses two 100352 devices configured to give a transceiver operation. The function table for the operation of the transceiver is shown in Figure 11. In order to transmit data from A to B, $\overline{OEN}_2$ is HIGH while $\overline{OEN}_1$ is LOW. The HIGH level on $\overline{OEN}_2$ "cuts off" the bottom driver and allows for data transfer from A to B. To transfer data from B to A, $\overline{OEN}_1$ is held HIGH with $\overline{OEN}_2$ at a LOW level. When both output enable pins are at a HIGH level, both 100352 devices are in the cutoff state which results in a lower than low V_{OLZ} state (V_{OLZ} = –2.0V) at points A and B.

ECL Transceiver (Continued)

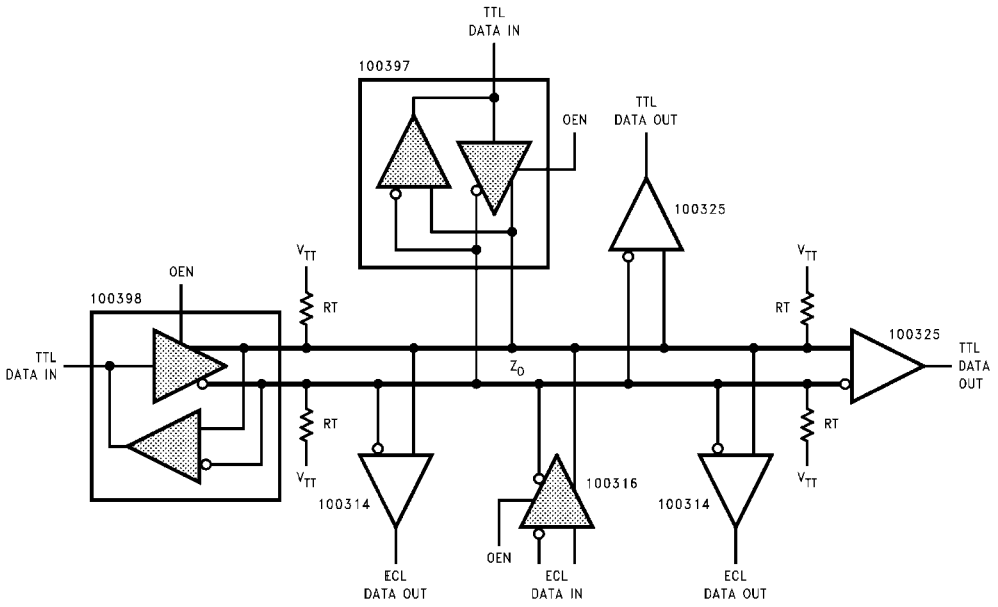
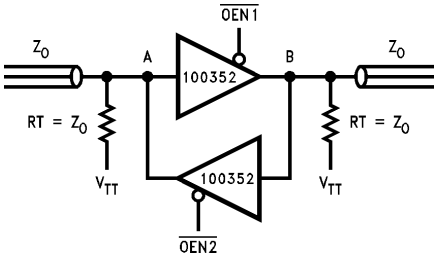


FIGURE 10. Differential ECL Backplane (1-Bit)



Truth Table

$\overline{OEN}_1$	$\overline{OEN}_2$	Outputs
L	L	A, B HIGH
L	H	Bus A Data to Bus B
H	L	Bus B Data to Bus A
H	H	A, B, Cutoff (V_{OLZ})

FIGURE 11. ECL Transceiver