APPLICATION NOTE

75W SMPS with TEA1507 Quasi-Resonant Flyback controller

Draft2 AN00047

Philips Semiconductors

TP97036.2/W97

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Abstract

This application note describes a 75W Switched Mode Power Supply (SMPS) for a typical Monitor or TV-application based upon the TEA1507 Quasi-Resonant controller. The power supply is based on a Flyback topology and operates in the critical conduction mode at various frequencies depending on the output load and input voltage. The TEA1507 uses current mode (on-time) control. This concept allows a very high efficiency also in low power mode as result of valley (zero/low voltage) switching. Depending on the component values it is possible to perpetrate the supply in no-load condition.

APPLICATION NOTE

75W SMPS with TEA1507 Quasi-Resonant Flyback controller

Draft1 AN00047

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Keywords

Flyback converter
Quasi-Resonant
Low power standby
Valley Switching
High efficiency

Number of pages: 39

Date: 2000-06-30

Summary

The TEA1507 controller is part of the GreenChip ™ family. It is intended for off-line $90V_{AC}$-$276V_{AC}$ power supply applications. The controller is optimized for a very high efficiency operation up to 90% utilizing an integrated start-up current source, a special valley switching feature, a special standby VCO mode or standby burst mode feature and low power consumption. The controller is equipped with many protection features, such as an accurate Over Voltage Protection, Over Current Protection, Over Power Protection, Over Temperature Protection, Demagnetization Sensing, Maximum and Minimum On Time Protection and Short Winding Protection. Another feature is the programmable Soft Start at primary side.

This application note starts with the introduction of the main application features (chapter 1) followed by Quasi-Resonant Flyback topology description in chapter 2. Functionality of the TEA1507 is descriped in chapter 3. In chapter 4 the design of a typical universal range monitor supply (cookbook) is described in more detail with some attached measurement results (chapter 5, EMI included). In the appendix a more detailed description of the QR-waveforms are treated.

CONTENTS

1. INTRODUCTION

The GreenChip^{TM} TEA1507 is a variable frequency SMPS controller designed for a Quasi-Resonant Flyback converter operating directly from the rectified universal mains (see Figure 1). The topology is in particular suitable for TV and Monitor Supplies. During nominal load it operates in a critical conduction mode including zero/low voltage switching (ZVS/LVS). The ZVS/LVS is achieved by the resonant behavior of the voltage across the power switch. This is also called the Quasi-Resonant mode. The Valley detection implemented in the controller ensures this ZVS/LVS operation.

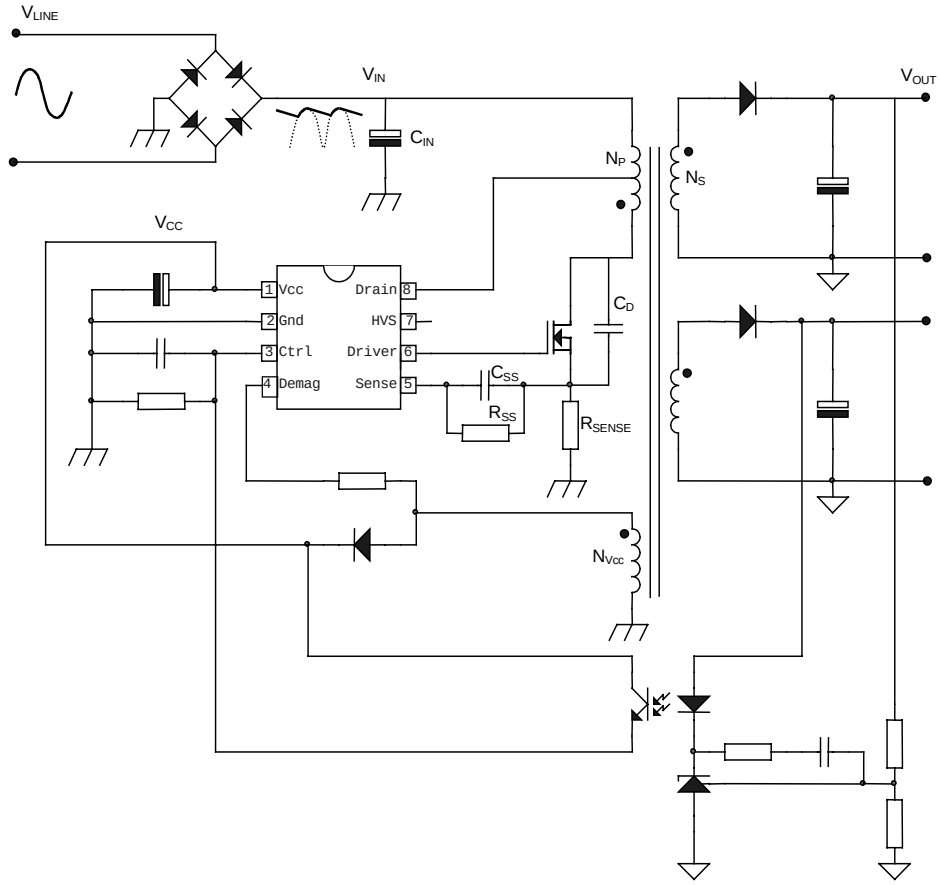

Figure 1 Quasi-Resonant Flyback converter

The control method applied in the TEA1507 is known by the name ‘Current-mode control’ with the benefit of having a good input line regulation. Control takes place by regulating the primary peak current that result in a frequency change depending on the power stage. The input voltage and the output load influence the frequency. The IC controls the turn-on moment of the power switch for ZVS/LVS operation by using the valley detection.
Feedback is provided by means of an opto-coupler, through which a good stabilization and good ripple suppression can be obtained.

The controller provides two different types of stand-by possibilities. The first is Frequency Reduction to minimize the switching losses at minimum output load. This feature enables stand-by power consumption below 3W and needs no additional circuitry. A second alternative for stand-by power consumption below 1W is called Burst mode, which needs only little additional circuitry.

The key features of the TEA1507 are:

Distinctive features
- Operates from universal mains input $85V_{AC}$ – $276V_{AC}$
- High level of integration leads to a very low external component count
- Soft (re)Start to prevent audible noise (ajustable)
- Leading Edge Blanking (LEB) for current sense noise immunity

Green features
- On-chip start-up current source, which is switched off after start-up
- Valley (zero/low voltage) switching for minimal switching losses
- Frequency Reduction at low power stand-by for improved system efficiency (power consumption < 3W)
- Burst mode operation for very low stand-by levels (power consumption <1W)

Protection features
- Safe-Restart mode for system fault conditions
- Mains dependent operation enabling level (Mlevel) (adjustable)
- Under Voltage Protection (UVLO) for foldback during overload
- Continuous mode protection by means of demagnetization detection
- Accurate Over Voltage Protection (OVP) over demag (adjustable)
- Cycle-by cycle Over Current Protection (OCP)
- Input voltage independent Over Power Protection (OPP)
- Short Winding Protection (SWP)
- Ton max Protection
- Over Temperature Protection (OTP)

These features enables an engineer to design a reliable and cost effective supply with a minimum number of external components and the possibility to deal with requirements on minimum power consumption during stand-by or other system idle modes.

2. QUASI-RESONANT FLYBACK TOPOLOGY

The Quasi-Resonant Flyback topology is very appropriate for TV or monitor applications because this topology has some important benefits compared to the “hard switching” fixed frequency Flyback topology. The efficiency can be improved up to 90%, which results in lower power consumption. Referring to an important requirement of monitor and/or TV supply it is possible to keep the input power below 75W, so that an additional PFC/MHR is not required. This will save total supply costs.
The resonant behavior makes it possible to turn on the MOSFET when the voltage has reached zero (ZVS) or the minimum value (LVS), which reduces the switch-on losses. Also the switch-off losses and the noise (dV/dt) will be reduced by the resonance capacitor. Further more the QR Flyback runs at the borderline between discontinuous (DCM) and continuous conduction mode (CCM). This means smaller peak and RMS currents in the circuit compared to fixed frequency DCM Flyback, which results in a more efficient power conversion.

For a clear understanding of the Quasi-Resonant behavior it is possible to explain it by a simplified circuit diagram of the Quasi-Resonant Flyback topology (see Figure 2). In this circuit diagram the secondary side is transferred to the primary side and the transformer is replaced by an inductance L_P. C_D is the total drain capacitance including the resonance capacitor C_R, parasitic output capacitor C_{OSS} of the MOSFET and the winding capacitance C_W of the transformer. The turns ratio of the transformer is represented by n (N_P/N_S).

In the Quasi-Resonant mode each period can be divided into four different time intervals (see Figure 3), in chronological order:

Interval 1:	$t_0 < t < t_1$	primary stroke	$t_{PRIM} = t_1 - t_0$
Interval 2:	$t_1 < t < t_2$	commutation time	$t_{COM} = t_2 - t_1$
Interval 3:	$t_2 < t < t_3$	secondary stroke	$t_{SEC} = t_3 - t_2$
Interval 4:	$t_3 < t < t_{00}$	dead time	$t_{DEAD} = t_{00} - t_3$

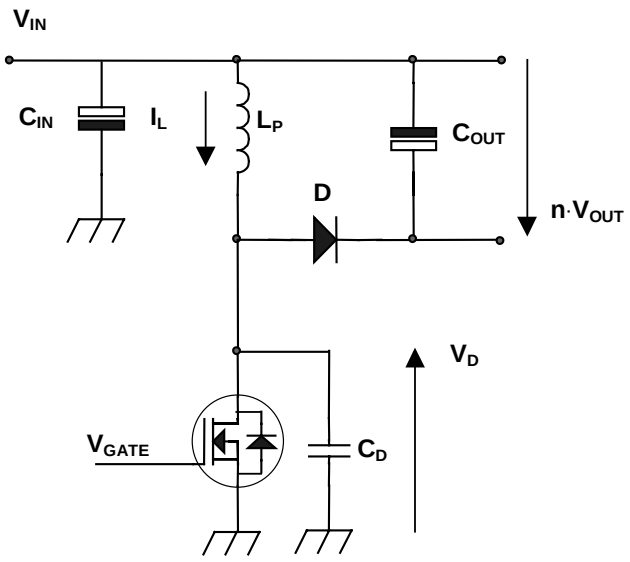

Figure 2 Basic circuit diagram

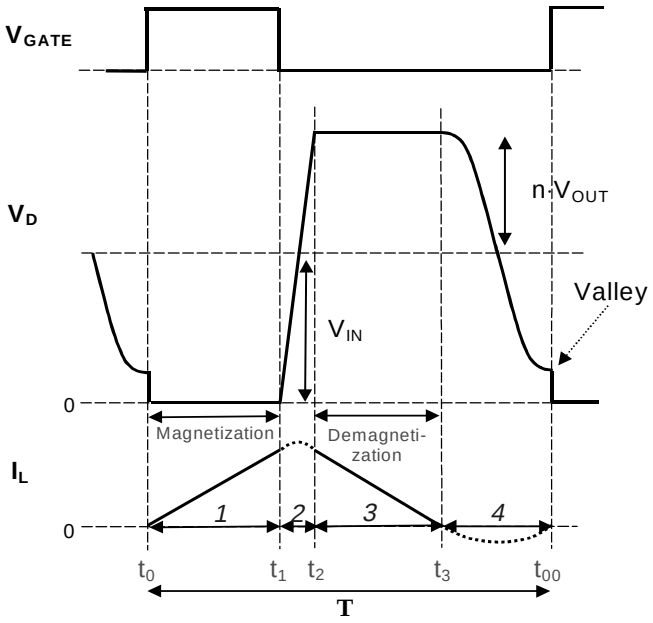

Figure 3 QR waveforms

At the beginning of the first interval, the MOSFET is turned on and energy is stored in the transformer (magnetization). At the end the MOSFET is switched off and the second interval starts.

In the second interval the drain voltage will rise from almost zero to $V_{IN}+n\cdot(V_{OUT}+V_F)$. V_F is the forward voltage drop of de diode that will be omitted from the equations from now on. The current will change its positive derivative, corresponding to V_{IN}/L_P, to a negative derivative, corresponding to $-n\cdot V_{OUT}/L_P$.
In the third interval the stored energy is transferred to the output, so the diode starts to conduct and the inductive current I_L will decrease. In other words the transformer will be demagnetized. When the inductive current has become zero the next interval begins.
In the fourth interval the energy stored in the drain capacitor C_D will start to resonate through the inductance L_P. The voltage and current waveforms are sinusoidal waveforms (see Figure 3) with an oscillation frequency of approximately:

$$f_{OSC} = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{L_P \cdot C_D}}$$ Equation 1

The drain voltage will drop from $V_{IN}+n\cdot V_{OUT}$ to $V_{IN}-n\cdot V_{OUT}$.
Depending on the input voltage three situations has to be distinguished:

Situation	Drain voltage at switch-on
1] $V_{IN} = n\cdot V_{OUT}$	ZVS
2] $V_{IN} < n\cdot V_{OUT}$	ZVS
3] $V_{IN} > n\cdot V_{OUT}$	LVS

Table 1 Zero Voltage Switching/Low Voltage Switching

In situation 1 the minimum drain voltage will be zero because V_{IN} equals $n\cdot V_{OUT}$. The controller detects this minimum and the MOSFET will be turned on again.
In situation 2 the input voltage is smaller than $n\cdot V_{OUT}$. The drain voltage wants to become negative, but the internal body diode of the MOSFET starts conducting and the voltage is clamped at the negative voltage drop of this diode. The controller detects this also as a valley and the MOSFET is turned on again. In both situations the switch-on losses become zero, which is a big advantage of the Quasi-Resonant Flyback topology.
In the third situation the minimum drain voltage stays above zero (see Figure 3). The controller will detect this valley and the switch-on losses will be very low even in this situation. For a more detailed description of all the intervals see APPENDIX 2.

Frequency behavior:
The frequency in the QR-mode is determined by the power stage and is not influenced by the controller (important parameters are L_P and C_D). The frequency varies with the input voltage V_{IN} and the output power P_{OUT}. If the required output power increases more energy has to be stored in the transformer. This leads to longer magnetizing t_{PRIM} and demagnetizing t_{SEC} times, which will decrease the frequency. See the frequency versus output power characteristics of Figure 4. The frequency characteristic is not only output power but also input voltage dependent. The higher the input voltage the higher the frequency will be.

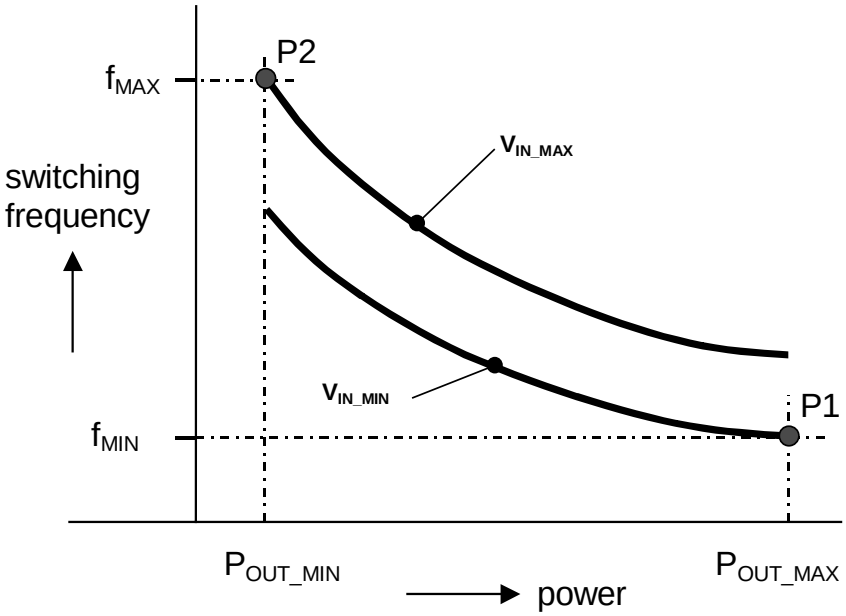

Figure 4 QR frequency characteristics at different input voltages

Point P1 is the minimum frequency f_{MIN} that occurs at the specified minimum input voltage and maximum output power required by the application. Of course the minimum frequency has to be chosen above the audible limit (>20kHz), but in principle the designer is free to choose the minimum frequency. The minimum frequency mainly defines the primary inductance and because of this also the (core) size of the transformer. In applications operating over the entire input voltage range (85Vac … 276Vac) it is not possible to choose a high minimum frequency because in this case the frequency at minimum load and high input voltage (see point P2 in Figure 4) will end up unacceptable high. See chapter 4 for a design example.

3. FUNCTIONAL IC DESCRIPTION

This chapter describes the functionality of the QR Flyback controller and all the different modes in which the controller can operate. It also describes how the features and protections are implemented in the controller. Table 3 in paragraph 3.6 shows an overview of the different functions behind each pin.

3.1 Start-up sequence

When the rectified line voltage V_{IN} (via the center tap connected to pin 8) reaches the Mains dependent operation level (Mlevel), the internal Mlevel switch will be opened and the start-up current source is enabled to charge the capacitor at the V_{CC} as shown in Figure 5. The soft start switch is closed when the Vcc reaches a level of 7V and the Soft start capacitor C_{SS} between the sense pin and the sense resistor is charged to 0.5V. Once the V_{CC} capacitor is charged to the start-up voltage (11V) the IC starts driving the MOSFET. Both internal current sources are switched off after reaching this start-up voltage. Resistor R_{SS} will discharge the soft start capacitor, such that the peak current will slowly increase. This will overcome audible noise caused by magnetostriction in the transformer. The time constant of the decreasing sense voltage (representing the increasing primary peak current) can be adjusted by choosing a different C_{SS} and/or R_{SS}. To use the total soft start window R_{SS} should be larger than (V_{OCP} = 0.5V divided by I_{SS} = 60µA) 8kΩ to be sure it is charged to 0.5V. During start-up the V_{CC} capacitor will be discharged until the V_{CC} winding voltage will take over charging the V_{CC} capacitor.

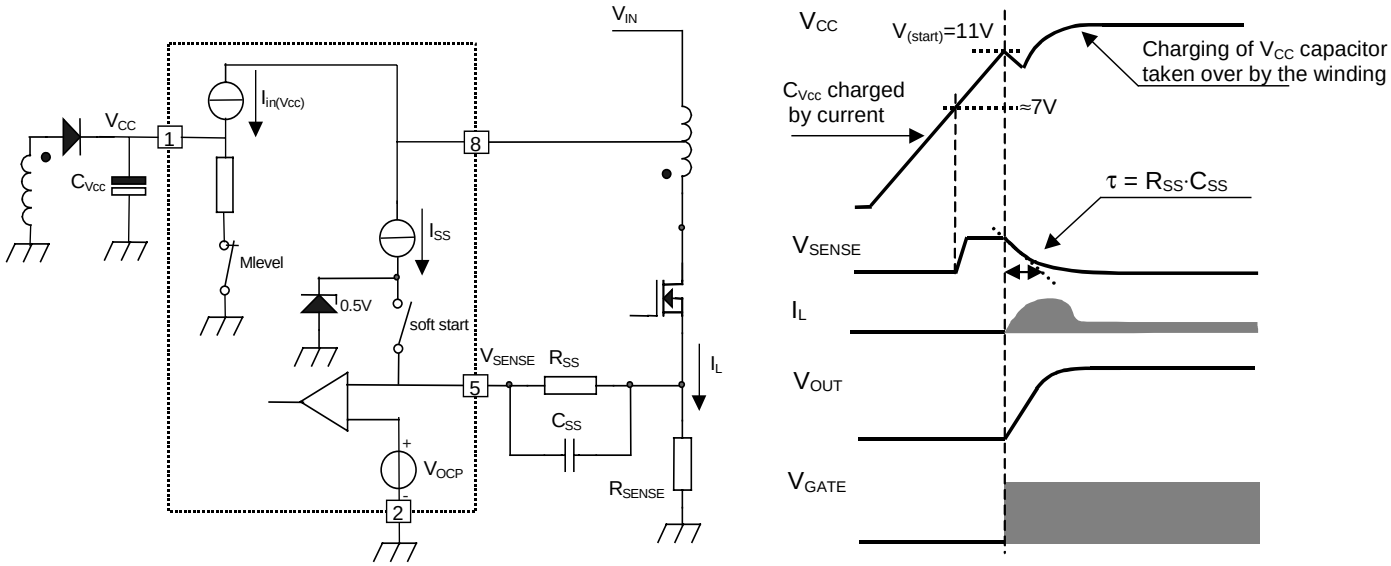

Figure 5 Start-up sequence

3.2 Multi mode operation

The supply can run in four different modes depending on the output power:

1. Quasi-Resonant mode QR;
2. Maximum frequency mode MaxF;
3. Frequency reduction mode FR;
4. Minimum frequency mode MinF.

The QR mode, described in the previous chapter, is used during normal operation, which gives a high efficiency. The maximum frequency mode is not entered during nominal conditions (probably only at maximum input voltage and low loads). But also in this mode it is still possible to take advantage of the reduced switch-on losses because of valley switching.
If referring to most Monitor or TV application it is possible to distinguish two stages: Normal operation and Stand-by operation. The relation between converter modes and load stages has to be as represented in the table below.

Supply mode	Load stage
1. Quasi-Resonant mode	A. Normal operation: $P_{OUT\_MIN} < P_{OUT} < P_{OUT\_MAX}$
2. Maximum Frequency mode	not entered
3. Frequency Reduction mode	B. Stand-by operation: $P_{OUT} = P_{STAND-BY}$
4. Minimum Frequency mode	

Table 2 Converter modes

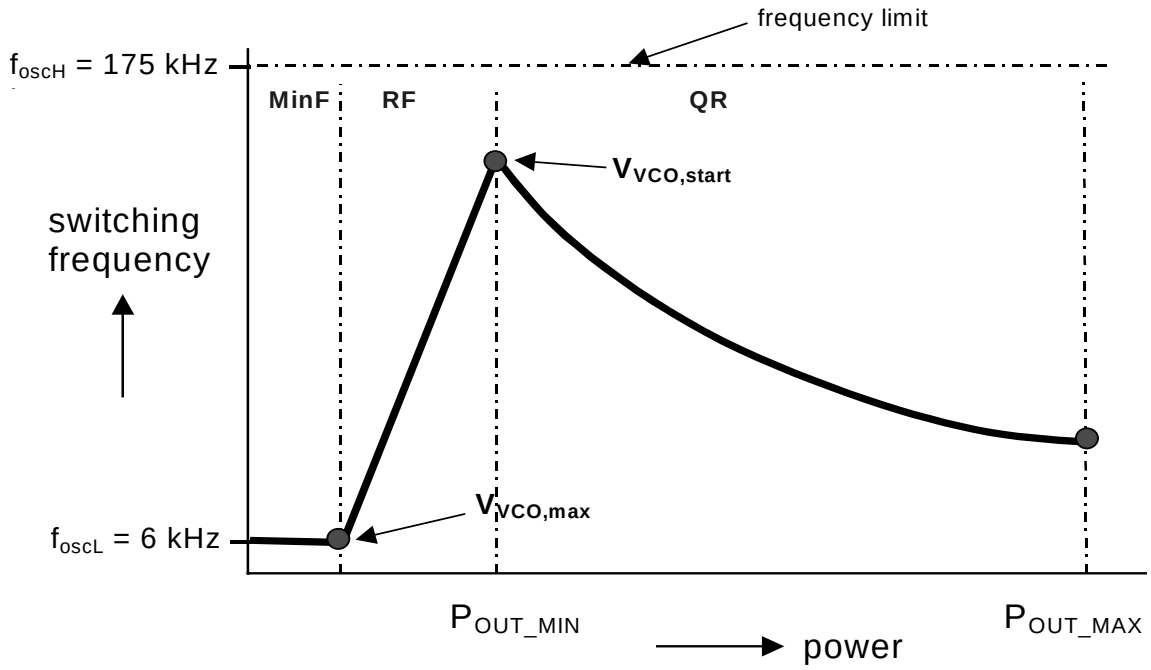

Figure 6 Multi mode operation

The frequency reduction mode FR (also called VCO mode) is implemented to decrease the switching losses at low output loads. In this way the efficiency at low output powers is increased, which enables power consumption smaller than 3W during stand-by.
The voltage at the Sense pin determines where the frequency reduction starts. This fixed sense level of 75mV is called $V_{VCO,start}$ (see Figure 6). This sense voltage controls the frequency of the internal oscillator over the range between 75mV and 50mV (At sense level larger than 75mV the oscillator will run on maximum frequency f_{oscH} = 175kHz typically). At 50mV ($V_{VCO,max}$) the frequency is reduced to the minimum level of 6kHz. The valley switching is still active in this mode.

At sense levels below 50mV the minimum frequency will remain on 6kHz called MinF mode. When the required output power decreases the controller will decrease the on-time, limited T_{ON_MIN} = 350ns. As a result of this low frequency it is possible to run at very low loads without having any output regulation problems.

3.3 Safe-Restart mode

This mode is introduced to prevent the components from getting destroyed during eventual system fault conditions. This mode is also used for one operational issue, namely Burst mode. The Safe-Restart mode will be entered if it is triggered by one of the following features:

- Over Voltage Protection;
- Short Winding Protection;
- Maximum 'on time' Protection;
- Over Temperature Protection;
- detecting a pulse for Burst mode;
- V_{CC} reaching UVLO level.

When entering the Safe-Restart mode the output driver is immediately disabled and latched. The V_{CC} winding will not charge the V_{CC} capacitor anymore and the V_{CC} voltage will drop until UVLO is reached. To recharge the V_{CC} capacitor the internal current source ($I_{(restart)(Vcc)}$) will be switched on to initiate a new start-up sequence as described in paragraph 3.1. This Safe-Restart mode will persist until the controller detects no faults or burst triggers.

3.4 Protections

3.4.1 Demagnetization sensing

This feature guarantees discontinuous conduction mode operation in every situation. The function is an additional protection feature against saturation of the transformer/inductor, damage of the components during initial start-up and an overload of the output. The demag(netization) sensing is realised by an internal circuit that guards the voltage (V_{demag}) at pin 4 that is connected to Vcc winding by resistor R_1. Figure 7 shows the circuit and the idealized waveforms across this winding.

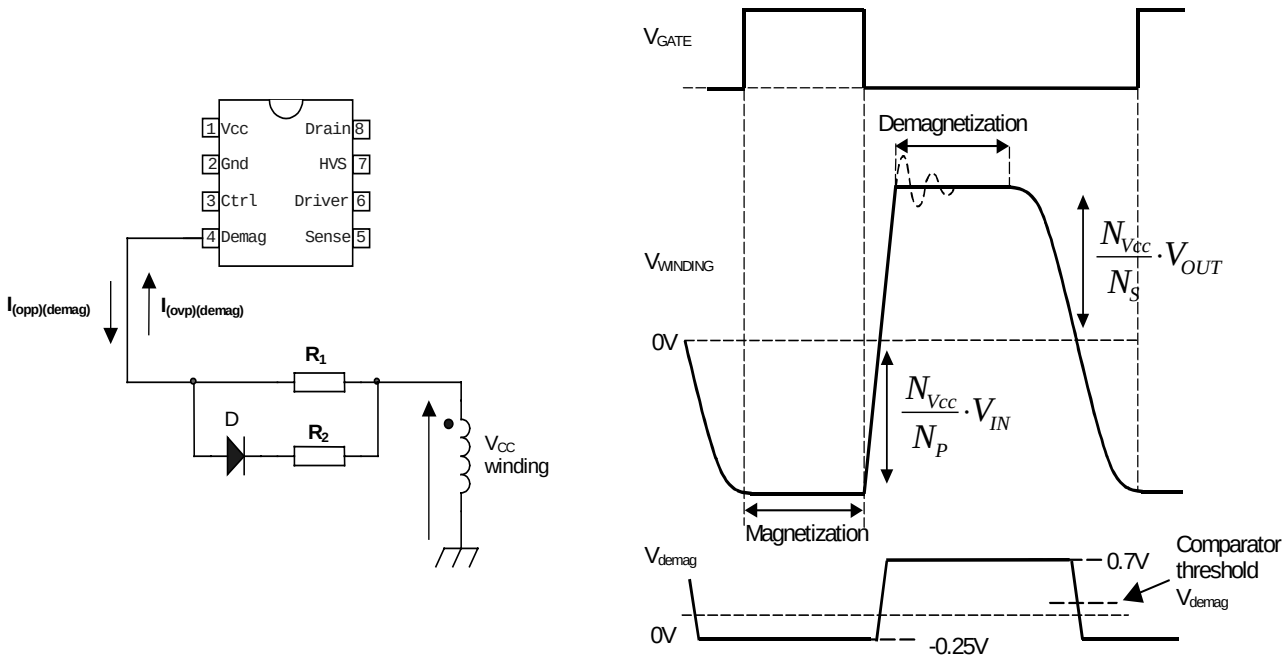

Figure 7 Demagnetization sensing

As long as the output diode is conducting (demagnetization of transformer), the winding voltage is positive. In this case V_{demag} is also positive and clamped at a level of 0.7V. The controller will force the driver output to stay off as long as the voltage at pin 4 is positive and above 100mV. In other words an increase of the switching period is a consequence of the demagnetization feature. After demagnetization the reflected output voltage at the auxiliary winding goes down. When the voltage comparator threshold V_{demag} < 100mV is reached the controller will wait for valley detection to allow a new switching cycle. OVP and OPP are using the same pin. These two functions determine the resistor value of R_1 and R_2. The following paragraph will describe these features.

3.4.2 Over Voltage Protection

The Over Voltage Protection ensures that the output voltage will remain below an adjustable level. This is realized by sensing the reflected output voltage across the V_{CC} winding via the current flowing into the Demag pin. This voltage equals the output voltage corresponding to the turns ratio of the V_{CC} winding and the secondary winding. The maximum output voltage is set by the resistor value R_1 that determines the current into the Demag pin. This current is mirrored and compared to a threshold level of 60µA. When this is reached the OVP is triggered. Choosing the maximum output voltage will determine the resistor R_1 that is calculated by the following equation:

$$R_1 = \frac{\left(\frac{N_{Vcc}}{N_s} \cdot OVP\right) - V_{clamp,demag(positive)}}{I_{(ovp)(demag)}}$$ Equation 2

Where,

N_{Vcc} = V_{CC} number of turns

N_S = secondary number of turns

OVP = maximum output voltage

$V_{clamp,Demag(positive)}$ = positive clamp voltage of Demag pin (0.7V)

$I_{(ovp)(Demag)}$ = current threshold of OVP protection (60µA)

After triggering the OVP the driver is disabled and the controller enters the Safe-Restart mode. This will stay as long as the over voltage is present at the output.
The dashed line in Figure 7 shows the more practical waveform at the V_{cc} winding. The ringing is caused by the leakage inductance of the transformer. To compensate this ringing (load dependent) the current into the Demag pin is integrated over the demagnetization time. False triggering of the OVP is prevented in this way, which result in a very accurate OVP.

3.4.3 Over Current and Over Power Protection

The maximum output power limitation needs some special attention when using a Quasi-Resonant converter. The maximum primary peak current I_{L_peak} does not only define the output power but also the input voltage because the operating frequency is input voltage dependent (see equation below).

$$P_{OUT\_MAX} = \eta \cdot \frac{1}{2} \cdot L_P \cdot {I_{L\_peak}}^2 \cdot f$$ Equation 3

Where f is input voltage depending

$$f = \frac{1}{t_{PRIM} + t_{COM} + t_{SEC} + t_{DEAD}}$$

$$t_{PRIM} = \frac{L_P \cdot I_{L\_peak}}{V_{IN}}$$

Equation 4

The maximum output power will increase with the input voltage when the OCP level would be a fixed level. To prevent over dimensioning of all the secondary power components an internal OCP compensation is used to get an independent OPP level. This compensation is realized by sensing the input voltage level via the V_{CC} winding. A resistor is connected between this winding and the demag pin. During magnetization of the transformer the reflected input voltage is present at this winding (see Figure 7). A negative current into this pin is used to compensate the OCP level. Figure 8 shows the relation between the negative current and OCP level.

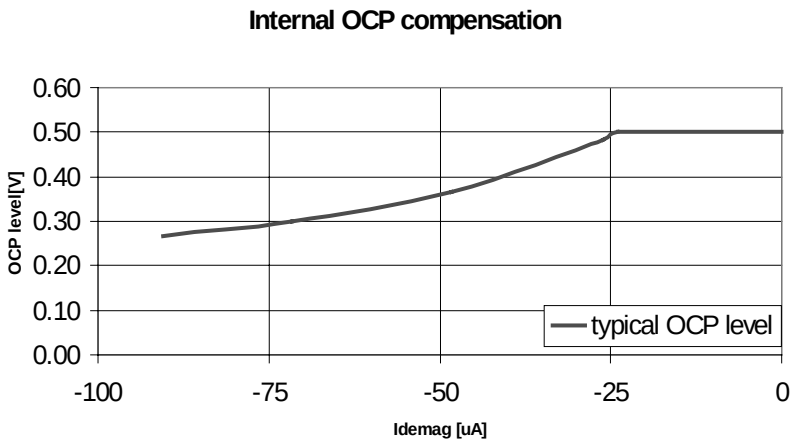

Figure 8 Internal OCP compensation

The current threshold level where the controller starts to compensate the OCP level is fixed at - 24µA. This threshold level is used to set the external resistor value at the minimum input voltage. The OVP and OPP protections are separated by means of a diode in series with R_2 (see Figure 7). The forward voltage drop of this diode is also taken into account when calculating the resistor R_2. Resistor R_2 is calculated by substituting the minimum input voltage and the current threshold level (see equation below).

$$R_2 = \frac{\left(\frac{N_{Vcc}}{N_P} \cdot V_{IN\_MIN}\right) + V_{clamp,demag(negative)} - V_F}{I_{(opp)(demag)} - \frac{\left(\frac{N_{Vcc}}{N_P} \cdot V_{IN\_MIN}\right) + V_{clamp,demag(negative)}}{R_1}}$$

Equation 5

Where,

N_{Vcc} = V_{CC} number of turns

N_P = primary number of turns

V_{IN_MIN} = minimum input voltage

$V_{clamp,demag(negative)}$ = negative clamp voltage of Demag pin (-0.25V)

V_F = forward voltage drop of diode
$I_{(opp)(demag)}$ = current threshold of OPP protection (-24μA)

3.4.4 Short Winding Protection

The short winding protection is implemented to protect against shorted transformer windings, for example in case of a secondary diode short. In this case the primary inductance is shorted out and the primary current starts to rise at very high rate (only limited by the leakage inductance) after turn on of the MOSFET. An extra comparator (fixed threshold of V_{swp} = 880mV) implemented in the IC will detect this fault condition by sensing the voltage level (via pin 5) across the sense resistor. Immediately the driver is disabled and the controller enters the Safe-Restart mode. This protection circuit is activated after the leading edge blanking time (LEB).

3.4.5 Minimum and maximum 'on-time'

The LEB (Leading Edge Blanking) time is an internally fixed delay that determines the minimum 'on time' of the controller. This minimum on time together with the minimum switching frequency and the primary inductance defines the minimum input power at which the output voltage is still in regulation. Because this minimum frequency is low it is possible to run at extremely low loads (without any pre-load).
The IC will protect the system against an 'on-time' longer then 50μs (internally fixed maximum 'on-time'). When the system requires on times longer than 50μs, a fault condition is assumed, and the controller enters the Save-Restart mode.

3.4.6 Over Temperature protection

When the junction temperature exceeds the thermal shutdown temperature (typ 140°C), the IC will disable the driver. When the V_{CC} voltage drops to UVLO, the V_{CC} capacitor will be recharged to the $V_{(start)}$ level. If the temperature is still too high, the VCC voltage will drop again to the UVLO level (Safe-Restart mode). This mode will persist until the junction temperature drops 4 degrees typically below the shutdown temperature.

3.4.7 Mains dependent operation enabling level

To prevent the supply from starting at a low input voltage, which could case audible noise, a mains detection is implemented (Mlevel). This detection is provided via pin 8(no additional pin needed), which detects the minimum start-up voltage between 60V and 100V. As previous mentioned the controller is enabled between 60V and 100V. This level can be adjusted by connecting a resistance in series with the drain pin, which increases the level by $R_1.I_{in(Drain)}$ volts.
An additional advantage of this function is the protection against a disconnected buffer capacitor (C_{IN}). In this case the supply will not be able to start-up because the V_{CC} capacitor will not be charged to the start-up voltage.

3.5 Burst mode Stand-by

Burst mode can be used to reduce the power consumption below 1W at stand-by. During Burst mode the controller is active (generating gate pulses) for only a short time and for a longer time inactive waiting for the next burst cycle. In the active period the energy is transferred to the secondary and stored in the buffer capacitor C_{STAB} in front of the linear stabilizer (see Figure 9). During the inactive period the load (e.g. microprocessor) discharges this capacitor. In this mode the controller makes use of the Safe-Restart mode.

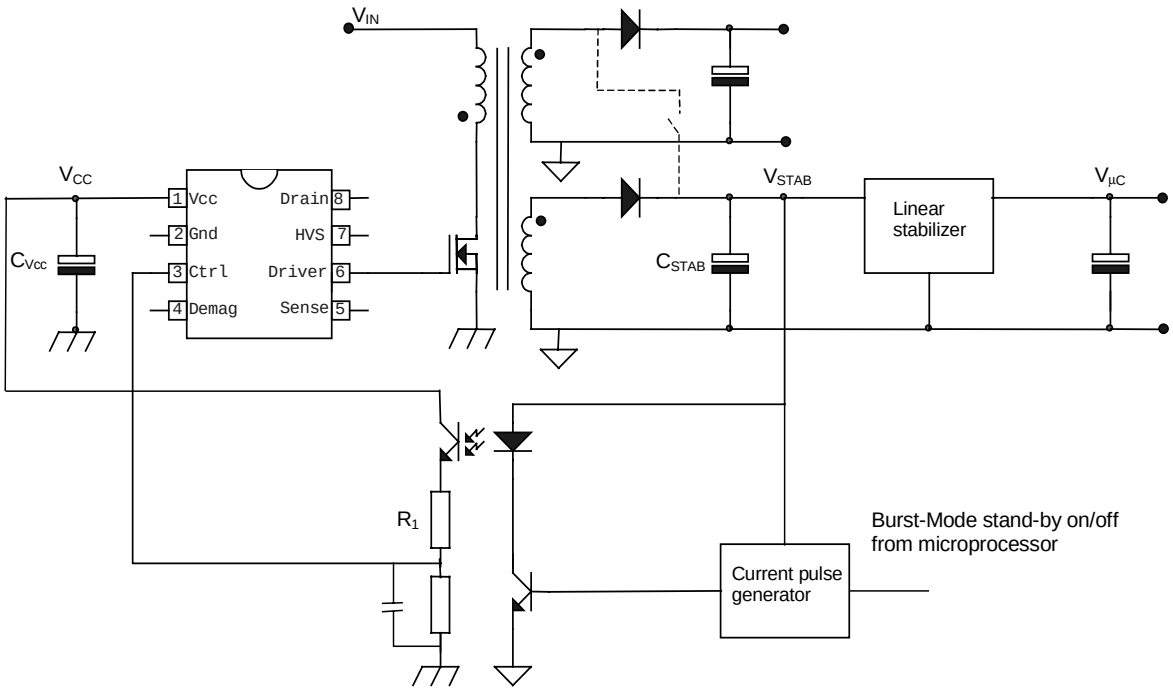

Figure 9 Basic Burst mode configuration

For a more detailed description of one burst cycle three time intervals are defined:

- **t1** Discharge of V_{CC} when gate drive is active
- **t2** Discharge of V_{CC} when gate drive is inactive
- **t3** Charge of V_{CC} when gate drive is inactive

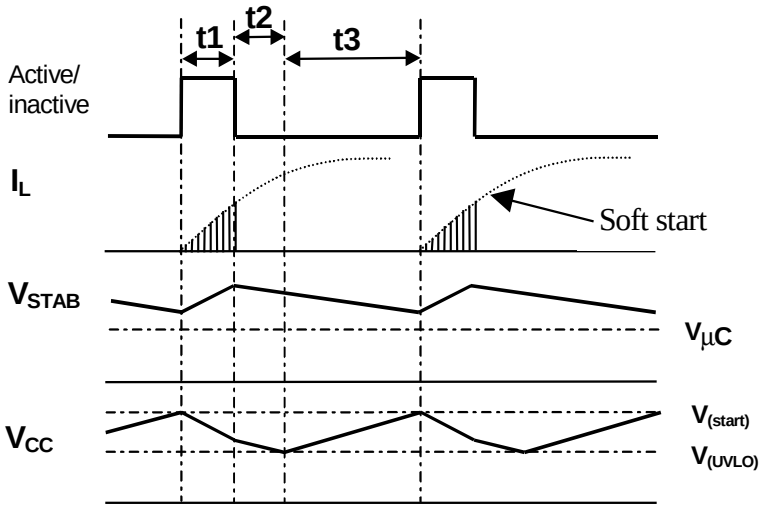

Figure 10 Burst mode waveforms

During the first interval energy is transferred, which result in a ramp-up of the output voltage (V_{STAB}) in front of the stabilizer. When enough energy is stored in the capacitor the IC will be switch-off by a current pulse generated at the secondary side. This pulse is transferred to the primary side via the opto coupler. When this pulse reaches a threshold level of 16mA into the Ctrl pin it will stop switching. Because of the large variation on the CTR of the opto coupler a resistor (R_1) is placed in series to limit the current going into the Ctrl pin. Meanwhile the V_{CC} capacitor is discharged but has to stay above V_{UVLO} (see
Figure 10).
During the second interval the V_{CC} is discharged to V_{UVLO}. The output voltage will decrease depending on the load. The third interval starts when the UVLO is reached. The internal current source charges the V_{CC} capacitor (also the soft start capacitor is recharged). Once the V_{CC} capacitor is charged to the start-up voltage the driver is activated and a new burst cycle is started.
The dotted line in Figure 9 shows an additional switch connected between the high voltage winding (e.g. 185V or 80V) and the output that supplies the microprocessor. Closing the switch during Burst mode gives an voltage reduction of the unused outputs. Reducing the output voltage will prevent consuming any power by these unused outputs, which result in lower power consumption during stand-by.

3.6 Pin description GreenChip™ TEA1507

SYMBOL	PIN	DESCRIPTION
Vcc	1	This pin is connected to the supply voltage. An internal current source charges the V_{CC} capacitor and a start-up sequence is initiated when the voltage reaches a level of 11V. The output driver is disabled when the voltage gets below 9V(UVLO). Operating range is between 9V and 20V.
Gnd	2	This pin is ground of the IC.
Ctrl	3	This pin is connected to the feedback loop. The pin contains two functions. Between 1V and 1.5V it controls the on time (oscillator). Above a threshold of 3.5V it is possible to initiate Burst mode stand-by via a current pulse.
Demag	4	This pin is connected to the V_{CC} winding. The pin contains three functions. During magnetization the input voltage is sensed to compensate the OCP level for OPP (independent of input voltage). During demagnetization the output voltage is sensed for OVP and a comparator is used to prevent continuos conduction mode when the output is overloaded.
Sense	5	This pin contains four different functions. Soft start, frequency reduction and protection levels OCP (OPP) and SWP. By connecting an R_{SS} and C_{SS} between the sense resistor and this pin it is possible create a Soft start. The frequency is reduced starting from a level of 75mV until 50mV where the frequency is equal to the minimum frequency of the oscillator (6kHz). Two different protection levels of 0.5V(this OCP level depends on the Demag current) and 0.88V(fixed SWP level) are implemented.
Driver	6	This pin will drive the switch (MOSFET). The driver is capable of sourcing and sinking a current of respectively 125mA and 540mA.
HVS	7	This is a High Voltage Spacer (keep this pin floating)
Drain	8	This pin is connected to the drain of the switch or center-tap of the transformer depending on the voltage (BV_{DSS} = 650V). The pin contains three functions. The Mlevel that enables the controller between 60V and 100Vinput voltage, supply the start-up current and valley detection for zero/low voltage switching.

Table 3 Pin description

4. DESIGN OF 75W UNIVERSAL RANGE MONITOR SUPPLY (COOKBOOK)

4.1 Introduction to design

This monitor supply is designed for a low/mid end 17" monitor with a universal input voltage range. Because of this Quasi-Resonant typology it is possible to achieve a high efficiency (above 90%). Another important requirement is the power consumption during stand-by (<1W). Using the Burst mode stand-by of the controller it is possible to fulfil this requirement.

4.2 Supply specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input requirements						
V_{LINE}	line voltage	nominal operation	85		264	V_{AC}
f_{LINE}	line frequency	nominal operation	50		60	Hz
$P_{Burst\ mode}$	Burst mode power consumption	Burst mode, 5V@ 20mA and other outputs at no load			1	W
Output requirements						
185V	Deflection output	all conditions		185		V_{DC}
	line regulation	$85V_{AC}$-$264V_{AC}$			100	mV_{DC}
	load regulation	I_{out}=60mA – 300mA			100	mV_{DC}
	line freq. ripple	$85V_{AC}$, 405mA			200	mV_{pp}
	switching freq. ripple	$85V_{AC}$, 405mA			20	mV_{pp}
	overshoot/undershoot	I_{out}=54mA–405mA visa versa			±1	V_p
	output current				300	mA
80V	Video output					V_{DC}
	output current				100	mA
16V	Base-drive output			16		V_{DC}
	output current			20		mA
12V	12V output(linear regulator)			12		V_{DC}
	output current			400		mA
±10V	vertical deflection output, cathode heater			±10		V_{DC}
	output current			0.9		A
5V	micro controller(linear regulator)			5		V_{DC}
	output current			20		mA
Miscellaneous						
η	efficiency	V_{LINE} = 110Vac and 230Vac, P_{OUT} = 75W		90		%

Table 4 Supply specification

4.3 Numeric calculations of reference design

4.3.1 Dimensioning the key components

This chapter could be used as a guide line to calculate the large signal components of the Quasi-Resonant converter including the primary transformer inductance L_P the resonance capacitor C_D and the sense resistor. This design strategy is used to design a monitor supply (see circuit diagram Figure Figure 12, page 26). It will be clear that the strategy differs in each application depending on costs, volume, efficiency etc.

Calculating the transformer inductance L_P and the resonance capacitor C_D two important requirements are used:
- Universal input range $85V_{AC}$…$264V_{AC}$;
- Operating power range 20W…$85W_{peak}$.

In normal operation, when the deflection circuit of a Monitor is enabled, there will be a certain amount of power consumption varying between 20W and $85W_{peak}$. Due to efficiency reasons the converter has to operate in the Quasi-Resonant mode within this power range, which makes it possible to achieve efficiency up to 90%.
There are also some other choices and criteria that have to be taken care of before starting the design. These choices strongly depend on the application as mentioned before.
- No peak clamp to limit the maximum voltage across the switch. Minimize component count and improve efficiency;
- maximum voltage across the power MOSFET (V_{D_MAX}, including ΔV caused by leakage inductance L_s) which defines maximum turns ratio n;
- f_{MIN} = 25kHz and f_{MAX} = 150kHz. The choice of f_{MIN} determines the transformer size and f_{MAX} is restricted by the maximum frequency of the controller.

Some additional requirements should be taken into account:
- dV/dt drain source < 4kV/us (EMI reduction)
- Maximum permitted on-time < 50us (t-on_{max} = 50us fixed by IC)

Eventually there are five different parameters to design:
- Turns ratio n;
- Primary inductance L_P and resonance capacitor C_D;
- Volt/turn to get the required voltages at the output;
- Core size (A_{eff} effective core surface).

In the following description the parameters are defined step by step.

Step 1 Maximum turns ratio n
The turns ratio should be as large as possible to get zero voltage switching also at high input voltages. This will reduce the switching losses of the MOSFET. However the turns ratio is restricted by the choice of the breakdown voltage of the MOSFET. In this case an 800V MOSFET is chosen because of the wide input voltage range (85Vac – 264Vac) and an additional spike caused by the leakage inductance of the transformer (no peak clamp is used). This means that the maximum drain voltage should be lower than 800V including the voltage caused by the leakage inductance L_S. The maximum drain source voltage is equal to:

$$V_{D\_MAX} = V_{IN\_MAX} + n \cdot (V_{OUT} + V_F) + \Delta V \qquad \text{Equation 6}$$

Where ΔV (caused by the leakage inductance) is estimated by:

$$\Delta V = I_{L\_peak} \cdot \sqrt{\frac{L_S}{C_D}} \qquad \text{Equation 7}$$

Where,
I_{L_peak} = peak inductor current (at maximum input voltage)
L_S = leakage inductance
C_D = total drain capacitance

Without a peak clamp ΔV depends on the leakage inductance, the total capacitance on the drain node (C_R and parasitic capacitance's C_{OSS}, C_W) and the primary peak current just before switch-off. These parameters are not known yet but assuming the ΔV would be 125V and substituting V_{IN_MAX} = 264√2V, V_{OUT} = 185V and V_F = 0.7V gives a maximum turns ratio of:

$$n \le \frac{V_{DS\_MAX} - V_{IN\_MAX} - \Delta V}{(V_{OUT} + V_F)} = \frac{800 - 264 \cdot \sqrt{2} - 125}{185.7} \le 1.62 \qquad \text{Equation 8}$$

Choosing the maximum turns ratio close to this value of 1.62 will give minimum switch-on losses at high input voltages. But keep in mind that the value of the ΔV should be checked afterward because this depends on the transformer construction (leakage inductance).

Step 2 calculating primary inductance L_P and resonance capacitor C_D

To simplify the formulas the commutation time is neglected and the dead time is assumed to be constant, which is not the case when $V_{IN} < n \cdot V_{OUT}$ (see APPENDIX 2, page 40). Now L_P and C_D can be calculated by the following formulas.

$$L_P = \frac{\left(\frac{1}{f_{MIN}} - \frac{1}{f_{MAX}}\right)^2}{\left[\sqrt{2 \cdot \frac{P_{OUT\_MAX}}{\eta} \cdot \frac{1}{f_{MIN}}} \cdot \left(\frac{1}{V_{IN\_MIN}} + \frac{1}{n \cdot V_{OUT}}\right) - \sqrt{2 \cdot \frac{P_{OUT\_MIN}}{\eta} \cdot \frac{1}{f_{MAX}}} \cdot \left(\frac{1}{V_{IN\_MAX}} + \frac{1}{n \cdot V_{OUT}}\right)\right]^2}$$

$$C_D = t_{DEAD}{}^2 \cdot \frac{1}{\pi^2 \cdot L_P} \qquad \text{Equation 9}$$

Where t_{DEAD} is equal to:

$$t_{DEAD} = \frac{1}{f_{MIN}} - L_P \cdot \sqrt{\frac{2 \cdot P_{OUT\_MAX}}{\eta \cdot L_P \cdot f_{MIN}}} \cdot \left(\frac{1}{V_{IN\_MIN}} + \frac{1}{n \cdot V_{OUT}}\right)$$

Substituting two different points P1 and P2 in the above formulas:
P1: f_{MIN} = 25kHz @V_{IN_MIN} = 100V_{DC}, P_{OUT_MAX} = 85W
P2: f_{MAX} = 150kHz @V_{IN_MAX} = 373V_{DC}, P_{OUT_MIN} = 20W
This gives an L_P = 1mH and C_D = 1.17nF. In practice the capacitor also consist out of a parasitic part (e.g. C_{OSS} and C_W). Because of this an actual capacitor value of 1nF is used.

Note:
Keep in mind that the main reason for placing the resonant capacitor is to limit the **switch-off losses** and to reduce the dV/dt for EMI reasons. When using the formulas above and choosing a small frequency range (f_{MIN}…f_{MAX}) it

may end up in a large capacitor value, which will result in higher **switch-on** losses (at high input voltage). In this case it is recommended to make another choice for the frequency range or the value of P_{MIN}.
The graphic below shows the frequency as function of P_{OUT} at $V_{IN\ MAX}$ = 373V_{DC} and $V_{IN\ MIN}$ = 100V_{DC}.

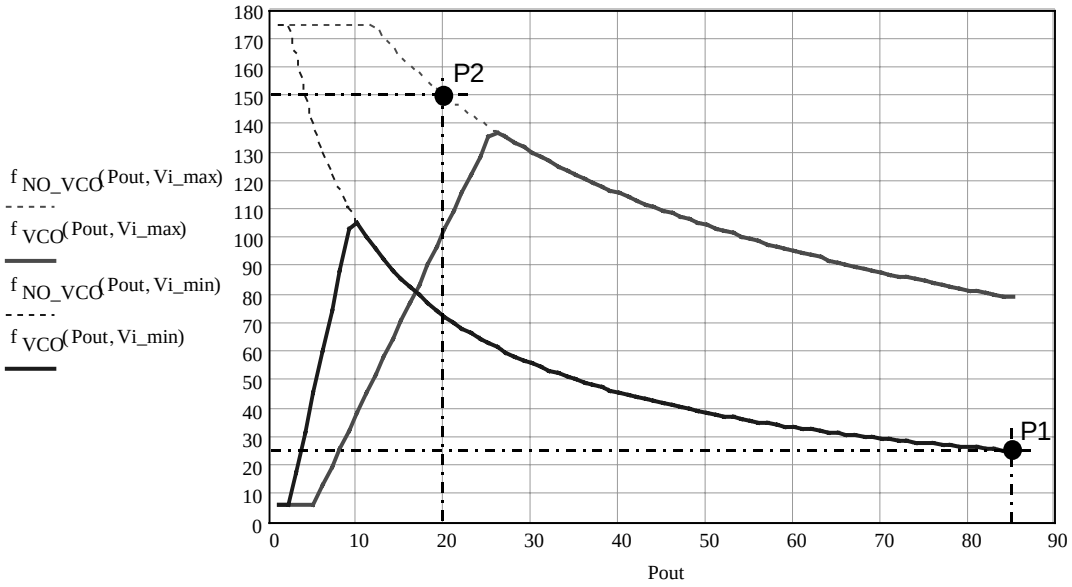

Figure 11 Calculated frequency characteristics

In practice the frequency will deviate from the calculated frequency especially at low output powers. This can be explained because the commutation time (t_{COM}) between magnetization and demagnetization is neglected and the dead time is assumed to be constant in the calculations.

step 3 defining secondary voltage/turn

The following output voltages are required: 185Vmain output, 80V, 16V and ±10V. Because the leakage inductance increases with the number of layers it is recommended to select the voltage per turn as large as possible to reduce the number of turns. Assuming N_S = 34 secondary turns for the main output gives 5.46V per turn (185.7V divided by 34 turns). In this case the other outputs requires respectively fifteen turns for the 80Voutput, three turns for the 16V output, V_{CC} winding and two turns for the 10V output.

step 4 defining primary number of turns N_P

The primary number of turns N_P is equal to:

$$N_P = n \cdot N_S$$
$$N_P = 1.62 \cdot 34 \approx 55$$

Equation 10

Sense resistor

The sense resistor in series with the MOSFET limits the maximum inductor peak current. The inductor peak current is calculated by:

$$I_{L\_peak} = 2 \cdot \frac{P_{OUT}}{\eta} \cdot \frac{n \cdot V_{OUT} + V_{IN}}{n \cdot V_{OUT} \cdot V_{IN} \cdot \left(1 - \pi \cdot \sqrt{L_P \cdot C_D} \cdot f\right)}$$

Equation 11

Limiting the output power to 90W and substituting η = 0.9, n·V_{OUT} = 300.5V, V_{IN} = 100V, L_P = 1mH, C_D = 1.17nF and f = 23.8kHz gives an primary peak current of 2.9A

Now the sense resistor can be calculated by:

$$R_{SENSE} = \frac{V_{OCP}}{I_{L\_peak}}$$ Equation 12

Where,
V_{OCP} = the Over Current Protection level (fixed at 0.5V @ $I_{(opp)(demag)}$ >-24µA)

Substituting V_{OCP} = 0.5V and I_{L_peak} = 2.9A gives a sense resistor of 172mΩ (two resistors of 330mΩ in parallel gives a maximum primary peak current I_{L_peak} = 3.03A @ V_{IN} = 100V). It is recommended to use low inductive current sense resistors preventing noise at the Sense pin.

Step 5 Selecting the core size

The peak flux density in the transformer can be calculated by the following equation:

$$B_{peak} = \frac{L_P \cdot I_{L\_peak}}{N_P \cdot A_{MIN}}$$ Equation 13

Where,
L_P = primary inductance
I_{L_peak} = primary peak current set by the OCP level
N_p = primary number of turns
A_{MIN} = minimum core area

The saturation flux density of a ferrite core (Philips 3C85) is equal to 330mT at 100°C. Substituting the previous calculated L_P, I_{L_peak} and N_P will give the minimum required core area.

$$A_{MIN} \geq \frac{L_P \cdot I_{L\_peak}}{B_{sat} \cdot N_P} \geq \frac{1 \cdot 10^{-3} \cdot 3.03}{330 \cdot 10^{-3} \cdot 55} \geq 167 mm^2$$ Equation 14

E42/21/15 core can meet this requirement. The core parameters of the E42 are:

SYMBOL	PARAMETER	VALUE	UNIT
Ve	effective volume	17300	mm^3
Ae	effective area	178	mm^2
A_{min}	minimum area	175	mm^2

Table 5 Core parameters

APPENDIX 3 shows an overview of the transformer data.
The core area is mainly defined by the minimum switching frequency f_{MIN} that is chosen before.
When the core size should be reduced it is recommended to increase the minimum switching frequency and calculate the new values for L_P and C_D.

Recommendation for the transformer construction:

The maximum drain source voltage is proportional to the leakage inductance L_S, which is modelled as an inductance in series with the primary inductance. This will cause an additional voltage spike across the MOSFET. Because of this it is necessary to minimize the leakage inductance. A layer transformer is a good choice regarding a low leakage inductance. Using a sandwich construction, where the primary winding is split into two windings with the secondary positioned between those two, will reduce the leakage inductance even more.

Another recommendation with respect to the transformer construction is to put the primary winding, which is connected to the drain of the MOSFET, at the inner side. In this case the other windings work as a shielding for E-field generated by this winding.

4.3.2 Protections

The OVP level is set by the resistor between the V_{CC} winding and de Demag pin.

$$R_{OVP} = \frac{\left(\frac{N_{Vcc}}{N_S} \cdot OVP\right) - V_{clamp,demag(positive)}}{I_{(ovp)(demag)}}$$ Equation 15

Substituting an OVP level of 200V gives a resistor value of 280kΩ.

$$R_{OVP} = \frac{\left(\frac{3}{34} \cdot 200\right) - 0.7}{60\mu} \approx 280k\Omega = R_{18}$$

The Over Power Protection level is set by the negative current going into the Demag pin. The OVP and OPP protections are separated by means of a diode in series with R_{17}. The forward voltage drop (V_F) of this diode is also taken into account when calculating R17.

$$R_{17} = \frac{\left(\frac{N_{Vcc}}{N_P} \cdot V_{IN(\min)}\right) + V_{clamp,demag(negative)} - V_F}{I_{(opp)(demag)} - \frac{\left(\frac{N_{Vcc}}{N_P} \cdot V_{IN(\min)}\right) + V_{clamp,demag(negative)}}{R_{18}}}$$ Equation 16

Substituting a minimum input voltage of 100V and a V_D = 0.6V will give the following resistor value:

$$R_{OPP} = \frac{\left(\frac{3}{55} \cdot 100\right) - 0.25 - 0.6}{24\mu - \frac{\left(\frac{3}{55} \cdot 100\right) - 0.25}{280k}} \approx 820k\Omega$$

4.3.3 Burst mode stand-by

Burst mode is implemented because the specification requires an input power below 1W during Stand-by. In this Monitor application it was necessary to reduce the unused output voltages because some of these outputs are still loaded for example the cathode heater of the CRT (Cathode Ray Tube) that is attached to the –10V output. A thyristor (D4) connects the higher output voltage winding (see schematic) to output that feeds the µC (in front of 5V linear stabilizer). Because of this bypass all the other output voltages are reduced depending on the turns ratio between the secondary windings. For example the –10V is reduced to about –1.3V.

$$V_{-10V} = \frac{N_{-10V}}{N_{80V}} \cdot V_{STAB} = \frac{2}{15} \cdot 10 \approx -1.3V$$

The thyristor is activated by an external signal (e.g. DPMS signal from μC or S_1 on the demo board). Once the thyristor is closed the voltage at the stabilizer will rise. When the voltage exceeds the zener voltage of Z_2 (and forward voltage drop of both D_{19}, TR_4) the transistor TR_5 is turned on to generate the current pulse to switch-off the IC. R_{33} limits the current through the opto coupler and C_{28}, R_{25} are used as feed forward to get a steep pulse. Via the opto coupler this current pulse will enter the Ctrl pin, which will activate the Burst mode stand-by. The minimum pulse width is defined by the blanking time of 30μs that prevents false triggering due to spikes. The amplitude should be larger then 16mA. The driver is immediately disabled and the controller will enter the Safe-Restart mode. Burst mode operation will continue until the DPMS signal is removed.

4.4 Circuit diagram

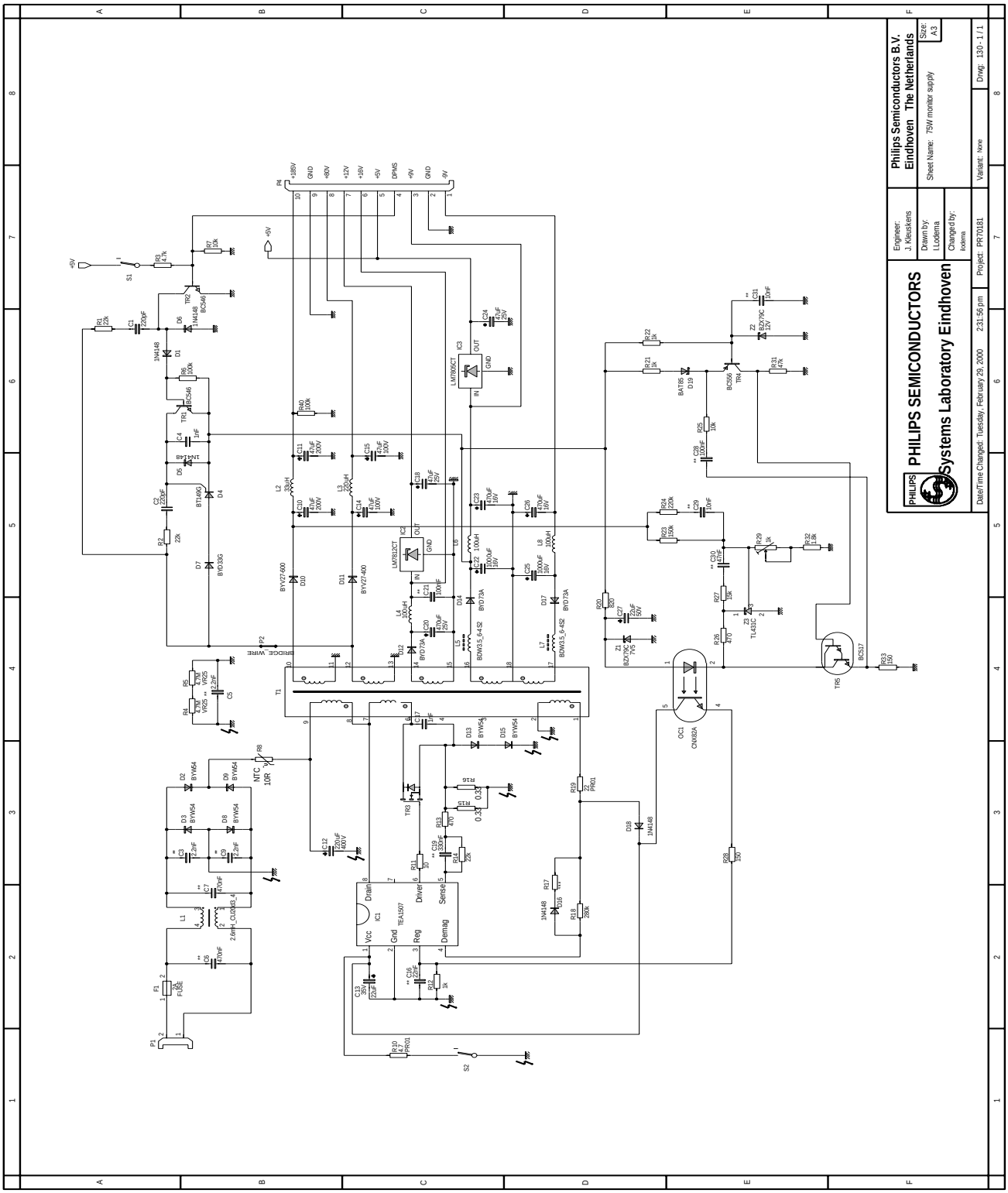

Figure 12 Circuit diagram

4.5 PCB design

4.5.1 Layout considerations

Some important points for a proper layout are reminded below (see also Figure 13):

- At primary side, keep large signal and small signal separated;
- Put a resistor in series with the soft start capacitor to prevent EMI distortion;
- Keep the area and the length of the drain track(high alternating voltages) as small as possible to prevent noise coupling with high impedance inputs (sense pin, Ctrl pin, Demag pin);
- Noise can be reduced by minimising the area of the current loops (e.g. 1 and 2) with fast alternating currents;
- Do not use a floating heatsink, but connect the heatsink directly or via a capacitor to the primary GND. Use the heat sink as EMI shield between the small signal and large signal part;
- Connect Cy, between primary GND and secondary GND, with a short track to the primary buffer capacitor. **Prevent a common GND with the controller!!**

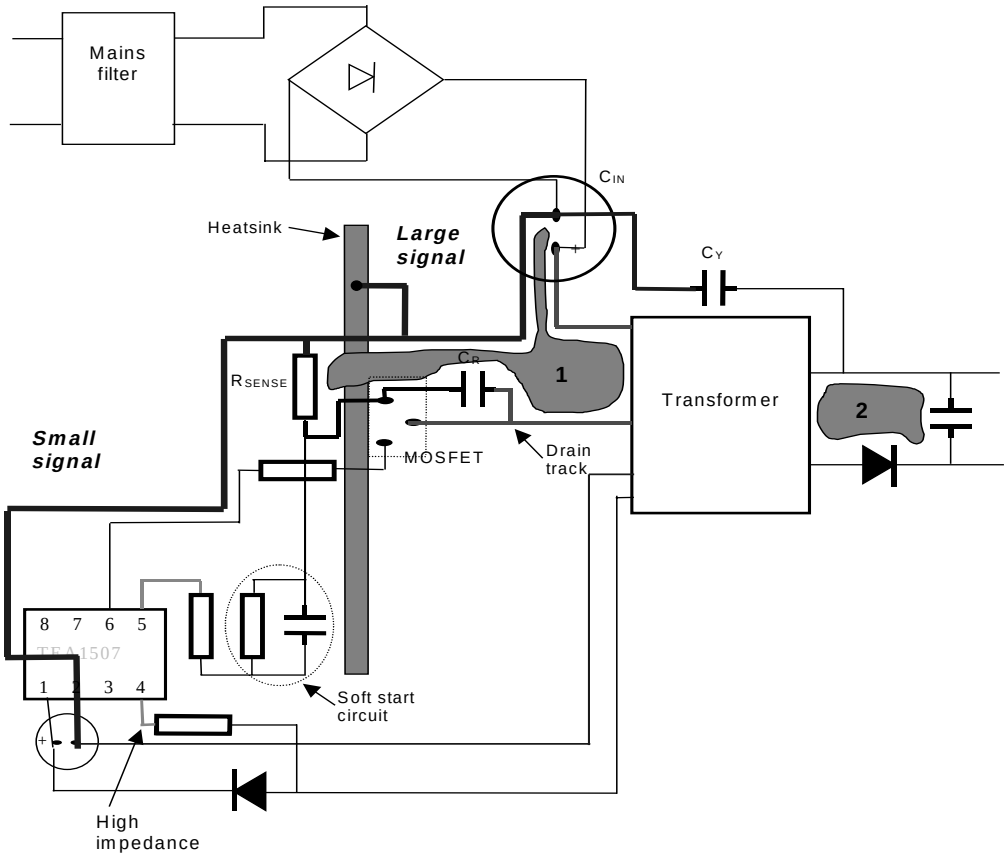

Figure 13 Layout considerations

4.5.2 PCB layout

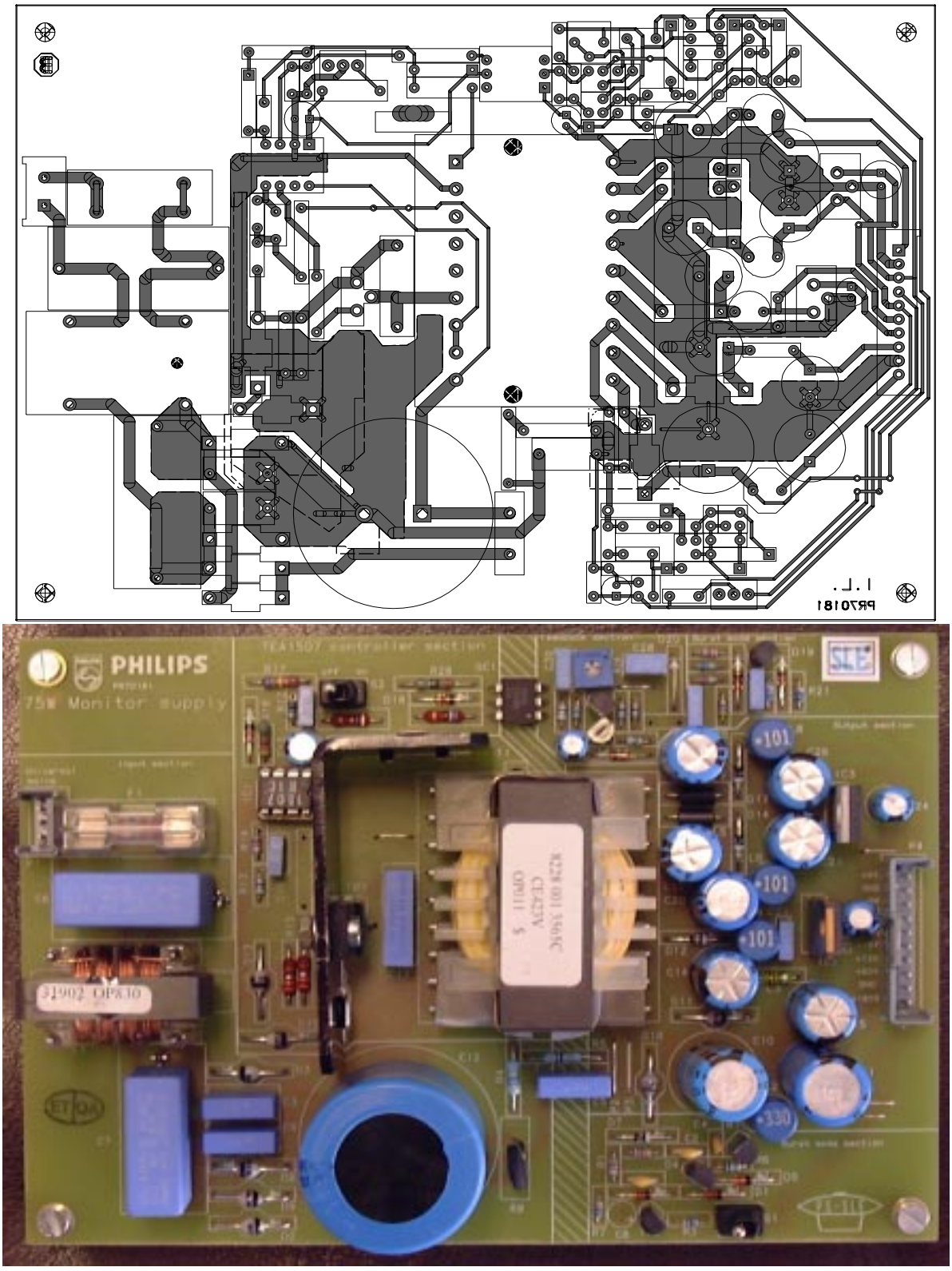

Figure 14 PCB layout

4.5.3 Parts list

REFERENCE	VALUE	TYPE	PACKAGE	12NC
Capacitors				
C1	220pF		CER2_1	2222-655-03221
C2	220pF		CER2_1	2222-655-03221
C3	2.2nF	MKP3366 (Y2)	C_B6_L12.5_P10mm	2222-336-60222
C4	1nF		CER1_1	2222-630-02102
C5	2.2nF	MKP3366 (Y2)	C_B6_L12.5_P10mm	2222-336-60222
C6	470nF	MKP336 (X2)	C_B15_L31_P27mm5	2222-336-10474
C7	470nF	MKP336 (X2)	C_B15_L31_P27mm5	2222-336-10474
C9	2.2nF	MKP3366 (Y2)	C_B6_L12.5_P10mm	2222-336-60222
C10	47uF	KO151	CASE_R18	2222-151-62479
C11	47uF	KO151	CASE_R18	2222-151-62479
C12	220uF	057 PSM-SI	CASE_3050	2222-057-36221
C13	22uF	037 RSM	CASE_R55_CA	2222-134-50229
C14	47uF	037 RSM	CASE_R16	2222-037-69479
C15	47uF	037 RSM	CASE_R16	2222-037-69479
C16	22nF	MKT 370	C370_A	2222-370-21223
C17	1nF	KP/MMKP376	C_B6_L18.5_P15mm	2222-375-44102
C18	47uF	097 RLP	CASE_R11_m	2222-037-56479
C19	330nF	MKT 370	C370_B	2222-370-11334
C20	470uF	136 RVI	CASE_R16	2222-136-66471
C21	100nF	MKT 370	C370_A	2222-370-11104
C22	1000uF	037 RSM	CASE_R16	2222-037-65102
C23	470uF	037 RSM	CASE_R14	2222-037-65471
C24	47uF	037 RSM	CASE_R74_m	2222-097-56479
C25	1000uF	037 RSM	CASE_R16	2222-037-65102
C26	470uF	037 RSM	CASE_R14	2222-037-65471
C27	22uF	037 RSM	CASE_R11_m	2222-037-90056
C28	100nF	MKT 370	C370_B	2222-370-21104
C29	10nF	MKT 370	C_B2.5_L7.2_P5mm08	2222-370-41103
C30	47nF	MKT 370	C370_A	2222-370-21473
C31	10nF	MKT 370	C_B2.5_L7.2_P5mm08	2222-370-76103
Diodes				
D1	1N4148	general purpose	SOD27	9330-839-90153
D2	BYW54	control. avalanche	SOD57	9333-636-10153
D3	BYW54	control. avalanche	SOD57	9333-636-10153
D4	BT149G	thyristor	TO92	9333-984-40112
D5	1N4148	general purpose	SOD27	9330-839-90153
D6	1N4148	general purpose	SOD27	9330-839-90153
D7	BYD33G	control. avalanche	SOD81	9337-234-10113
D8	BYW54	control. avalanche	SOD57	9333-636-10153
D9	BYW54	control. avalanche	SOD57	9333-636-10153
D10	BYV27-600	control. avalanche	SOD57	9340-418-70113
D11	BYV27-400	control. avalanche	SOD57	9340-366-90133
D12	BYD73A	control. avalanche	SOD81	9337-537-40163
D13	BYW54	control. avalanche	SOD57	9333-636-10153
D14	BYD73A	control. avalanche	SOD81	9337-537-40163
D15	BYW54	control. avalanche	SOD57	9333-636-10153
D16	1N4148	general purpose	SOD27	9330-839-90153
D17	BYD73A	control. avalanche	SOD81	9337-537-40163
D18	1N4148	general purpose	SOD27	9330-839-90153
D19	BAT85	shottky barrier	SOD68	9336-247-60112
Z1	BZX79C	zener	SOD27	9331-177-60153
Z2	BZX79C	zener	SOD27	9331-178-10153
Z3	TL431C	voltage regulator	TO226AA	TL431C
IC's				
IC1	TEA1507	PWM controller	SOT97_s	DIL8
IC2	LM7812CT	linear stabilizer	TO220_vc	PN-LM7812CT
IC3	LM7805CT	linear stabilizer	TO220_vc	PN-LM7805CT
OC1	CNX82A	Opto-coupler	SOT231	9338-846-80127
Magnetics				
L1	2.6mH CU20d3_4	common mode choke	CU20d3	3112-338-32441
L2	33uH	Choke	TSL0707_2e	TSL0709-33K1R9

L3	220uH	Choke	uChoke_3e	LAL03NA221K
L4	100uH	Choke	TSL0707_5mm0	TSL0709-101KR66
L5	BDW3.5_6-4S2	ferrite bead		4330-030-38741
L6	100uH	Choke	TSL0707_5mm0	TSL0709-101KR66
L7	BDW3.5_6-4S2	ferrite bead		4330-030-38741
L8	100uH	Choke	TSL0707_5mm0	TSL0709-101KR66
T1	1000uH	CE422v SMPS transformer		8228-001-32811
Resistors				
R1	22k	SFR16T		2322-180-73223
R2	22k	SFR16T		2322-180-73223
R3	4.7k	SFR16T		2322-180-73472
R4	4.7M	VR25		2322-241-13475
R5	4.7M	VR25		2322-241-13475
R6	100k	SFR16T		2322-180-73104
R7	10k	SFR16T		2322-180-73103
R8	10	NTC		2322-594-XXXXX
R10	4.7	PR01		2322-193-13478
R11	10	SFR16T		2322-180-73109
R12	1k	SFR16T		2322-180-73102
R13	470	SFR16T		2322-180-73471
R14	22k	SFR16T		2322-180-73223
R15	0.33	SFR25H		RES-186-SFR25H
R16	0.33	SFR25H		RES-186-SFR25H
R17	820k	SFR16T		2322-180-73105
R18	280k	SFR16		2322-187-53284
R19	22	PR01		2322-193-13229
R20	820	SFR16T		2322-180-73821
R21	1k	SFR16T		2322-180-73102
R22	1k	SFR16T		2322-180-73102
R23	150k	SFR16T		2322-180-73154
R24	220k	SFR16T		2322-180-73224
R25	2.2k	SFR16T		2322-180-73222
R26	470	SFR16T		2322-180-73471
R27	15k	SFR16T		2322-180-73153
R28	150	MRS25		2322-156-11501
R29	1k	SFR16T		2322-180-73821
R31	47k	SFR16T		2322-180-73473
R32	1.8k	SFR16T		2322-180-73182
R33	150	SFR16T		2322-180-73151
R40	100k	SFR16T		2322-180-73104
Miscellaneous				
F1	2A	fuse	GLAS_HOLDER	2412-086-28196
P1	MKS3730_2p_220V	connector (mains)		MKS3733-1-0-303
P4	MKS3730_10p	connector (output)		MKS3740-1-0-1010
S1		SPDT		FARNELL-150-559
S2		SPDT		FARNELL-150-559
Transistors				
TR1	BC546	general purpose	TO92	9332-055-20112
TR2	BC546	general purpose	TO92	9332-055-20112
TR3	STP7NB80FP	MOSFET	TO220	STP7NB80FP
TR4	BC556	general purpose	TO92	9332-055-40112
TR5	BC517	darlington	TO92	9335-671-30112

Table 6 Parts list

5. MAESUREMENTS

5.1 Static performance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Line regulation						
185V	Horizontal deflection, EHT	$85V_{AC}<V_{in}<264V_{AC}$, I = 405mA	185.00		185.01	V_{DC}
Load regulation						
185V	Horizontal deflection, EHT	$V_{line} = 110V_{AC}$ $60mA<I_{out\_185V}<300mA$, others unloaded	185.06		185.02	V_{DC}
Standby power consumption from line						
P_{stby}	Input power	$V_{LINE} = 230V_{RMS}$, 20mA @ 5V		980		mW

Table 7 Static performance

5.1.1 Switching frequency vs output power

Figure below shows the measured switching frequency as a function of output power at two different input voltages.

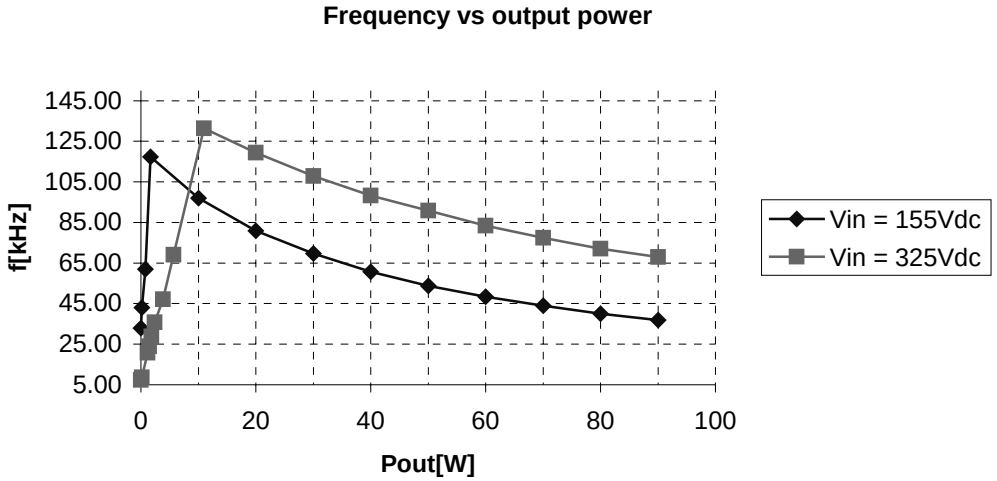

Figure 15 Measured frequency curve

Note: DC input voltage is applied during this measurement

5.1.2 Efficiency

The figure below shows the efficiency measured at two different input voltages respectively 110Vac and 230Vac. Both curves showing efficiency above 90% at a nominal output power of 75W. The efficiency stays even above 87% over the power range from 20W to 85W. Efficiency is a big advantage of the Quasi-Resonant Flyback converter compared to the Fixed Frequency Flyback converter.

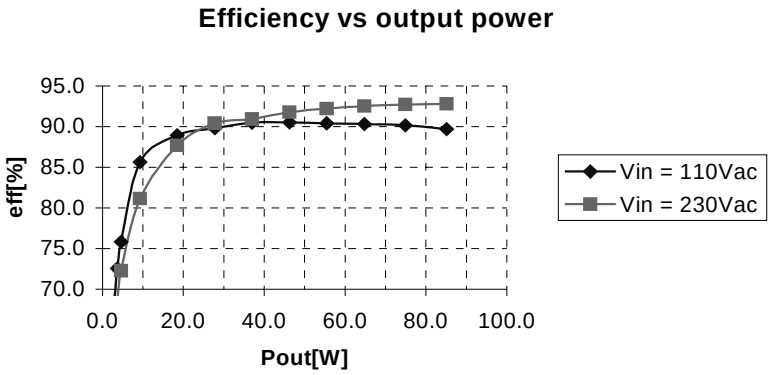

Figure 16 Measured efficiency

Note: Only the 185V output is loaded during this measurement

This high efficiency is mainly achieved because of the ZVS/LVS switching, which reduces the switch-on losses and makes it possible to use a non-dissipative dV/dt limiter (only a capacitor across the drain-source of the MOSFET).

5.1.3 Over Voltage Protection

To illustrate the accuracy of the Over Voltage Protection a measurement is done at different input voltage and at different output loads such that the ringing of the reflected output voltage will be different in each condition. As previous described the ringing of the reflected output voltage is integrated, which makes the Over Voltage Protection rather accurate. The diagram below shows the OVP level under different conditions.

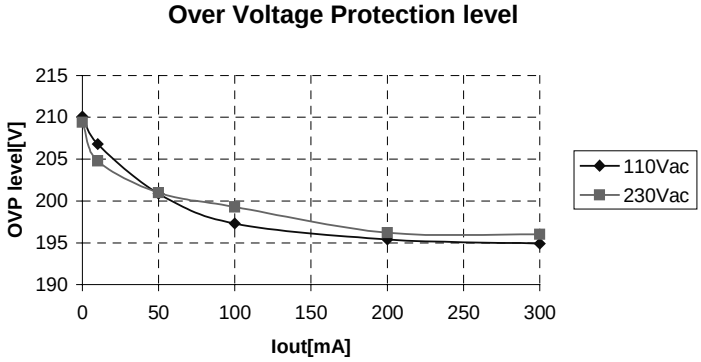

Figure 17 Measured OVP level

From this measurement it can be seen that the OVP level stays within 5% of the nominal value.

5.1.4 Over Power Protection

This internal OCP compensation is big advantage when using a Quasi-Resonant Flyback converter. Because of this compensation the maximum output stays almost equal independent of the input voltage. The diagram below shows the OPP level over the entire input voltage range.

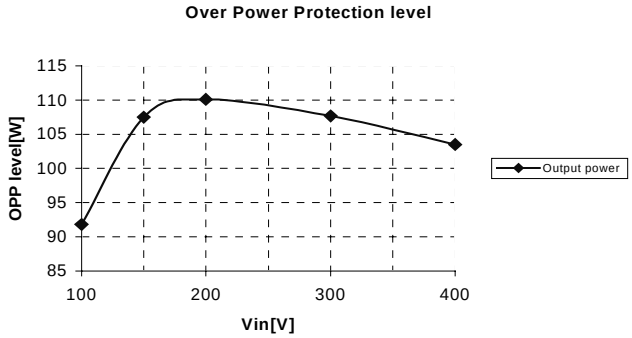

Figure 18 Measured OPP level

From this measurement it can be seen that the OPP level stays within 20% of the maximum value.

5.2 Dynamic performance

5.2.1 Start-up sequence

Figure 19 shows the waveforms during start-up. The Vcc capacitor is charged to $V_{(start)}$ and the driver is activated. In the meanwhile the voltage at the soft start capacitor C_{19} is charged to 0.5V. The peak current of the inductor will increase exponential which can be seen from the voltage (CH3) measured across the sense resistor. The OCP level, that depends on the input voltage, limits the maximum peak current. In this case the OCP level is close to 0.5V because this measurement is done at low input voltage (110Vac). After about 35 ms the output is in regulation and the peak current is reduced depending on the output power.

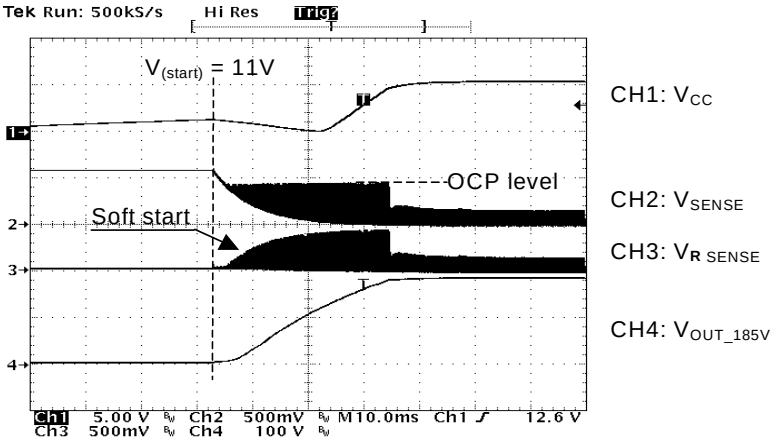

Figure 19 Start-up sequence

5.2.2 Load response

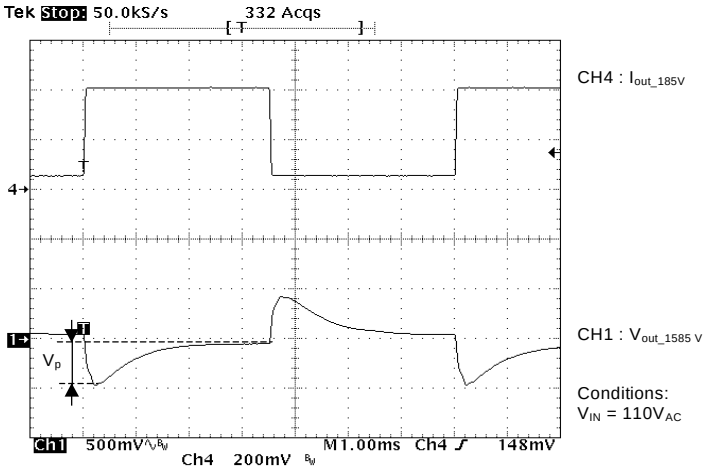

Figure 20 Load response

Figure 20 shows the response of the 185V deflection output when applying a load step. The load varies between 54mA (10W) and 405mA(75W). This is an even more severely load step than compared to a transition from black to full white screen in a monitor application. The overshoot is equal to V_P = 410mV. From this it can be concluded that the overshoot stays within the specification of ±1V of its nominal range.

5.2.3 Line and switching ripple

Figure 21 shows the line related AC ripple of the 185V output during minimum input voltage (worst case) and 75W output power. The output ripple is 90mV_{PP}. This is well within the specification of 200mV_{PP}.

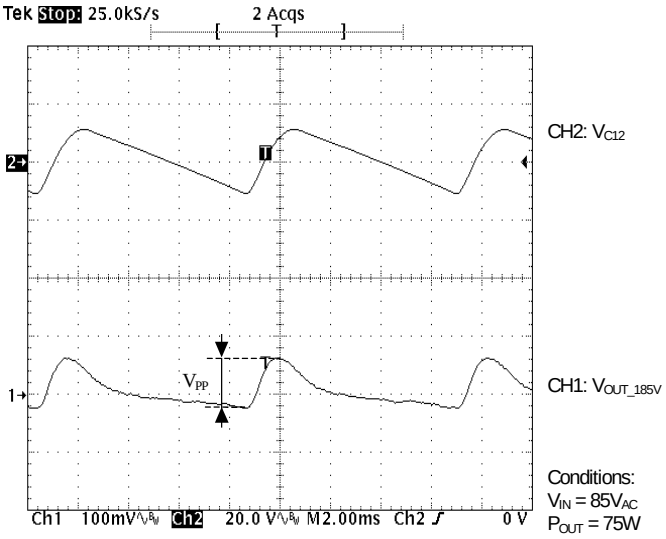

Figure 21 Line related ripple

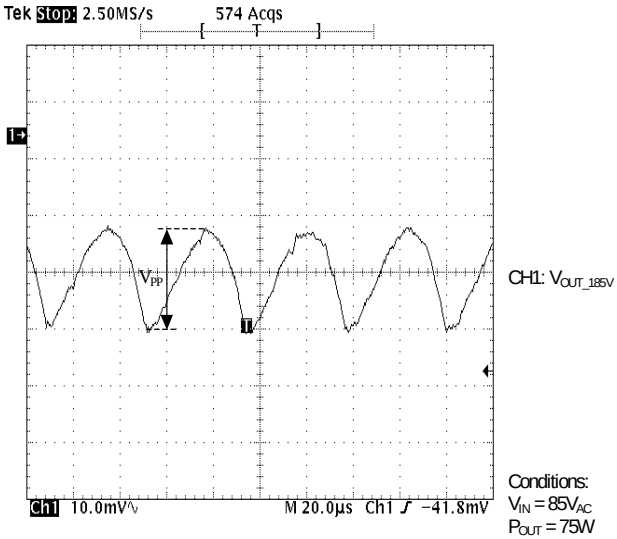

Figure 22 Switching ripple

Figure 22 shows the switching frequency related AC ripple of the 185V output at minimum input voltage (worst case) and 75W output power. The output ripple is 18mV_{PP}. This is within the specification of 20mV_{PP}.

5.2.4 Loop transfer function

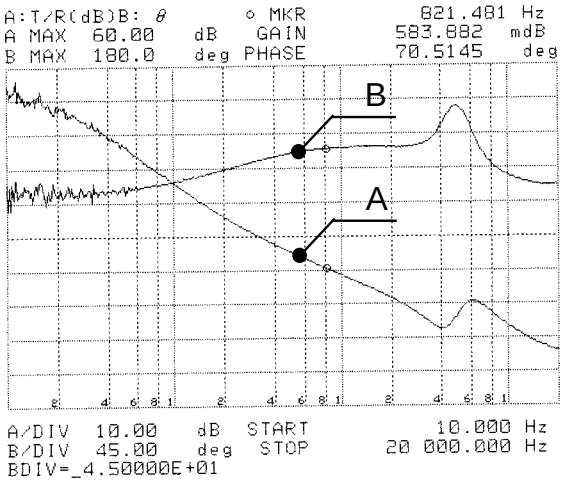

Figure 23 Bode plot

Figure 23 shows the bode plot of the measured loop transfer function including the Gain (trace A) and the Phase (trace B). This plot shows that the bandwidth is 820Hz and phase margin is 70 degrees at V_{LINE} = 110V_{AC} and P_{OUT} = 75W.

5.2.5 EMI results

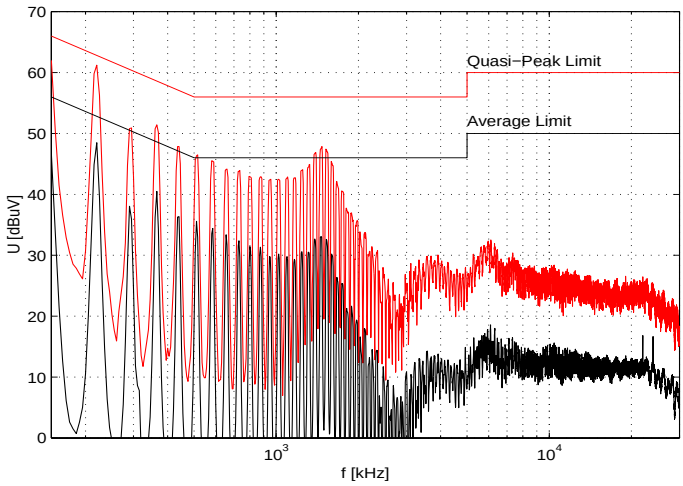

Figure 24 CISPR 13/22 measurement (150kHz-30MHz) @ Vin = 230Vac, nominal load

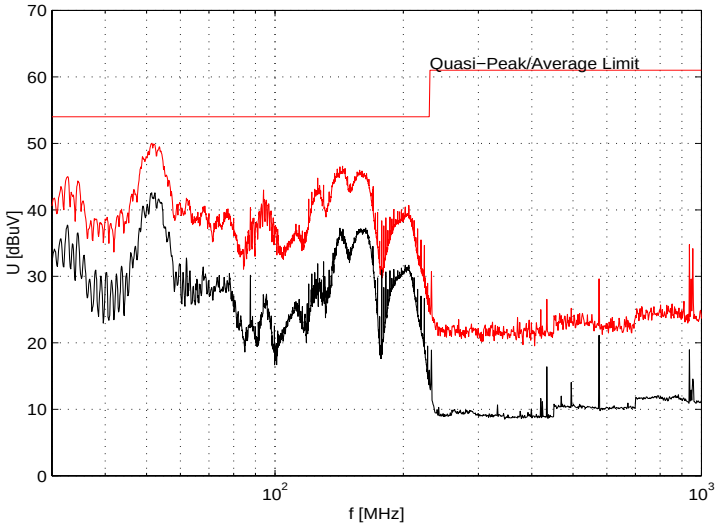

Figure 25 CISPR 13/22 measurement (30MHz-1GHz) @ Vin = 230Vac, nominal load

APPENDIX 1 LIST OF SYMBOLS

Symbol	Description
n	Transformer turns ratio
N_x	Number of turns
V_{LINE}	Line voltage
f_{LINE}	Line frequency
V_{IN}	Rectified line voltage
V_{OUT}	DC output voltage
I_{OUT}	DC output current
V_F	Diode forward voltage drop
V_{CC}	IC supply voltage
V_{OCP}	Over Current Protection level
CTR	Current Transfer Ratio
R_{SENSE}	Primary current sense resistor
$R_{DS(ON)}$	Drain-source on-resistance
C_D	Total drain node capacitance (including C_R, C_{OSS} and C_P)
C_R	Drain-source resonance capacitor
C_{OSS}	Parasitic MOSFET output capacitance
C_W	Parasitic transformer winding capacitance
V_D	Drain voltage
I_L	Inductor current
L_P	Primary transformer inductance
L_S	Leakage inductance
ZVS	Zero Voltage Switching
LVS	Low Voltage Switching

Table 8 List of symbols

APPENDIX 2 DETAILED PERIOD DESCRIPTION OF QR WAVEFORMS

The period can be divided into four time intervals, in chronological order:

Interval 1:	$t_0 < t < t_1$	primary stroke	$t_{PRIM} = t_1 - t_0$
Interval 2:	$t_1 < t < t_2$	commutation time	$t_{COM} = t_2 - t_1$
Interval 3:	$t_2 < t < t_3$	secondary stroke	$t_{SEC} = t_3 - t_2$
Interval 4:	$t_3 < t < t_{00}$	dead time	$t_{DEAD} = t_{00} - t_3$

Three situations of V_{IN} with regard to $n \cdot V_{OUT}$ has to be distinguished:

Situation	Drain voltage at switch-on
1] $V_{IN} = n \cdot V_{OUT}$	ZVS
2] $V_{IN} < n \cdot V_{OUT}$	ZVS
3] $V_{IN} > n \cdot V_{OUT}$	LVS

1] $V_{IN} = n \cdot V_{OUT}$

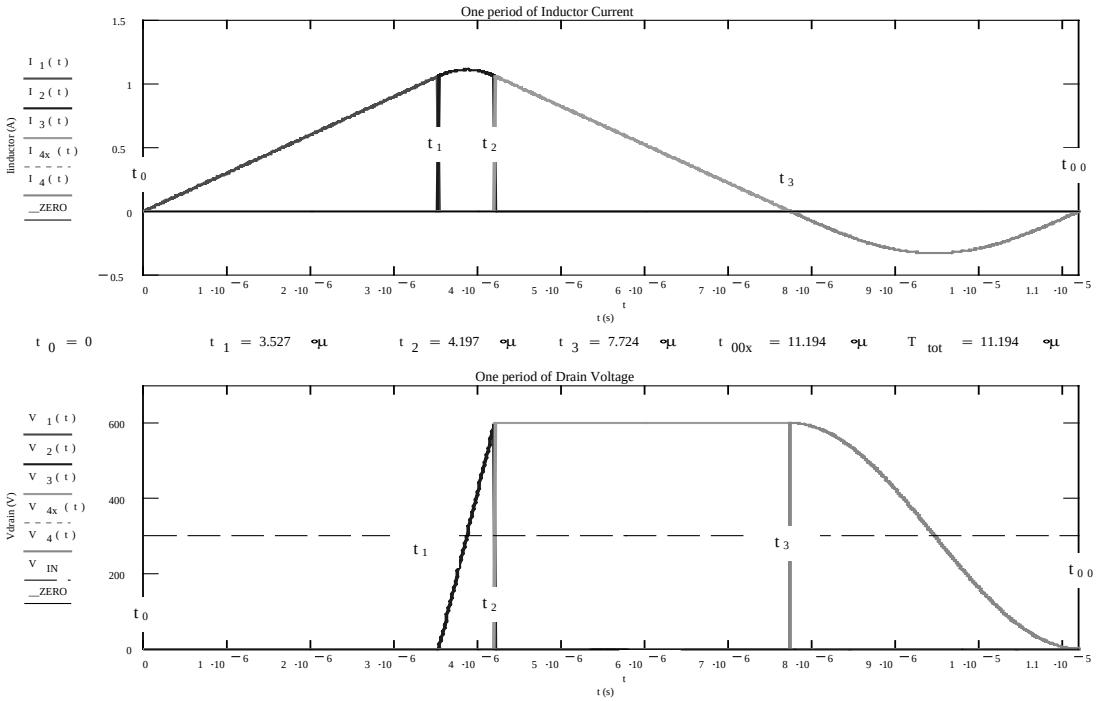

Figure 26 Waveforms $\mathbf{V_{IN} = n \cdot V_{OUT}}$

Interval 1: $t_0 \leq t < t_1$ *primary stroke:*

During this interval inductive current will be built up in the transformer, which is also called 'Magnetization' and/or primary stroke. End point t_{00} of the period is the start point of the new period t_0. As can be seen in Figure 26 the MOSFET is switched on at zero drain voltage called ZVS. The inductive current and drain voltage during this interval can be described by:

$$I_L(t) = \frac{V_{IN}}{L_P} \cdot (t - t_0) + I_L(t_0) \qquad \text{where } I_L(t_0) = 0 \text{ and } t_0 = 0$$

$$V_D(t) = I_L(t) \cdot (R_{SENSE} + R_{DS(ON)})$$

Equation 17

Interval 2: $t_1 \le t < t_2$ *commutation time* t_{COM}

At t = t_1 the MOSFET stops conduction. The energy in the inductor L_P is transferred to the resonance capacitor C_D. A resonance circuit of L_P and C_D is formed and during this interval the inductive current/voltage will follow a part of the L_PC_D-oscillation. The inductive current and drain voltage during this interval can be described by:

$$I_L(t) = V_{IN} \cdot \sqrt{\frac{C_D}{L_P}} \cdot \sin\{\omega(t-t_1)\} + I_L(t_1) \cdot \cos\{\omega(t-t_1)\} \quad \text{where: } \omega = \frac{1}{\sqrt{L_P \cdot C_D}}$$

$$V_D(t) = I_L(t_1) \cdot \sqrt{\frac{L_P}{C_D}} \cdot \sin\{\omega(t-t_1)\} - V_{IN}(t_1) \cdot \cos\{\omega(t-t_1)\}$$

Equation 18

The inductive current needs this interval to alter its positive derivative, equal to V_{IN}/L_P, to the negative derivative, equal to $-n \cdot V_{OUT}/L_P$, with which the transformer in the next interval will be demagnetized. This interval does not belong to the Magnetization or Demagnetization part, so it can be considered as a commutation time, which is called t_{COM}, between the primary and secondary stroke.

t_{COM} can be approached by:

$$t_{COM} = \frac{C_D \cdot (V_{IN} + n \cdot V_{OUT})}{I_L(t_1)}$$

Equation 19

Interval 3: $t_2 \le t < t_3$ *secondary stroke*

During this interval (primary) inductive energy will be transferred to the output. The diode starts conducting and the inductive current will be decreased, which is also called 'Demagnetization' At t_3 the transformer is completely demagnetized, for that reason this point is called Demag. The inductive current and drain voltage during this interval can be described by:

$$I_L(t) = -\frac{n \cdot V_{OUT}}{L_P} \cdot (t - t_2) + I_L(t_2)$$

$$V_D(t) = V_{IN} + n \cdot V_{OUT}$$

Equation 20

In practice the leakage inductance (L_s) will cause an oscillation together with the resonance capacitor C_D. The resulting oscillation current and voltage must be add to respectively the inductive current and drain voltage. This phenomenon is beyond the scope of this waveform explanation and is neglected for that reason.

Interval 4: $t_3 \le t < t_{00}$ *dead time* t_{DEAD}

At t_3 = Demag all energy has been delivered to the load, so the diode stops conducting. Again a resonance circuit of L_P and C_D is formed.

The controller measures the derivative of the drain voltage. When at t_{00} after a negative slope the derivative will become zero, what occurs in the valley, the MOSFET will be switch-on again.

$$VALLEY = derivative\ drain\ voltage\ zero: \frac{dV_D}{dt} = 0$$

The inductive current and drain voltage during this interval can be described by:

$$I_L(t) = -n \cdot V_{OUT} \cdot \sqrt{\frac{C_D}{L_P}} \cdot \sin\{\omega(t - t_3)$$

$$V_D(t) = V_{IN} + n \cdot V_{OUT} \cdot \cos\{\omega(t - t_3)$$

Equation 21

The actually dead time is almost constant and can be calculated by:

$$t_{DEAD} = \pi \cdot \sqrt{L_P \cdot C_D}$$

New period Interval 1:
Time t_{00} will be t_0 in the next period

$$at\ t_{00}\quad \frac{dI_L}{dt} = \frac{n \cdot V_{OUT}}{L_P} \qquad at\ t_0\quad \frac{dI_L}{dt} = \frac{V_{IN}}{L_P} \qquad \text{Equation 22}$$

The derivatives of the inductive current at the end of interval 4 is not equal to that of the begin of interval 1. Because of that a discontinuity (of the slope) in the current waveform occurs.

2] $V_{IN} < n \cdot V_{OUT}$

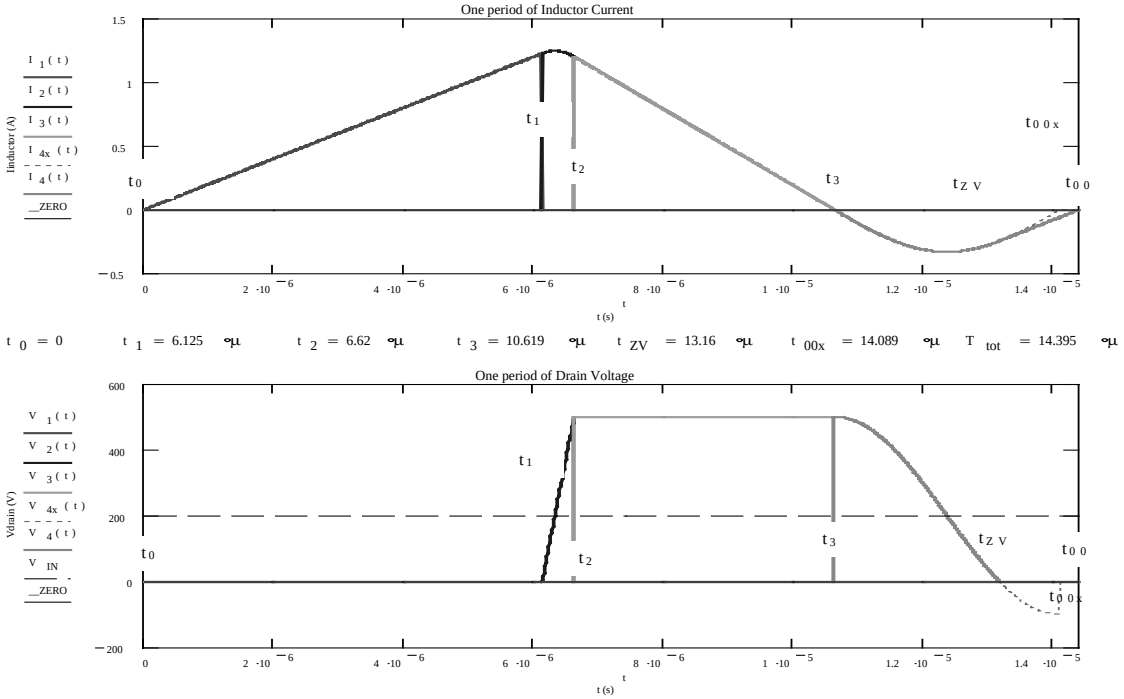

Figure 27 Waveforms $V_{IN} < n \cdot V_{OUT}$

The description of the period is mainly the same as the previous condition when $V_{IN} = n \cdot V_{OUT}$. The inductive current and drain voltage during of the intervals-1, -2 and –3 can be described with the same formulas. The main difference is the voltage/current description of interval-4 and the longer t_{DEAD} in this situation.

Interval 4: $t_3 < t < t_{00}$ *dead time* t_{DEAD}
The current and voltage will follow a part of the oscillation again of L_P and C_D. The drain voltage 'wants' to cross zero level but this is avoided by the anti parallel body diode of the MOSFET. When the drain voltage goes negative the internal MOSFET diode start to conduct en the drain voltage will remain on minus forward diode voltage till the MOSFET is switched on.
The derivative of the drain voltage is still measured by the controller. When at t_{ZV} after a negative slope the derivative has been become zero due to the clamping of the diode, the controller is judging it as sensing a valley, so the MOSFET will be switch-on again.
The forward voltage of the internal body diode is neglected, so drain voltage is assumed to be zero. In this situation interval-4 can be divided into two subintervals. The inductive current and drain voltage during this interval can be described by:

Subinterval-4a: $t_3 \leq t < t_{ZV}$

$$I_L(t) = -n \cdot V_{OUT} \cdot \sqrt{\frac{C_D}{L_P}} \cdot \sin\{\omega(t - t_3)$$

$$V_D(t) = V_{IN} + n \cdot V_{OUT} \cdot \cos\{\omega(t - t_3)$$

Equation 23

Subinterval-4b: $t_{ZV} \leq t < t_{00}$

$$I_L(t) = \frac{V_{IN}}{L_P} \cdot (t - t_{ZV}) + I_L(t_{ZV})$$

$$V_D(t) = 0 \quad \text{and so} \quad \frac{dV_D}{dt} = 0$$

$$\frac{dI_L}{dt} = \frac{n \cdot V_{OUT}}{L_P}$$

Equation 24

As can be seen in Figure 27 the MOSFET is switched on at t_{ZV} , where the drain voltage is zero. The MOSFET will first conduct the negative current, with derivative V_{IN}/L_P. From t_{ZV} until t_{00} there is no energy stored in the transformer that will be transferred to the output. The result of this is that the dead time is slightly longer compared to the previous situation. This means also that there is no direct relation anymore between the on time (=width gate pulse) and the energy that is transferred to the output.
In all three situations $T_{tot}=t_{00}$. In this situation t_{00x} represents the value of t_{00} if there was no 'head bumping'.

3] $V_{IN} > n \cdot V_{OUT}$

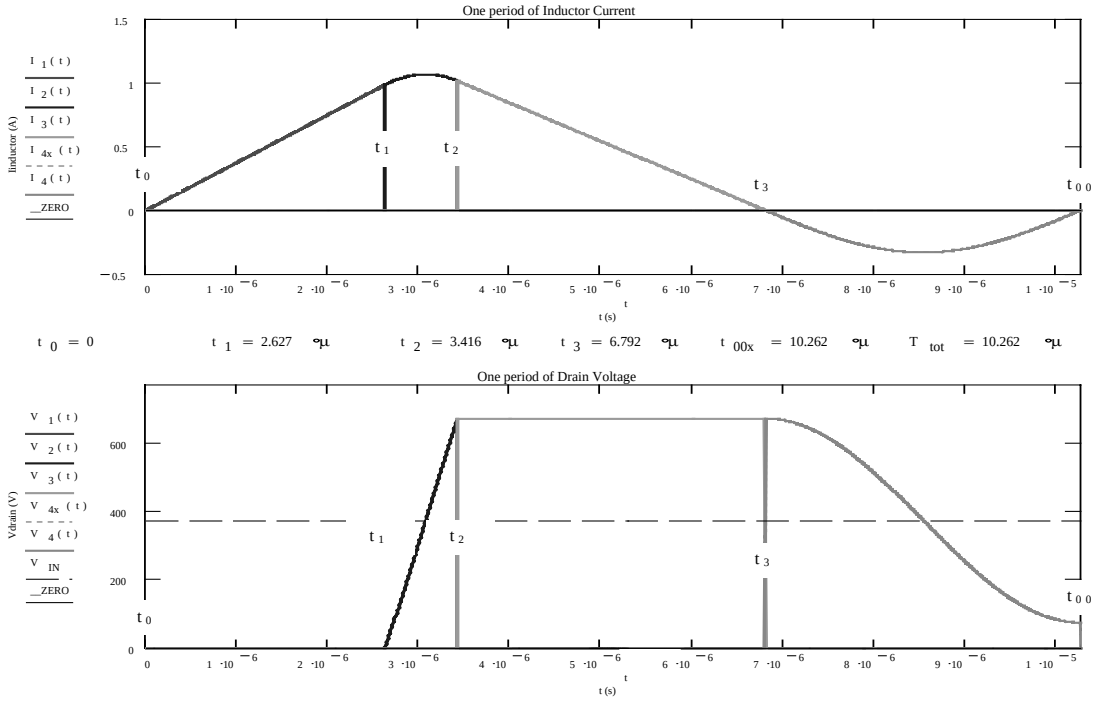

Figure 28 Waveforms $V_{IN} > n \cdot V_{OUT}$

The description of the period is mainly the same as the first situation when $V_{IN} = n \cdot V_{OUT}$, so the inductive current and drain voltage during all intervals can be described with the same formulas. The only difference is the voltage across the MOSFET during switch-on.

As can be seen in Figure 28 the MOSFET is switched on again at the valley of the drain voltage. The voltage level in this situation is not zero but slightly above zero. This is called LVS, which result in switch-on losses in the MOSFET.

APPENDIX 3 TRANSFORMER DATA

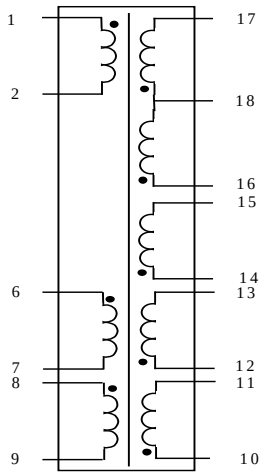

Figure 29 Transformer pin diagram

Electrical data	**Conditions**	**Value**	**Unit**
Inductance 6-9[1]	1V @ 10kHz	1000 ±5%	µH
Leakage inductance[2]	0.2V @ 100kHz, all secondary windings shorted	≤ 10	µH
Core data	**Material**	**Airgap**	
E42/21/15	3C85	TBD	µm
Winding data	**Description**	**Number of turns**	**Wire dia**
Primary windings			
6-7	Main input	28	8 x 0.2
8-9	Main input	27	8 x 0.2
1-2	Auxiliary	3	0.2
Secondary windings			
10-11	Main output 185V	34	8 x 0.2
12-13	80V	15	0.2
14-15	16V	3	0.3
16-18	10V	2	0.2
18-17	-10V	2	0.2

Table 9 Transformer data

Note 1: For primary inductance measurements pins 7 and 8 have to be interconnected

Note 2: For leakage inductance measurements all secondary pins have to be interconnected