EMI Reduction Techniques

Cameron Katrai and Chris Arcus

Electromagnetic interference (EMI) is increasing as a result of higher clock speeds in today's PCs and workstations. This radiation, mainly produced by fundamental and low-order harmonics, unfortunately coincides and interferes with many popular radio FM bands. This has forced the regulatory agencies to place limits on electromagnetic radiation produced by PCs and any electronic instrument that might use clocks and generate emissions.

Electromagnetic Interference Analysis

Almost any electrical transitions with sharp edges, such as clocks, data, address and control, produce electromagnetic radiation. As performance requirements increase, clock speeds have also increased. The transition edge, or in engineering terms, the slew rate, has become faster and faster as the need for meeting set up and hold time has become harder to meet. Set up is the time needed for a data pulse to be stable before the rising edge of the clock, and hold time is the time for the data pulse to remain stable after the edge of the clock.

Clocks are no longer fed to only one or two devices on circuit boards. Rather, they are being distributed all over the circuit board. Also, increased memory requirements, and other loads on the clock lines, have significantly contributed to electromagnetic radiation. EMI is linearly proportional to current, the area of the current loop, and with the square of frequency. EMI is defined as $EMI = kIAf^2$ where I is the current, A is the loop area, f is the frequency, and k is the constant depending on PCB materials and other factors. There are two types of EMI radiation: Differential Mode and Common Mode . Current loops formed between traces and the ground plane on PC add-in cards and motherboards cause the Differential Mode. These loops act as antennas and radiate EMI that may exceed FCC limits. Localized ground noise injected into the PC's I/O traces and cable causes Common Mode radiation. Since these cables and traces are long, they act as antennas. In the past, shielding was the most prevalent method used to decrease EMI.

One powerful method to reduce EMI is the spread spectrum technique which modulates the signal and spreads the energy over a wider frequency range. Spread Spectrum is a controlled and careful modulation of the clock signal in a way that does not contribute significantly to jitter. It has been successfully shown that by using Spread Spectrum, radiation has been lowered from 7 to 20dB depending on the degree of modulation.

Spread Spectrum Analysis

The Spread Spectrum technique is primarily applied to squarewave signals. Squarewave signals include both the fundamental frequency and odd multiples of the fundamental frequency. Energy is contained in both the fundamental and the harmonics. The energy contained in the harmonics decreases with order since the spectral density rolls off at a rate that is inversely proportional to the frequency. It is important to mention several facts here.

First, most clocks do not have a 50 percent duty cycle. The result is the magnitude of harmonics is higher. Second, the spectrumis related to the Fourier transform of the signal, which transforms the signal into its frequency domain. The Fourier transform displays the signals in the frequency domain, and shows the frequency content of that signal. For example, a sinusoidal signal that is only at a single frequency will appear as a vertical spike at that frequency in the frequency domain.

The most severe radiation involves the fundamental, the third, and fifth harmonic of the clock frequency. Distributing the fundamental energy over a tightly controlled range, as in the Spread Spectrum method, also distributes the harmonic energy over a wider range. This is because the bandwidth of the nth harmonic is n times the bandwidth of the fundamental. The spread spectrum method must be controlled and slow compared to clock rate to guarantee that the change in the clock rate is transparent to the system. Both cycle-to-cycle jitter and peak-to-peak jitter must remain within the system's specifications.

Method

The modulation method is a very simple concept. Usually the modulation is measured as a percentage. For example, a 0.5 percent modulation means that a 100 MHz clock is modulated between 99.5 MHz and 100.5 MHz. This is called a center 0.5 percent modulation (Δ) since the 100 MHz fundamental frequency remains the center frequency.

Another important factor is the modulation frequency. This frequency, usually in kHz range, is basically a measure of the rate the frequency is swept between 99.5 and 100.5. The linear sweep is predictable and most prevalent.

The spread spectrum method must guarantee also that the minimum clock period is not violated. The clock is usually swept between 99.5 and 100 MHz to avoid exceeding the maximum frequency of the system. In this method, called down spreading, the clock frequency deviation is measured as a negative percentage and the spread is - 0.5 percent (Δ). Linear modulation is also called triangular modulation. A general example of a triangular frequency modulation profile is shown in Figure 1. The modulation profile in a modulation period can be expressed as follows:

$$F = \begin{cases} (1 - \Delta)\, f_{NOM} + 2\,(\Delta)\,(f_M)\,(t)\, f_{NOM} & (\text{when } 0 < t < 1/f_M) \\ (1 + \Delta)\, f_{NOM} - 2\,(\Delta)\,(f_M)\,(t)\, f_{NOM} & (\text{when } \frac{1}{(2\, f_M)} < t < 1/f_M) \end{cases}$$

Where f_{NOM} is the nominal clock frequency in the non-Spread Spectrum mode, f_M is the modulation frequency and Δ is the modulation amount, or the amount of change in the clock frequency.

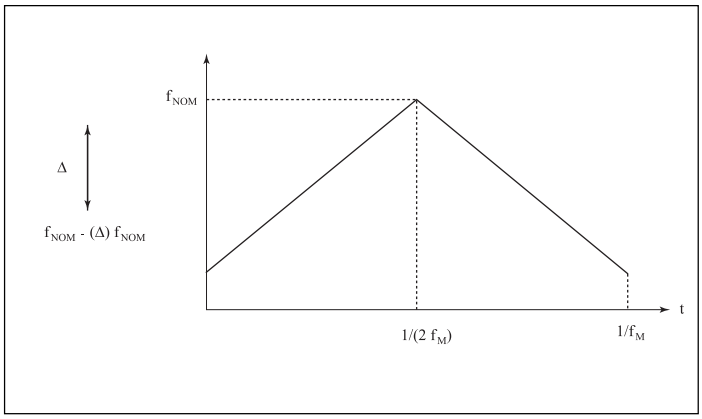

Figure 1. Clock Modulation Profile

Spread Spectrum has been mainly applied to system clocks. (The clock specifications for today's 400 MHz PCs call for specific reductions in Electromagnetic Radiation generated by the clock alone.) Table 1 shows an example of Desired Peak Amplitude reductions by Spread Spectrum.

Table 1. Desired Peak Amplitude Reduction by Spread Spectrum

CPU Clock Frequency	Peak EMI Reduction = PR	Measurement Frequency
66 MHz	7dB	600 MHz (9th harmonic)
100MHz		700 MHz (7th harmonic)

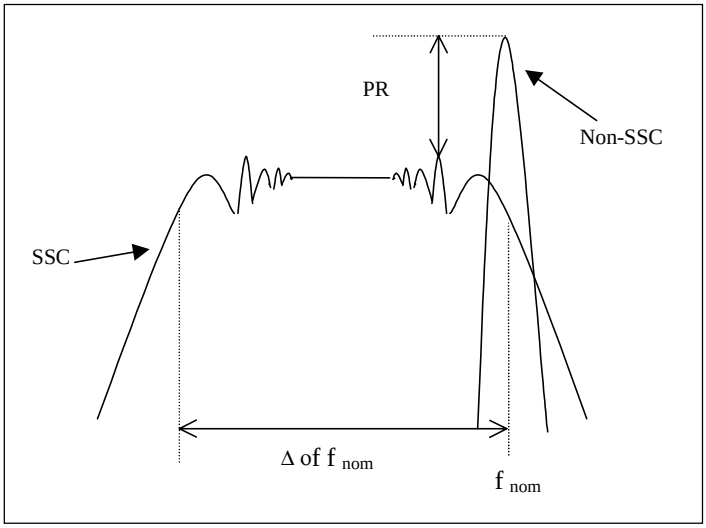

Figure 2. Spectral Fundamental Frequency Comparison

Pericom Clocks such as PI6C104 for desktop applications and PI6C103 and 102 for mobile applications with Spread Spectrum capability allow more margins for EMI emission compliance in the overall system. All Pericom Desktop and Mobile PC clocks possess Spread Spectrum EMI reduction capability. PI6C104 Spread Spectrum capability provides modulation on the CPU and PCI Clocks only. Clocks such as REF and other fixed clocks (24 and 48 MHz) are not modulated.

With the use of I²C control method, Pericom's PC clocks allow several types of modulation. For example the PI6C104 allows Δ of ±0.5%, ±0.9%, ±1%, -1%, -0.5%, ±0.25% and no modulation at all (Spread Spectrum is off). Moduation frequency is set at 60 kHz.

Jitter

The Spread Spectrum modulation introduces an insignificant amount of jitter to the clock. At modulation frequencies such as 30 to 60 kHz, this jitter can be shown to be small and insignificant.

As shown in Figures 1 and 3, the sweep from (1- Δ) f_{NOM} to f_{NOM} happens in $1/2f_M$ time period. For f_{NOM} of 100 MHz, the T1 is 1/100 MHz and Tn = 1/99.5 MHz (Δ is 0.5%).

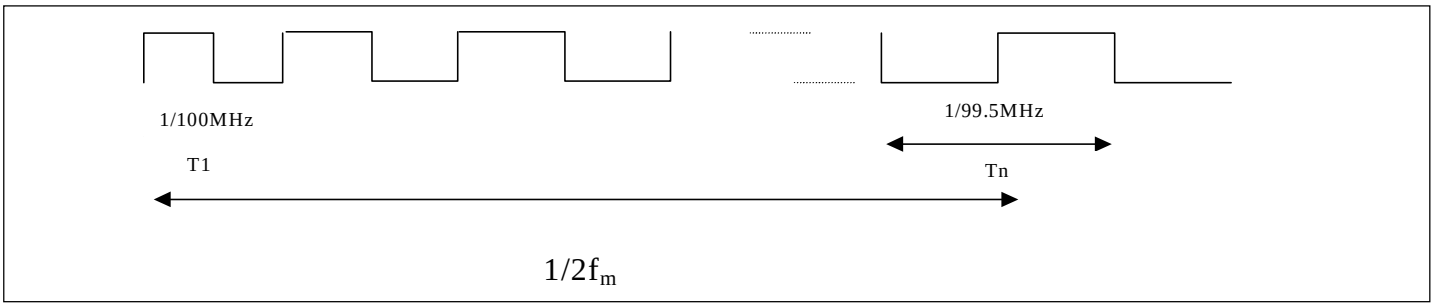

Figure 3. Sweep Profile

The maximum period difference between the cycles in $1/2f_m$ time period is defined as Tn – T1.

$$Tn - T1 = \{1 / [(1-\Delta)fnom]\} - 1/fnom \qquad (2)$$

We define the total number of Cycles that exist between Tn and T1 as N. The total time is $1/2f_m$.

N is given by dividing the total time $1/2f_m$ by the average of the spread spectrum frequency.

$$N = [1/(2f_m)] / (1/f_{avg}) = f_{avg}/(2f_m) \qquad (3)$$

Combining 2 and 3 we can then calculate the jitter.

$$Jitter = (Tn - T1) / N$$

$$Jitter = (2f_m\Delta)/ [(1-\Delta)(1-\Delta/2) fnom^2]$$

For example, if fnom is 100 MHz, f_m is 60 kHz, and a Δ of 0.5 percent, Jitter is calculated to be only 0.0604 picosecond.

Other Helpful Guides

To combat EMI, designers have also adhered to a series of guides and methods. Here are some of these methods:

We highly recommend that solid ground and power planes be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops. In this example, the larger the current loops the higher the magnitude of radiation. Routing any channel lines, especially clocks, over a segmented ground plane must be avoided.

Place the clock drivers near the center of the PCB rather than at the periphery. A periphery location increases the magnetic dipole moments. For clock traces that are routed on the surface plane, to further reduce EMI, it is better to route parallel ground traces on either side of the clock trace. However, it is even better to place the clock traces in the layer in between Ground and the Vcc plane. Use 4 to 8 mil traces for clock signals since narrow signal traces tend to increase high frequency damping and reduce capacitate coupling between traces. In general, right angles or 'T' crosses should be avoided. Right angles increase trace capacitance and also add an impedance discontinuity that effect signal degradation.

Impedance must be matched as closely as possible. Usually cases impedance mismatches cause emissions. Signal integrity mainly depends on impedance matching. Do not run long clock traces parallel to each other because they effect crosstalk that contributes to EMI.It is a good idea to make sure that the spacing between traces is at least equal to the trace width.

If you are designing graphic memory subsystems, make sure clock traces are placed at least 2.5 inches away from any PC I/O connector. This includes parallel ports, serial ports, keyboard connector, monitor connector, etc. This method should minimize common mode radiation which is reduced by placing ground isolation trenches around the I/O connector. To suppress high frequency common mode radiation, we suggest ferrites with appropriate impedance characteristics. Since the impedance of the ferrites varies with frequency, at high frequency ferrites behave more like a resistor than an inductor. At high frequencies ferrites resistive losses can be used to fight radiation.

Using Vdd decoupling capacitors for clock sources (whether external or internal) should help reduce the EMI. Placement of decoupling caps is very important to reduce emissions from the clock source's package. All capacitors should be placed within 20 mils of the Vdd pins. Decoupling cap values are based on the resonance frequency of the capacitor. Capacitors in the 100pF range are appropriate for the higher frequencies of the clock generator.

Reduce both the length of the high frequency trace and the area of current loops.

RC filters at the clock source are placed to control rise and fall times. Slower rise and fall times (as slow as possible without violating timings) result in lower emitted frequencies.

Power supply pins for the clock should be next to the ground pins. Minimize power supply loops. By keeping power and ground leads parallel and adjacent to each other, significant reductions in package EMI can be realized.

More Filtering

When the source of the signal noise cannot be eliminated, filtering is recommended as the last resort. EMI filters and ferrite beads are commonly available filters. Ferrite beads add inductance to suppress high frequency.

EMI Filters

EMI filters are commercially available to eliminate high frequency noise in power lines. They not only stop the noise from entering the system, they also stop the noise manufactured by the system to leave the system and reach other parts of the bigger system. This effect is called bidirectional. A combination of inductors and capacitors make up the EMI filters. The impedance of the node that requires an EMI filter determines this configuration of capacitors and inductors. A high-impedance node requires a capacitor and a low-impedance node requires an inductor.

EMI filters can also be in configurations such as feedthrough capacitors, L-Circuits, PI-Circuits, and T-Circuits. The component of a feedthrough capacitor component is a capacitor. Feedthrough capacitors are good choice when the impedance connected to the filter is high. Figure 4 (see below) depicts the feedthrough capacitor. The feedthrough capacitor does not provide high frequency current isolation between nodes.

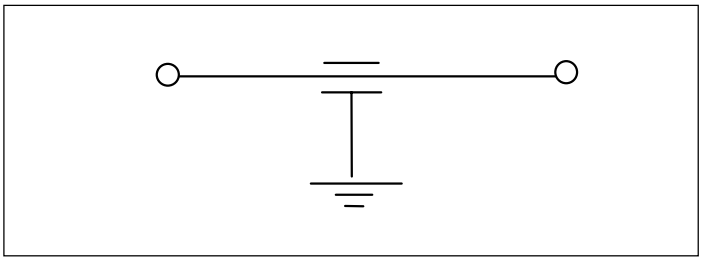

Figure 4. Feedthrough Capacitor

As shown in Figure 5 below, the L-Circuit has an inductor on one side of the capacitor. This configuration works best for the line and load that have a large difference in impedance. The inductive element gets connected to the lowest impedance.

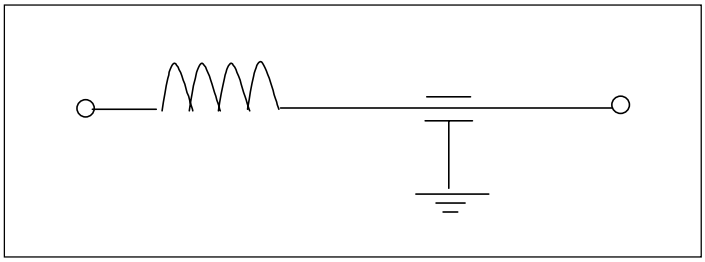

Figure 5. L-Circuit with Inductor on One Side

As shown in Figure 6, in a PI-Circuit two capacitors surround an inductor. When the line and load have a large difference in impedance, the PI-Circuit is the most suitable. The PI-Circuit also is used when high levels of attenuation are needed.

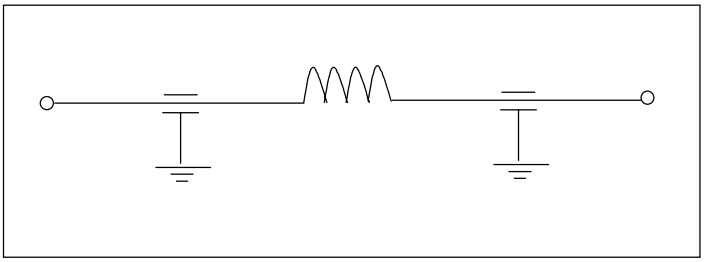

Figure 6. PI-Circuit with Two Capacitors Surrounding an Inductor

As shown in Figure 7 below, the T-Circuit has inductors on either side of the capacitor. It works best when both line and load impedances are low.

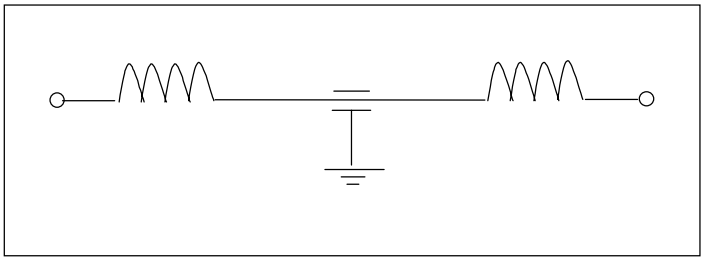

Figure 7. T-Circuit with Inductor on Either Side of the Capacitor

Ferrite Noise Suppressors

As shown in Figure 8 below, the Ferrite noise suppressors are beads surrounding the conducting material.

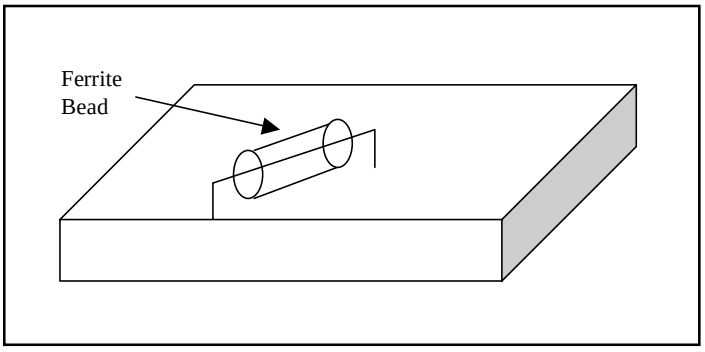

Figure 8. Ferrite Noise Suppressors

Ferrite suppressors add inductance in series with the line. The added impedance is a function of frequency. The insertion loss is calculated from the formula below:

$$\text{Loss (db)} = 20 \text{ Log}_{10} [(Zs + Z_L + Z_F) / (Zs + Z_L)]$$

Where Zs = Source Impedance
Z_L = Load Impedance
Z_F = Ferrite Impedance

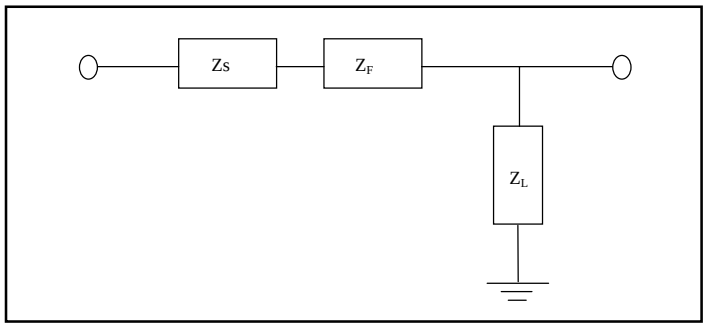

Figure 9. Equivalent Circuit

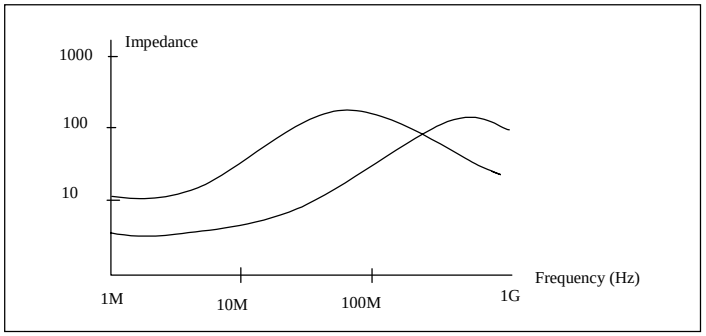

Figure 10. Frequency Response of Ferrite Filters

Without adding DC resistance, ferrite suppressors add sufficient inductance to the line. This ferrite suppressor quality makes them the ideal choice for line-noise suppressors on Vcc pins of devices.

Device Speed

In addition to clocks, high-speed devices generate more high-frequency noise. This is as a result of shorter transition times that have more energy in the high frequency range. Figure 11 shows a square wave pulse with its related Fourier transform. Looking at the Fourier transform, there are two points of interests. The period of the square wave determines the $1/\pi t_L$ on the Fourier transform. The transition time of the signal or the slew rate determines the $1/\pi t_F$. After this point ($1/\pi t_F$), the curve drops off very rapidly. This shows that the $1/\pi t_F$ point is the highest frequency component of the signal.

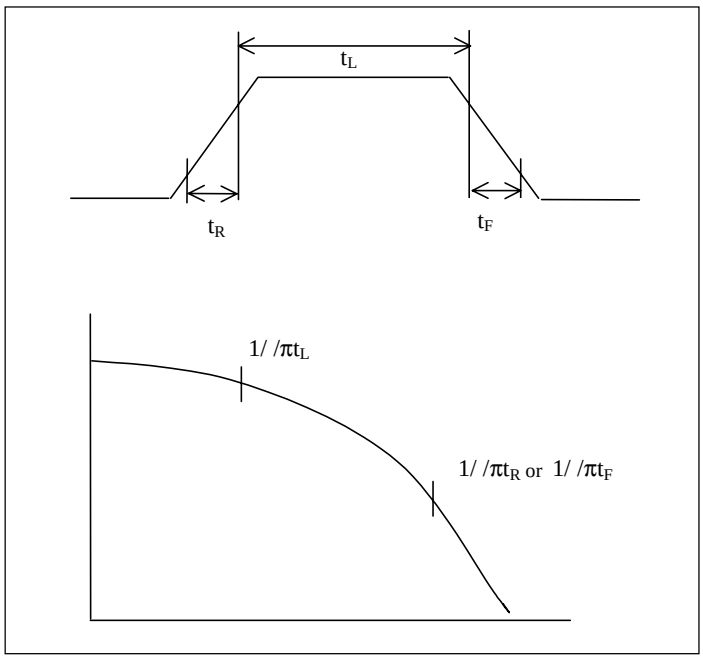

Figure 11. Square Wave Pulse with Related Fourier Transform

For example the frequency component of the edge of a device with a typical transition time of 1.5 ns is calculated as:

$$F = 1/\pi 1.5\text{ns} = 213 \text{ MHz}$$

This shows that regardless of clock frequency, the output signal has a high-frequency component of 213 MHz.

Summary

Over all, the spread spectrum method, which has allowed system performance to increase without compromising EMI, can expedite a product's time-to-market by eliminating interference and by reducing packaging and shielding costs. However, designers should also use all available methods and guides to reduce EMI.

Tips for Noise Reduction Techniques when Designing with Clocks

- ☐ If there are Op Amps in the design, terminate unused op-amps in dual and quad packs by grounding the positive input and connecting the – input to the output.
- ☐ Filter all signals leaving a noisy environment and filter all signals entering the board.
- ☐ Place I/O drivers near where they leave the board.
- ☐ Place the crystals flush to board and ground them.
- ☐ Place the clock at the center of the board, however, if the clock goes off the board, place the clock near the connector.
- ☐ Divide the circuits on the board based on their frequency and current switching levels.
- ☐ Separate noisy and quiet leads.
- ☐ Separate digital and analog lines and route the signals away from each other.
- ☐ Clock and digital signal lines must be placed as far away as analog input and voltage reference pins.
- ☐ Clock circuit must be placed away from I/O cables.
- ☐ Length of sensitive leads such as decoupling capacitors must be as short as possible.
- ☐ Use all power and ground pins of an IC.
- ☐ To cancel mutual coupling, twist noisy lead together.
- ☐ Place a ground lead between low-level signal leads and noisy leads in the same connector like a ribbon cable.
- ☐ Keep high-speed lines short and direct.
- ☐ Avoid running trace under Crystal.
- ☐ Sensitive traces should not be run in parallel with high current, fast switching signals.
- ☐ Critical traces should have Wide Trace and must be guarded with a ground on each side of the trace.