

THREE AND FOUR PHASE BRUSHLESS DC MOTOR CONTROLLERS USING PULSE-WIDTH MODULATION

May 1993

ABSTRACT

This paper describes the five motor circuits which drive brushless DC Motor controllers and are available as standard products from LSI Computer Systems, Inc. The theory of operation of each of the circuits is explained, accompanied by circuit block diagrams. Numerous applications are illustrated and interface circuits for driving high voltage motor windings using bipolar and MOS power transistors are indicated. The first of these five is the LS7261, which is an open or closed loop commutator sequencer. It operates at 7 to 28 Volts and has externally selectable input and output codes for 60°, 120°, 240° and 300° electrical sensor spacing. It has a pulse width modulation for analog speed control and forward/reverse inputs. In addition, this circuit contains positive static braking, overcurrent input, and an output enable control. There are 6 outputs for driving 3 phase or 4 phase motors.

Whereas in the LS7261 the overcurrent causes the outputs to switch on and off directly from the overcurrent sense input, the LS7260 and LS7262 circuitry causes the outputs to switch off immediately upon sensing the overcurrent condition. It only switches back on at a rate determined by the pulse width modulation chopping rate.

The LS7263 is a highly accurate speed regulator operating at 10 to 28V and designed to control the speed of a 3-phase brushless DC motor. The specific circuit is programmed for 3600 RPM applications using a 3.58MHz crystal. Other speeds can be controlled by changing the crystal frequency or by having the circuit reprogrammed by the company. It is presently available for 4 or 8 pole motors and 60° and 120° sensor separation.

The LS7264 is basically the same as the LS7263 except that it was designed for the 4-phase brushless DC motor.

switches are separated electrically by 60°, 120°, 240° or 300°. Figure 1 illustrates the commutator circuit block diagram. CS1 and CS2 inputs are used to select the proper decode mode depending on the Hall electrical separations. S1, S2, and S3 designate the Hall inputs. Also indicated are the forward/reverse inputs, the enable input, the brake input, the common input and the output drivers. The speed of the motor can be controlled by the sawtooth oscillator circuitry. The external R-C network was chosen to set the oscillator at approximately 30KHz. The oscillator will ramp within the power supply rails as shown. By adjusting VTRIP to the desired voltage, the comparator output duty cycle can be adjusted to be between 0 and 100%. This output is then applied to the output driver circuitry and causes the outputs to be chopped at the oscillator frequency. Varying the duty cycle will result in output drive signals that can vary from full-off to full-on or to any level in between.

The LS7260 and LS7262 incorporates a flip-flop as part of the overcurrent protection circuitry. An overcurrent condition generates a voltage greater than VREF and resets the flip-flop which disables the output drivers through the And gate. When the overcurrent condition terminates, the next positive sawtooth oscillation edge will enable the drivers

BRUSHLESS DC MOTOR COMMUTATOR

The advent of brushless DC motors has brought with it the need to integrate its unique circuit control requirements into a flexible, low cost integrated circuit. The ideal circuit should be able to commutate 3 and 4 phase motors. It should have some means of controlling the speed of the motor. It should also have overcurrent protection circuitry, a brake input, a forward/reverse input and be able to accommodate different electrical sensor spacings.

The heart of the LS7261 and the LS7262 commutator circuit is the decoder which senses the Hall effect inputs and creates the proper turn-on sequence of the output devices which are used to drive the motor. In addition, these circuits are able to commutate properly whether the Hall switches are separated electrically by 60°, 120°, 240° or 300°.

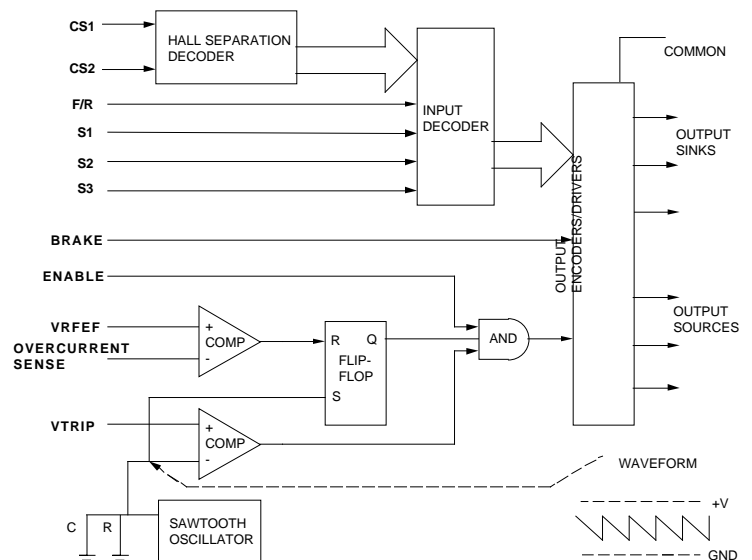


FIGURE 1
LS7261/LS7262 BLOCK DIAGRAM

again. The ensuing result of this circuit is to limit the maximum switching rate of the output drivers to the chopping frequency. The LS7261 does not have this flip-flop. The overcurrent sense comparator drives the And gate directly. In this case, the motor and driver circuit time constants will determine the maximum output driver switching rate.

Using the LS7261/LS7262 for three phase push-pull operation, the output driver circuitry consists of six MOS transistors with a common terminal. The output circuit driving a delta configured motor is shown in Figure 2, while a center tapped single ended driver circuit is illustrated in Figure 3. Pin numbers are included for reference. The sequencer logic causes the external driver transistors to turn on in the correct timing relationship. Referring to Figure 2, it can be seen that in order to drive the motor windings, the external transistors must turn on in pairs. For example to drive winding L1, PNP transistor Q1 and NPN transistor Q5 must turn on simultaneously or PNP Q2 and NPN Q4 must turn on simultaneously. These transistors are turned on by enabling internal MOS driver transistors. Turning on transistors Q2 and Q5 require QA and QE to turn on. By driving the gates of MOS transistors QA and QE negative, current is forced to flow through the bases of Q1 and Q5. Output 1(O1) sinks current and Output 5 (O5) sources current. Similarly, enabling QB and QD causes current to flow through the bases of Q2 and Q4.

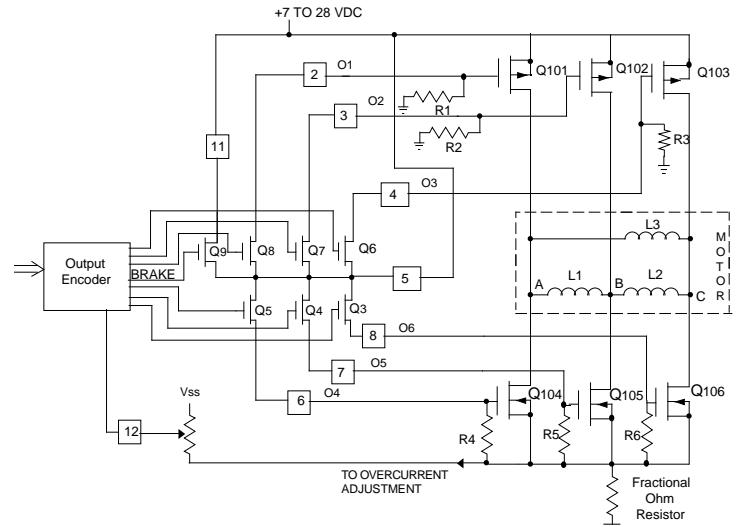


FIGURE 2A. BIPOLAR THREE PHASE OUTPUT DRIVER CIRCUITRY

Figure 2A indicates a similar circuit using the LS7260 for driving P Channel and N Channel FETS and developing a full 12 Volt Drive for the N Channel and P Channel FETS when using a 12 Volt supply. In this configuration, the appropriate bottom N Channel transistor turns on while the upper P Channel transistor turns off. To turn winding L1 on, Q8 of the LS7260 turns off, allowing the external resistor R1 to force the gate of Q101 to ground. Since the source of Q101 is tied to +12 Volts, the gate drive on Q101 is -12 Volts. Internal transistor Q4 is turned on and since Pin 5 of the LS7260 is tied to +12 Volts, the gate drive of Q105 becomes +12 Volts. Current is forced through L1 from Q101 to Q105. Similar current is reversed through L1 when P Channel FET Q102 turns on and N Channel FET Q104 turns on. The overcurrent sense circuitry performs in exactly the same manner as the LS7262 does when driving bipolar transistors. The overcurrent conditions causes internal transistors Q3, Q4 and Q5 to cut off and Q6, Q7 and Q8 to turn on. This causes the external power FETS to turn off. Applying the brake signal causes internal transistors Q6, Q7 and Q8 to turn on cutting off the external P Channel power FETS and causes internal transistors Q3, Q4 and Q5 to turn on which, in turn, turn on the external N Channel power FETS. This causes the Motor windings to short together stopping the motor. As in the LS7262, the brake signal always overrides the overcurrent sense input.

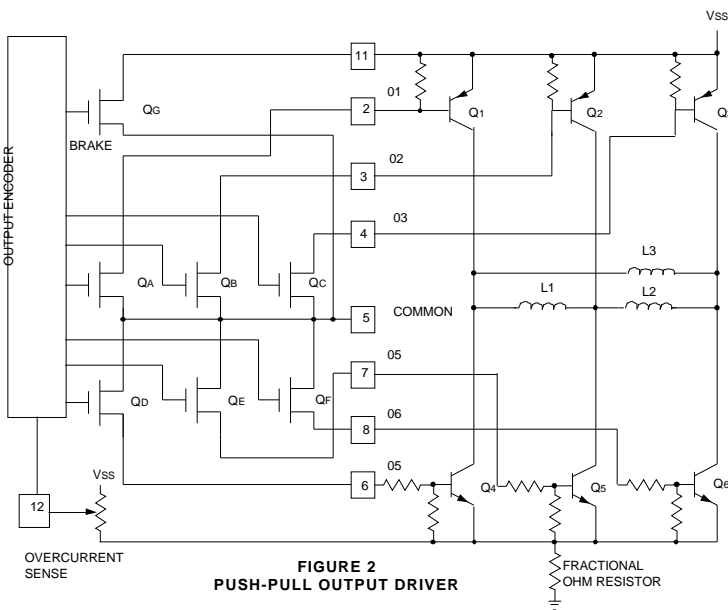


FIGURE 2 PUSH-PULL OUTPUT DRIVER

Using the LS7261/LS7262, the overcurrent circuit indicated in Figure 2 consists of a potentiometer and a fractional ohm resistor. The potentiometer is adjusted until all outputs are disabled for currents greater than the desired limit. During the overcurrent condition, all MOS driver transistors are cut off which causes the bipolar driver transistors to disable. If a brake signal is applied, then the common terminal is forced to the positive supply voltage, Vss. Since QA, QB, and QC are turned on, O1, O2 and O3 are driven to the positive supply voltage cutting off external transistors Q1, Q2 and Q3. In addition, internal transistors QD, QE and QF are turned on which causes Q4, Q5 and Q6 to turn on shorting the motor windings together and stopping the motor. The brake signal always overrides the overcurrent sense input.

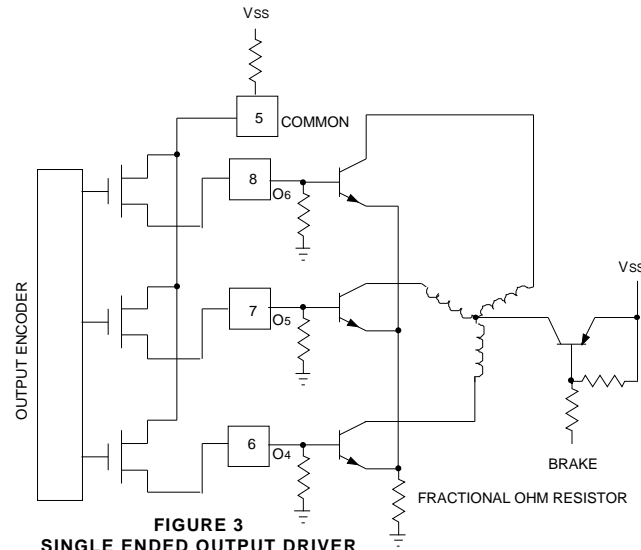


FIGURE 3 SINGLE ENDED OUTPUT DRIVER

Figure 3 shows a much simpler set up using single ended drivers. Q₄, Q₅ and Q₆ will turn on sequentially as before. Only one base current limiting resistor is required and this is in series with the common terminal that is connected to the supply voltage. Applying the brake to this circuit causes all the output transistors to turn on and the motor power supply to disconnect which causes the motor windings to short together.

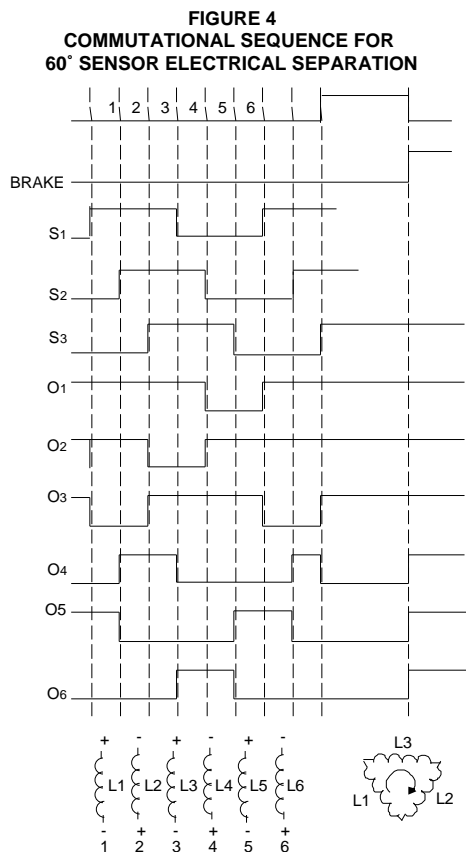


Figure 4 indicates the output commutation sequence for sense inputs which are 60° electrically separated and for the forward/reverse input equal to a logic 1. The motor is assumed to be wound in a delta configuration and clockwise is assumed to indicate a positive voltage. The circuit is assumed to be configured as in Figure 2. When S₁ is high and S₂ and S₃ are low, O₃ becomes negative and O₅ becomes positive turning on the winding L₂ as shown. This is commutation State 1 as shown in Figure 4. The next commutation State 2 occurs when S₁ and S₂ are high and S₃ is low. In this case, O₃ becomes negative and O₅ becomes positive turning on winding L₂ as shown. This is commutation State 1 as shown on Figure 4. The next commutation State 2 occurs when S₁ and S₂ are high and S₃ is low. In this case, O₃ remains negative and O₄ becomes positive causing winding L₃ to turn on as shown. The rest of the sequence is indicated in Figure 4 and will repeat every rotation of 360° electrical degrees. The overcurrent condition causes O₁, O₂ and O₃ to become high and O₄, O₅ and O₆ to become low. As stated previously, this causes all of the output bipolar transistors to cut off. Also as indicated previously, this causes all of the output bipolar transistors to cut off. Also as indicated previously, the brake input causes all the outputs to go high shorting the motor windings together.

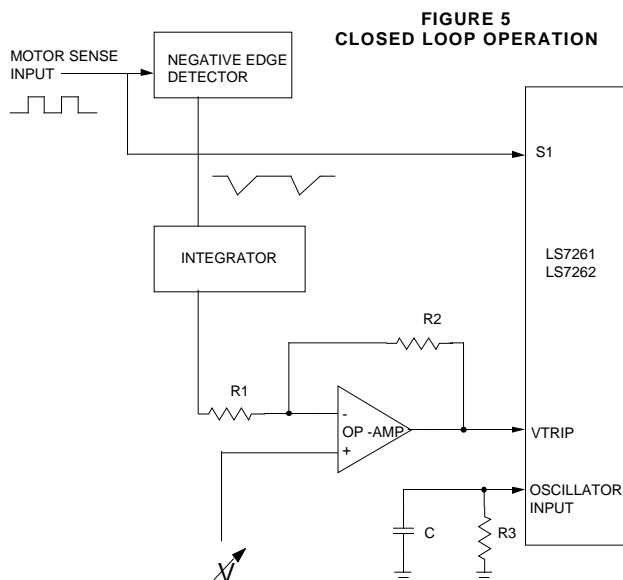
The LS7261 or LS7262 can also interface with four phase motors by connecting inputs CS₁ and CS₂ low and connecting Hall sense inputs S₂ and S₃ together. Four phase operation is indicated by Table 1.

S1	S2,S3	FWD/RVS = 1	FWD/RVS = 0
0	0	01	04
1	0	03	06
1	1	04	01
0	0	06	03

TABLE 1 - FOUR PHASE COMMUTATION

The four phase motor uses two Hall sensors 90° electrically apart. The Hall inputs create four outputs turning on successively as indicated in Table 1. For single ended drive with center tapped windings, the circuit common is tied to the positive supply through a base limiting resistor and outputs O₁, O₃, O₄ and O₆ drive transistors whose collectors are tied to the four coil windings of a four phase motor and whose center tap is tied to the motor supply.

Circuit driving FETS can be used for the LS7261 or LS7262. A closed loop operation block diagram is depicted in Figure 5. Either one, two or three Hall sense inputs can be used as inputs to the negative edge detector. If two sense inputs are used, they are applied to an exclusive OR gate whose output drives the negative edge detector. Three sense inputs require two exclusive OR gates. The use of two or three inputs will increase the loop gain of the feedback loop since the number of pulses appearing at the output of the negative edge detector will double or triple. In Figure 5, one Hall sense input (S₁) is depicted. The output of the negative edge detector is applied to the integrator and consists of pulses whose width is constant but where the separation between pulses is a function of motor speed. The integrator produces a negative DC voltage whose value depends on the separation of pulses. If the motor speed increases, pulse separation decreases causing the output of the integrator to become more negative and the output of the operational amplifier to increase. This raises the VTRIP input to the LS7261/LS7262 and lowers the duty cycle of the output driver circuitry. The lower duty cycle will cause the motor speed to decrease. Similarly, a decrease in motor speed causes the pulse separation to widen resulting in a decrease of voltage at the VTRIP input which raises the output driver duty cycle and the resultant motor speed. The desired speed is set by varying the voltage at the positive input terminal of the Op-Amp which adjusts the nominal VTRIP input.



BRUSHLESS DC MOTOR SPEED CONTROLLER

The LS7263 and LS7264 are designed for 3600 RPM \pm .1% regulated, fixed speed operation using a 3.58 MHz parallel resonant crystal. The circuits contain programmability for tailoring to specific motor applications. The principle of operation is similar to the closed loop operation previously described. Speed is adjusted by varying the output driver duty cycle. However, the output is not chopped as in the LS7261/LS7262. For each commutation, the corresponding motor winding is turned on and remains on for a percentage of the total time that occurs before the next commutation sequence begins. The On time is determined by a mask programmable ROM Look-Up Table.

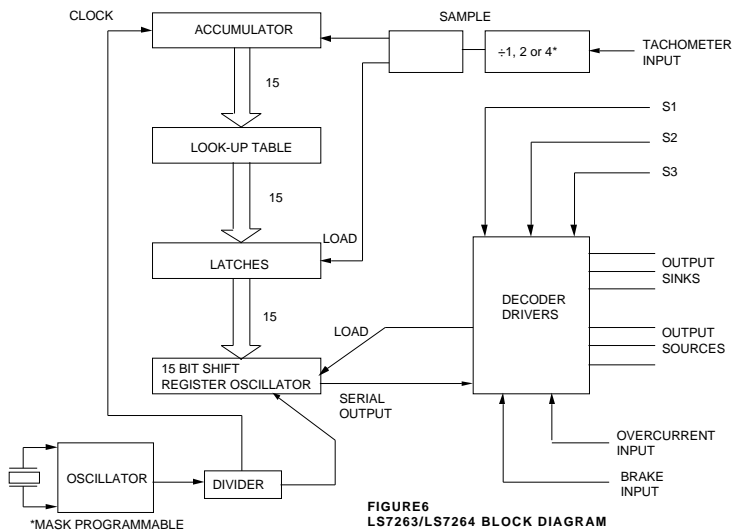


FIGURE 6
LS7263/LS7264 BLOCK DIAGRAM

Figure 6 illustrates a simplified block diagram of the circuit. The tachometer input can be any one of the three Hall sense inputs S₁, S₂ or S₃. This input can be divided by 1, 2 or 4 which is mask programmable. This enables speed update information to be gathered either once or twice a revolution for a four pole motor and once, twice or four times a revolution for an eight pole motor. The output of the tachometer divider circuit is used to transfer new data to the latches and reset the accumulator enabling it to count clock pulses from a zero setting. The accumulator counts for a period equal to the time between tachometer inputs (or a multiple or that time). The number reached in the accumulator is proportional to the time between tachometer inputs which is inversely proportional to the motor speed. As the accumulator advances, its output which addresses the ROM Look-Up Table causes the 15 outputs from the Look-Up Table to change from all logic zeros to logic ones, one at a time. The next output of the tachometer divider loads the Look-Up Table outputs into the latches and resets the accumulator to zero. The output driver duty cycle is proportional to the number of stages of the 15 stage latch that are set to a logic one. If the motor had been going at a much slower speed than desired, the latches would be loaded with all logic ones. If the motor had been going at too high a speed, the latches would be loaded will all logic zeros. If the motor is at or near the desired speed, then some of the latches would be loaded with a logic one and others with a logic zero. The exact curve of the percentage of on-time versus speed and therefore, the loop gain is determined by the ROM in the

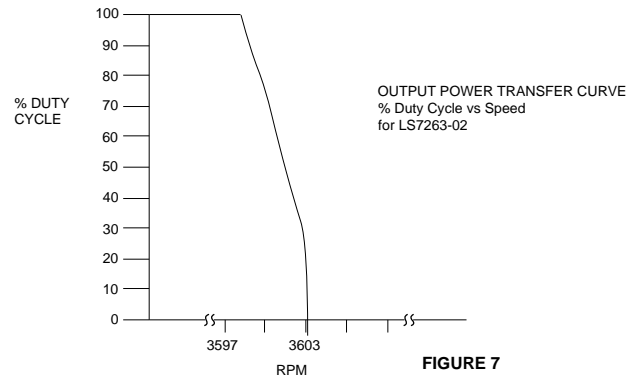
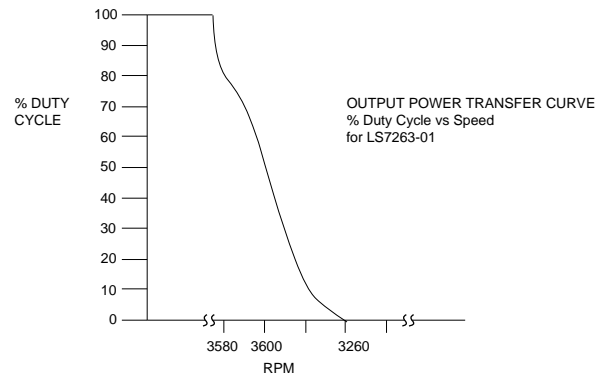


FIGURE 7

Look-Up Table and can be tailored to specific motor designs. Figure 7 illustrates the output power transfer curve for 2 versions of the LS7263. The medium gain LS7263-01 circuit has its duty cycle change from 0 to 100% over a 40 RPM motor speed change while 0 to 100% duty cycle change for the high gain LS7263-02 occurs over a 6 RPM motor speed change.

The outputs of the latches are loaded at the beginning of each new commutation time to the 15-bit shift register. The shift register is clocked by a programmable divider. The divider, whose input is the 3.58 MHz crystal controlled clock, must be programmed to accommodate motors with different numbers of poles since the commutation time will vary, and therefore, the speed of the shift register clock must be made to vary. The 15 bits of the shift register are entirely shifted out during each commutation time and applied to the LS7263 decoder driver circuitry. Like the LS7261/LS7262, the LS7263 decoder can be programmed to accommodate sensor separations of 60°, 120°, 240° and 300°. The decoder is set for 90° separation for the LS7264. The decoder driver circuitry provides three output current sinks and three output current sources. These devices have output duty cycles which are determined by the number of latches in the 15 stage latch that are set to a logic one. They will become full On if the motor is going too slow and cut off if the motor is going too fast. A Quiescent condition occurs when the motor is operating at 3600 RPM. The output duty cycle under these conditions is between 30 and 70%. An overcurrent input is also provided which shuts off the output drivers during an overcurrent condition using a circuit similar to that used for the LS7261. Additionally, there is a brake input which will turn off all the sink outputs and turn on all the source outputs thereby shorting all the motor windings together. There are four versions of the LS7263. Each one has been tailored to a specific motor operating at a fixed 3600 RPM speed. At present, only one version of the LS7264 exists. Table II indicates the programming differences for each circuit available at present.

TABLE II. DEVICE PROGRAMMING

TACHOMETER	NUMBER GAIN	SENSOR DIVISION	SETTING	AT 3600 RPM	DIVIDER	DUTY CYCLE	TYPE	OF POLES	SEPARATION
7263-01	4		60		Medium	1	384		35%
7263-02	8		120		High	4	192		65%
7263-03	4		120		Medium	2	384		35%
7263-07	8		120		Medium	4	192		65%
7264	4		90		Medium	1	384		65%

Even though the LS7263 and LS7264 are designed for fixed speed 3600 PRM operation, other speeds are possible. For example, to operate at 5400 RPM using the LS7263-02, the motor tachometer input is first divided by two and then applied to the integrated circuit. Since the LS7263 now has more time to accumulate clock pulses, the circuit will interpret this to mean that the motor is going too slow and will therefore speed up. By using an external crystal of 2.68 MHz, the motor will operate at exactly 5400 RPM. An alternate method of varying speed is simply to adjust the oscillator input frequency. The oscillator input pin can be forced with an external drive signal instead of hooking it up as a crystal oscillator. By lowering the input drive signal frequency, less clocks will be counted in the accumulator. This will be interpreted by the LS7263 as going too fast and the motor will slow down operation. Operation down to 1500 RPM or less is possible using this technique.

MOTOR DRIVER CIRCUITS

The LS7260/LS7261/62/63/64 are all designed to operate from 7 to 28 volts and have similar output circuitry. Figure 2 indicates a mode of operation in which the motor controller circuit and the motor operate at the same power supply voltage. The LS7362 is identical to the LS7262 except that only the lowside drivers are pulse width modulated. This provides an ideal situation when the IC must interface with level converters to drive high voltage brushless DC motors. By pulse width modulating the low side drivers only, switching losses in the high side drivers is minimized. There are numerous applications in which the DC motor is designed to operate at a voltage higher than the integrated circuit can operate at. In this case, a level converter must be used. For the LS7261/LS7262 and LS7362 level converters are easily constructed if the common input, Pin 5, is tied to the integrated circuit positive supply

(Vss).

Figure 8 indicates how the LS7261/LS7262 and LS7362 can be used to interface with bipolar transistors to drive a high voltage brushless DC motor. NPN transistors Q101, Q102 and Q103 are used as level converters to drive output PNP bipolar drivers Q107, Q108 and Q109. The low side drivers are NPN transistors driven from the Vss supply. Figure 9 indicates how the same type level converters can be used to drive P Channel power FET stage Q107, Q108 and Q109. Zener diodes Z1, Z2 and Z3 are used to develop the proper gate drive levels for the power FETS. The low side drivers are N Channel power FETS driven from the Vss supply which will normally be set at 15 Volts to obtain proper N Channel power FET gate drive. Switching losses in Figures 8 and 9 will be less for the LS7362 than the LS7261 or LS7262 because only the low side drivers are pulse width modulated when using the LS7362, while both low and high side drivers are pulse width modulated when using the LS7261 or LS7262.

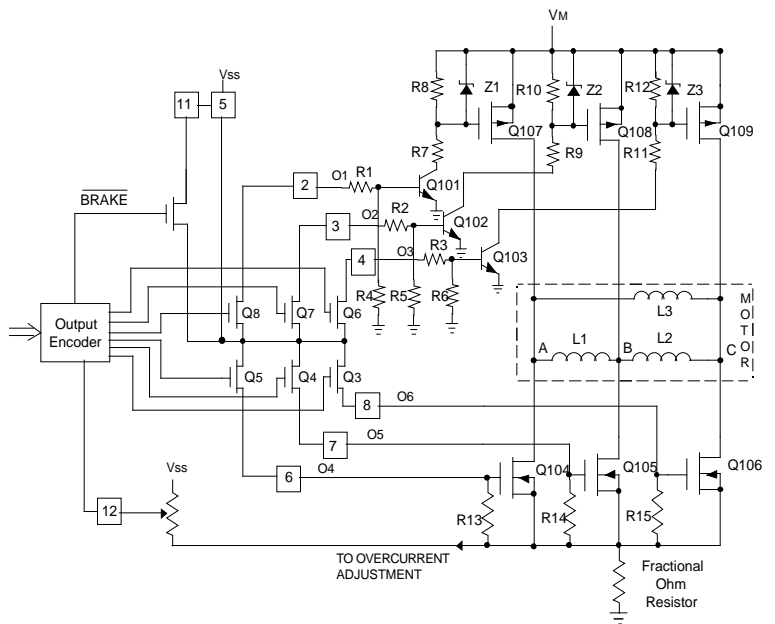
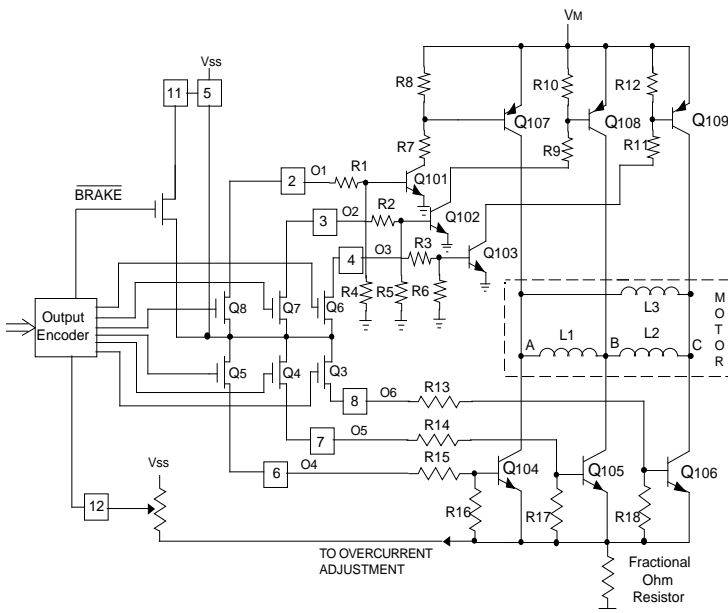


FIGURE 8. BIPOLAR THREE PHASE OUTPUT DRIVER CIRCUITRY

FIGURE 9. POWER FET THREE PHASE OUTPUT DRIVER CIRCUITRY

One of the disadvantages of the circuit illustrated in Figure 9, is the use of P Channel power FETS. P Channel power FETS are at a disadvantage when compared to N Channel power FETS. P Channel FETS have a much higher on-resistance, are harder to get and more expensive than N Channel FETS. High on-resistances reduce switching speed and absorb power which lowers efficiency and reliability. A more efficient power FET circuit utilizes identical N Channel power FETS in a push-pull configuration. In order to achieve this, an external supply must be developed for driving the gate of the upper N Channel power FET above the motor power supply voltage. A complete working circuit utilizing Siemens BUZ73 power FETS operating a 150 Volt 3 phase brushless DC motor is depicted in Figures 10 and 11. Figure 10 illustrates the power supply used for generating the upper N Channel gate drive. The 555 oscillator provides a square wave which is AC coupled to a diode network that is referenced to 150 Volts by the upper IN4004.

The lower 1N4004 rectifies the 12 Volt peak-to-peak square wave producing approximately 162 Volts DC at point G. This becomes the gate drive of the upper N Channel power transistor. Figure 11 illustrates the driver circuit. A high output on Pin 2 turns on Q1 and Q2 driving the gate of the upper N Channel FET to 162 Volts.

The source of this FET will then rise to the motor supply of 150 Volts. The 16 Volt Zener Diode protects the gate to source junction during the rise time. When the output at Pin 2 returns to zero, Q1 and Q2 will turn off causing the gate to source capacitance of the upper N Channel FET to be discharged rapidly through Q3. A high output on Pin 6 is buffered by two parallel inverters of a CD4050 for charging the gate capacitance of the lower BUZ73 N Channel power FET. A low output on Pin 6 causes the gate capacitance to discharge rapidly. This circuit is extremely efficient since significant current only flows during the switching times.

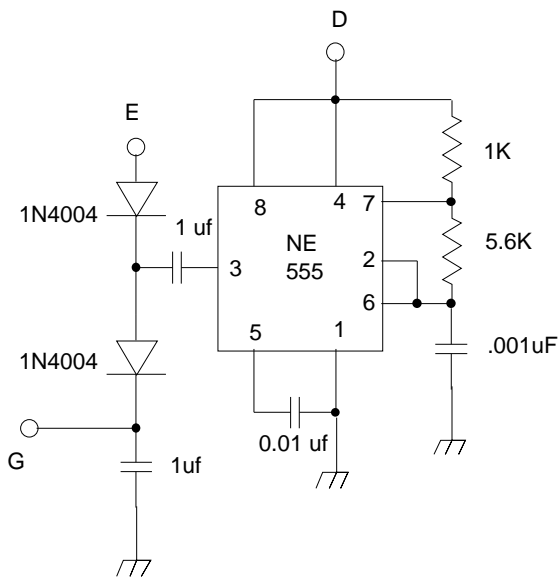
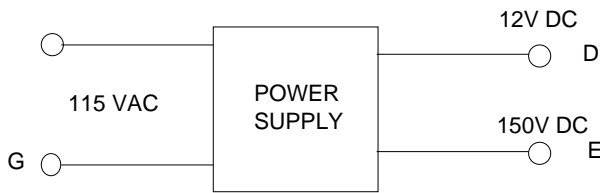


FIGURE 10
VOLTAGE ADDER CIRCUIT FOR ALL
N-CHANNEL POWER STAGE MOTOR DRIVER

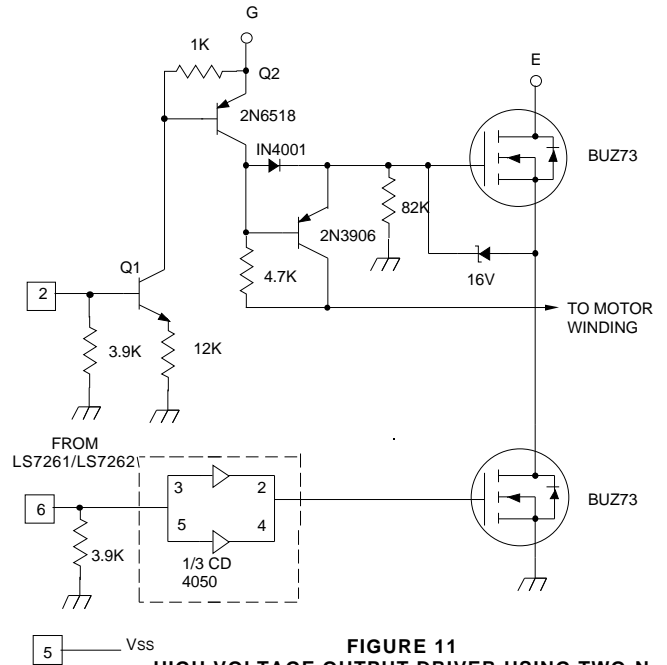


FIGURE 11
HIGH VOLTAGE OUTPUT DRIVER USING TWO-N
CHANNEL POWER FETS

EMULATOR

LSI COMPUTER SYSTEMS, INC. has developed an LS7263/LS7264 emulator for optimizing the circuit programmability for any 3 or 4 phase brushless DC motor. If none of the four different types of 3 phase speed controllers or the one type of four phase speed controller available from LSI COMPUTER SYSTEMS, INC. will exactly match specific motor requirements, then a new circuit can be programmed accordingly. The emulator has 15 thumbwheel switches for adjusting the output power transfer curve and switches for selection of sensor separation, 4 or 8 pole motors and tachometer division. The emulator provides all the interfacing circuitry found in the integrated circuit and is readily available.

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.