APPLICATION NOTE

TDA9965
CCD SIGNAL PROCESSOR

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Philips
Semiconductors

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TDA9965
CCD SIGNAL PROCESSOR

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1 INTRODUCTION

The TDA9965 is an analog to digital interface for CCD based cameras. This chip includes a clamp and track&hold block (CTH), a programmable gain amplifier (PGA), a calibration clamp loop and a 12-bits analog to digital converter (ADC). CTH bandwidth, PGA gain, ADC black reference and other control pulses polarities are programmed through a simple 3 wires serial interface.

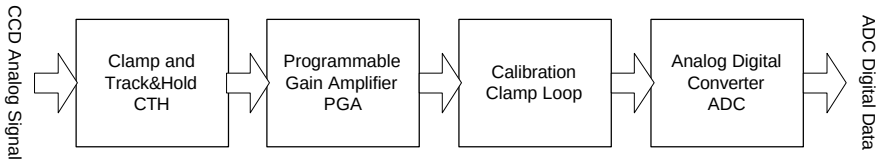

Figure 1. Philips CCD preprocessor features

2 CCD VIDEO SIGNAL

Light falling on CCD pixels generates charges, which are sensed with a capacitor. This sensing capacitor must be reset to a reference level thanks to a MOS switch before being filled with pixel's charges. The video signal is the voltage shift at the sensing capacitor.

The CCD output signal can be decomposed into three steps as described on Figure 2:

- First the sensing capacitor charge is initialized to supply voltage (20V typ.) through the R_{on} of the output MOS switch. It results in a reset peak often called *reset feedthrough level.*
- Then, when the switch is opening, the switch parasitic capacitor is put in parallel with the sensing capacitor, hence the reset voltage across those capacitors decreases to a level called *floating gate level*.
- At last, the sensing capacitor collects the electrical charges resulting from light integration. This is the active video.

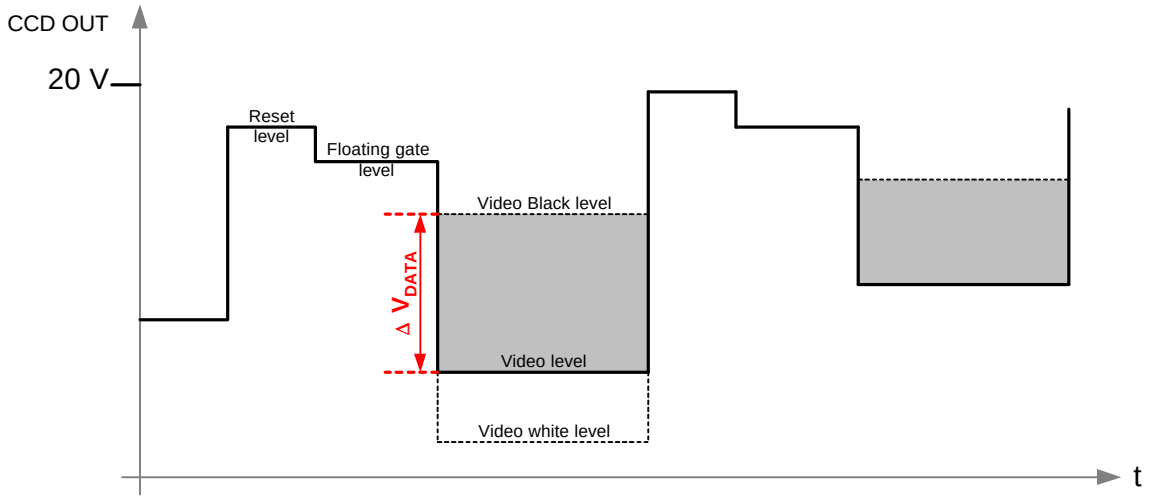

Figure 2. CCD video signal

3 INPUT BUFFER

The useful output data is the difference between the Black level and the Video level. It will be obtained thanks to the CDS stage which will store the analog Black and Video levels in two internal capacitors that are located at the device input.
Many competitors advise to use an external output buffer to drive those capacitors but taking care of the current needed (3 mA and more) and of the power supply (more than 15 V), you have to take into account more than 45 mW extra power consumption.
Thanks to its internal input buffer, TDA9965 doesn't need an additional external buffer in most cases. If the output of the CCD is high impedance -depending on the CCD type and on the connection length between CCD and the CDS input, only a very small external buffer will be needed.

4 CLAMP AND TRACK&HOLD (CTH)

4.1 The optical black clamp loop (CLPOB)

Usually the video level coming out of the CCD is not equal to the floating gate level even if no light has been collected by the pixel. Dark current and clock feedthrough noise cause this shift called ΔV_{BLACK} between floating gate level and what is called black level.

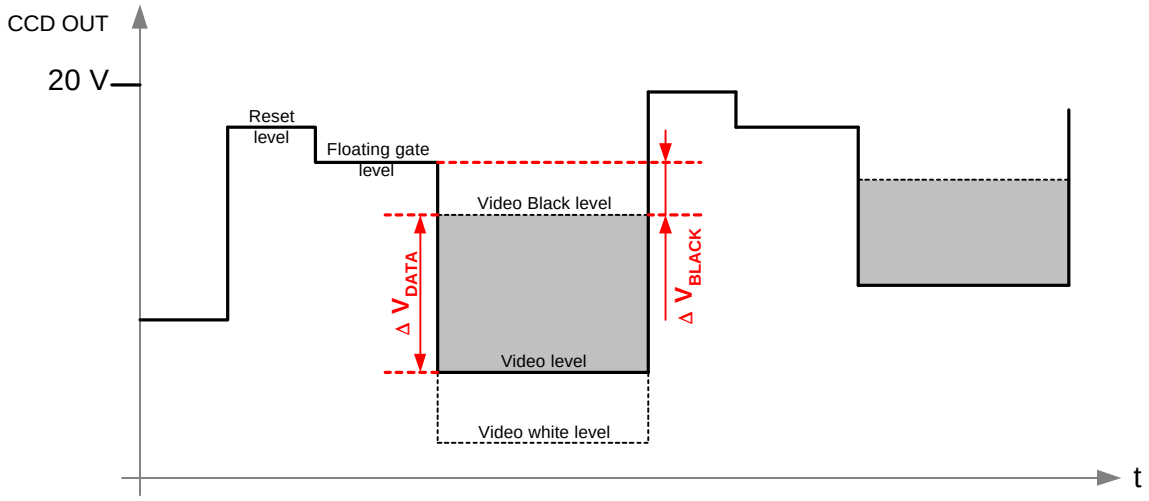

Figure 3. Black Offset and Data

This offset shouldn't be taken into account in video level to know what is the amount of light the pixel has collected. That is why it must be removed before amplification to preserve the video dynamic range, especially in low light conditions when ΔV_{DATA} could become smaller than ΔV_{BLACK}.

To remove the ΔV_{BLACK} level from the video signal, an optical black clamp loop circuitry is implemented inside the preprocessor. In the pixel stream coming out of the CCD, some pixels called "optical black pixels" are used as reference to measure ΔV_{BLACK}. The CLPOB signal indicates to the preprocessor that ΔV_{BLACK} calibration has to be done.

The principle is the following:

- The reference voltage REF32 is used as the internal black level. REF32 is generated by the regulator and has a typical value around 3.2 V.
- During CLPOB, the STGE capacitor is charged up to the moment when the output voltage of the CTH is equal to REF32. Then, the voltage on the STGE pin takes into account the offset ΔV_{BLACK}. A typical value on STGE is 2.4 V if there is no offset between the floating gate level and the video black level.

Depending on the application targeted, the capacitor associated with the black clamp loop (STGE) must be adjusted:

- To decrease clamp noise by a factor n, one can multiply by n^2 the clamp capacitor value.
- The charge current is fixed to around plus or minus 800 µA up to the moment the clamp capacitor voltage reaches its final value plus or minus 6 mV. Then the current depending on the voltage error on the capacitor is linear. In order to avoid oscillations, the clamp capacitor must be big enough to enter the linear area.
- Increasing the clamp capacitor value also increases the start up time of the system.

4.2 Track&Hold

4.2.1 Acquisition

The principle of Clamp and Track&Hold (CTH) is to measure the difference between the floating gate level and the video level (ΔV_{DATA}) and to remove the offset ΔV_{BLACK}.

The principle is the following (SHP and SHD pulses are indicated on Figure 4):

- On the SHP pulse, the voltage value stored in the STGE capacitor is applied via a buffer at the input pin INCCD. The typical value on INCCD is then 3.35 V if there is no offset between the floating gate level and the video black level. Then the CTH ouput value is equal to REF32, the internal black level (see Chapter 4.1). The voltage value on INCCD will be higher or lower if ΔV_{BLACK} differs from zero.
- During the transition at the CCD output, the input coupling capacitor transmits the voltage difference between the floating gate level and the video level on INCCD.
- On the SHD pulse, this new level is stored by he CTH and is transmitted at the CTH output where it is compared to REF32. Because the offset ΔV_{BLACK} has been taken into account during the SHP pulse the difference between REF32 and the CTH output is ΔV_{DATA}.

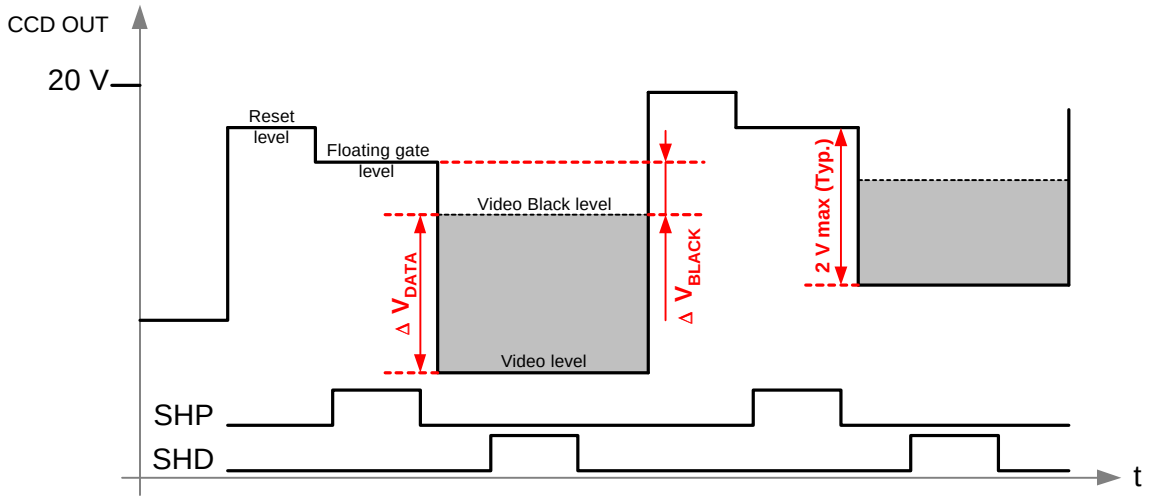

Figure 4. CCD signal sampling and limiting values

Sampling of floating gate and video levels should be adjusted to reach the best performances.

- The sampling pulses width should be as large as possible to reach the highest step transitions, especially for SHD. The SHP width is less critical because the CTH only refresh the input capacitor, which has a small value.
- The timings $t_{h(IN-SHP)}$ and $t_{h(IN-SHD)}$ must be respected. Those timings are due to the different processing delays of the CCD signal and of the SHP and SHD signals inside the chip.

4.2.2 Reset noise

The reset switch generates noise which results in a shift of the reset reference level, as described in Figure 5.

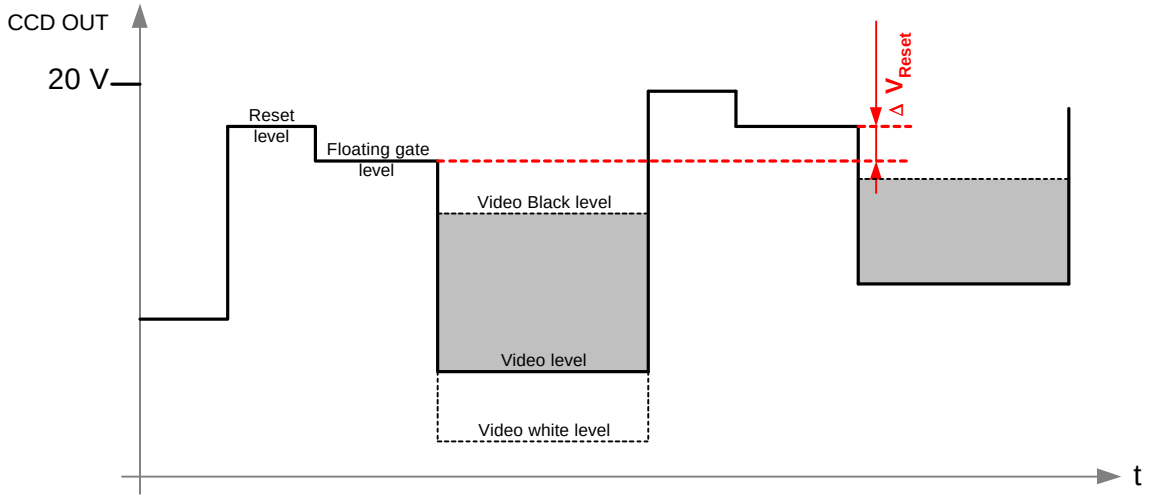

Figure 5. Reset noise effect on two consecutive pixels

This shift affects similarly the floating gate level and the video level but it differs from one pixel to the other. Because the CTH only measures the difference ΔV_{DATA}, it removes this offset and also every low frequency noise.

4.2.3 DC common-mode level

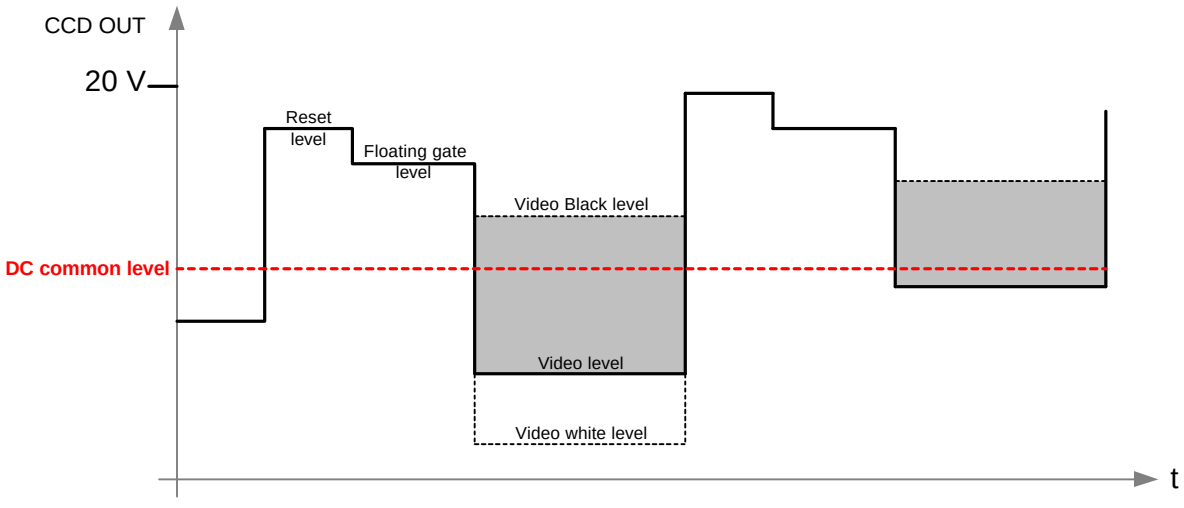

Figure 6. DC common-mode level of a CCD video signal

The common-mode level of the image sensor's output signal could range from 0 V to more than 10 V. Fortunately, the CTH structure requests the TDA9965 to ac-coupled with the CCD.

During the SHP pulse, the CTH restores the video black level to a typival value around 3.35 V, thanks to the serial capacitor, so the signal is automatically adjusted to a usable dc voltage.

5 ADC CLAMP LOOP (CLPADC)

The ADC Clamp Loop goal is to set an output code for the video black level. This code is programmed through the serial interface over 10 bits, from 0 to 1023 in steps of one ADC ouput LSB.

To set the clamp active during the black pixels will reach the best performance on ADC clamp loop. The clamp performance isn't guaranteed for an output code for the video black level under 32 or a PGA gain over 30 dB.

So the timing diagram and the signals' waveforms will be the following:

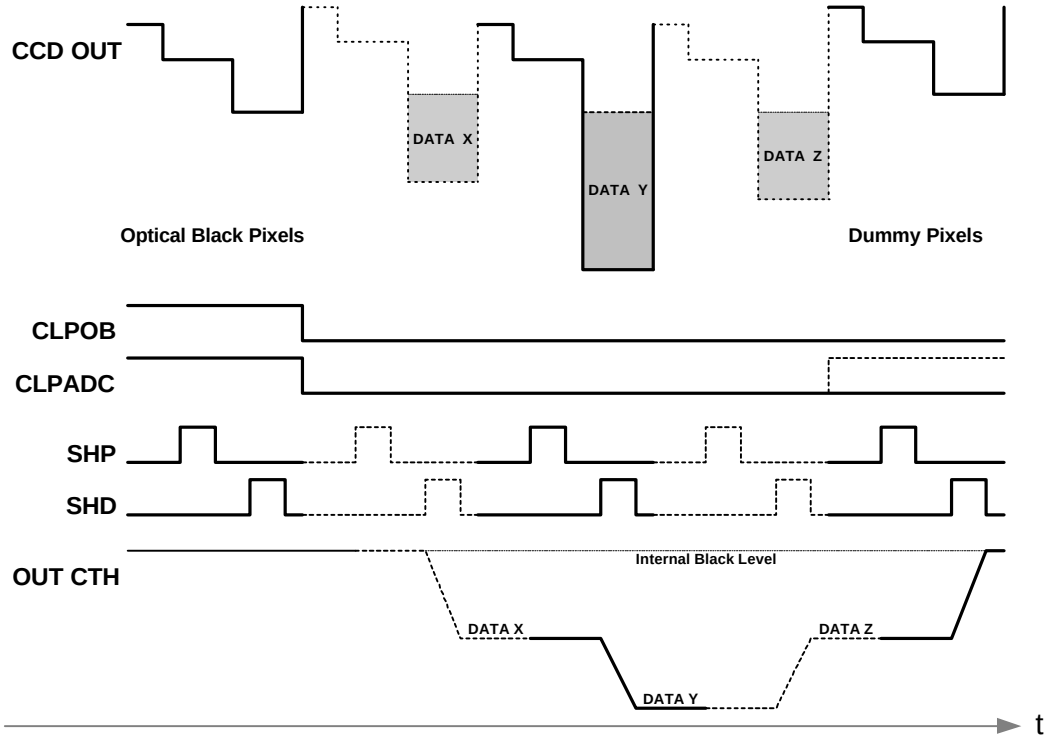

Figure 7. Timing diagram

6 PROGRAMMABLE GAIN AMPLIFIER

The goal of the PGA is to amplify the data obtained thanks to the CTH to use the maximum input range of the ADC. Full scale input (code 0 to 4095 at ADC output) will be reached with a ΔV_{DATA} of 2 V for the gain code 0. The desired gain setting is programmed via the 3 wires serial interface.

The equation of gain, described on Figure 8, is the following.

- For code between 0 and 767 : $Gain_{dB} = \left(\frac{Code}{767} * 36dB \right)$
- For code between 767 and 1023, gain is set to 36 dB

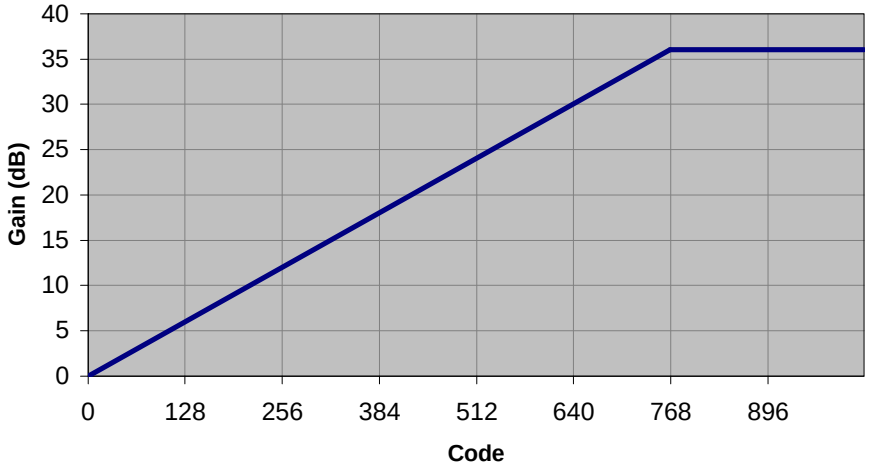

Figure 8. PGA Gain = f(Code)

The main characteristics of PGA are:

- Setting over 10 bits
- Gain range = 36dB
- Steps = 0.05dB

When the maximum ΔV_{DATA} value in V (DataMax) on a frame is known, the code to be set in order to have a full scale input is given by the following equation:

$$Code = \frac{20 \cdot \log\left(\frac{2V}{DataMax} \right)}{36dB} \cdot 767$$

7 START-UP

The start-up sequence is the following:

- First the regulator sets its reference voltages.
- Next the optical black clamp loop use REF32 to set the STGE voltage.
- At the end, the ADC clamp loop uses the result of the optical black clamp loop to set the Vref voltage.

7.1 Regulator start-up time

The regulator start-up time depends on the analog supply ramp-up time and the capacitor on REF32. To ensure a low clamp noise, a capacitor bigger than 100 nF is recommended on REF32.

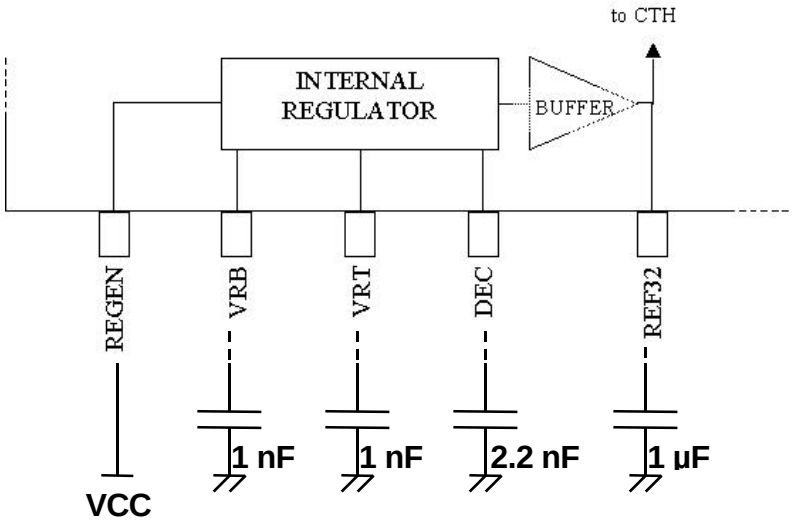

Figure 9. TDA9965 internal regulator and signals

In most cases, the Internal regulator charge will follow the analog supply ramp-up. In the worst case (ramp-up in less than 100 µs), an extra time of 200 µs must be added to the ramp-up time for a 1µF capacitor on REF32. So the worst start-up time is typically around 300 µs.

7.2 Settings

When the power supplies increase from zero to VCC, the init-on-power block initializes the circuit as follows:

- Cut-off freqency of the CTH circuit is set to: code $f_{co(CTH)} = 0$
- PGA gain control is set to: code $G_{PGA} = 0$
- Clamp code of the ADC is set to: code $ADC_{CLP} = 0$
- SHP and SHD sample on High level; CLKADC active with rising edge.
- CLPOB and CLPADC active on high level.

If the clock polarities are different in the application, the new settings should be registered through the serial interface before starting the clamp loops.

7.3 STGE start-up time

The STGE capacitor will be charged during the optical black clamp loop in three steps:

- if V(STGE) < 1.6 V (t0 to t1), the clamp will charge the capacitor automatically.
- if 1.6 V < V(STGE) < 2.4 V (t1 to t2), the clamp will charge the capacitor with a 700 µA current when CLPOB will be active.
- If V(STGE) reaches 2.4 V plus or minus 6 mV (t2 to t3), the clamp will charge the capacitor with a 115 µA/mV (referenced to 2.4 V) current when CLPOB will be active.

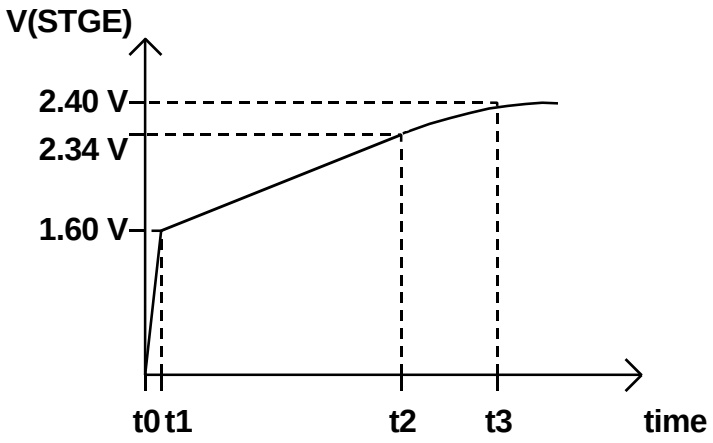

Figure 10. STGE start-up as a function of time

Then we have the following typical start-up time for STGE:

- C (STGE) = 47 nF ➔ t3 = 1µs + 68.5 µs + 1.5 µs
  t3 = 71 µs (*)
- C (STGE) = 100 nF ➔ t3 = 142 µs (*)

(*) This time supposes the supplies are able to drive the needed current between t0 and t1.

7.4 Vref start-up time

The Vref capacitor will be charged during the ADC clamp loop in three steps (example with code ADC_{CLP} = 128):

- if V(Vref) < 1.0 V (t0 to t1), the clamp will charge the capacitor automatically.
- if 1.0 V < V(Vref) < 1.58 V (t1 to t2), the clamp will charge the capacitor with a 400 µA current when CLPADC will be active.
- If 1.58 V < V(Vref) < 1.61 V (t2 to t3), the clamp will charge the capacitor with a 50 µA current when CLPADC will be active.

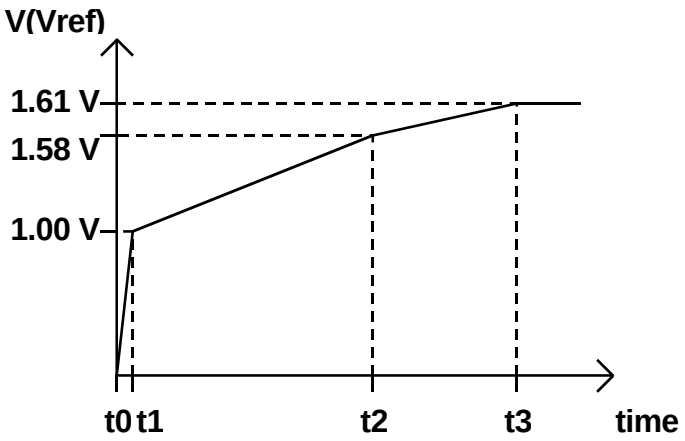

Figure 11. Vref start-up as a function of time

Then we have the following typical start-up time for Vref:

- C (Vref) = 47 nF ➔ t3 = 2µs + 72.5 µs + 30 µs
  t3 = 104.5 µs (*)
- C (Vref) = 100 nF ➔ t3 = 209 µs (*)

(*) This calculation supposes the supplies are able to drive the needed current between t0 and t1.

When we add all the start-up times, we obtain a total start-up time around 700 µs.

8 INPUT STAGE ATTENUATION

The TDA9965 input stage is equivalent to a high-pass filter C-R. Because the coupling capacitor is small, the signal is attenuated after the input stage.

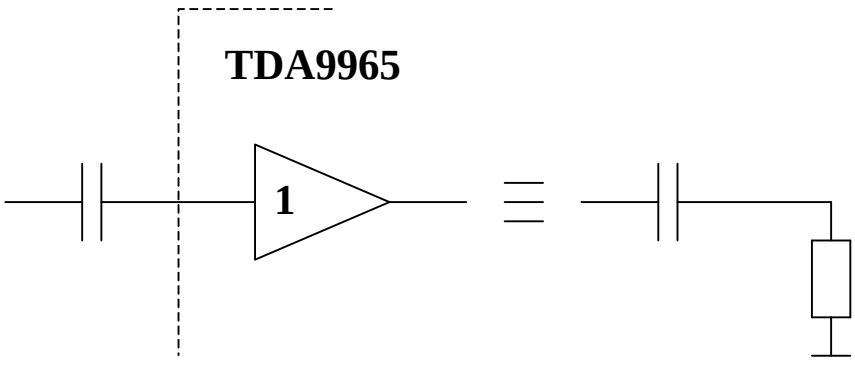

Figure 12. TDA9965 input buffer equivalence

This attenuation can move from 5 % to 15 %, mainly depending on the coupling capacitor value. The higher the capacitor will be, the smaller the attenuation will be.

9 LAYOUT AND IMPLEMENTATION INFORMATION

The TDA9965 is a high speed and high precision analog circuitry combined with an analog to digital converter. To get the best performances this IC has to be treated as an analog component and should be properly decoupled from wideband noise generated by digital circuitry:

- For the front end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be taken into account, particularly with respect to power and ground connections.
- The connection between CCD interface and CDS input should be as short as possible and a ground ring protection around this connection can be beneficial. It is recommended to protect the input signal with a shield made of a clean ground which will be connected to input pins 1 and 3.

Separate analog and digital supplies provide the best performance. If it is not possible to do this on the board then the analog supply pins must be decoupled effectively from the digital supply pins with 0.1µF ceramic chip capacitors. The decoupling capacitors must be placed as close as possible to the IC package. Short leads length and low ground impedance are important to reach the best performance.

In a two-ground system, in order to minimize the noise through the package and die parasitics, the following recommendation must be implemented:

- The ground pin associated with the digital outputs must be connected to the digital ground plane and special care should be taken to avoid feedthrough in the analog ground plane. The analog and digital ground planes must be connected together with an inductor as closely as possible to the IC in order them to have the same dc voltage.
- The digital output pins and their associated lines should be shielded by the digital ground plane which can then be used as a return path for the digital signals.

Special care has to be taken when driving inputs with high-speed digital ICs. Due to their very high slew rate, high-speed digital circuits generate high frequencies. Those, due to bad impedance matching, are able to generate overshoots and undershoots beyond power supply potentials. In general adding resistors in series with digital signals will remove offending transients and prevent them from disturbing internal circuitry.

The digital lines that this IC will have to drive towards the DSP may be highly capacitive. In this case high intensity instantaneous current will flow through output buffers to charge the parasitic capacitance. Those currents could feed back into the analog region and affect the performances of the circuit. Either using damping resistors or buffers in series with each data line may help to reduce the surge current.

In case of the use of several devices with only one regulator for all of them, special care has to be taken to connect together the regulator pins V_{RB} (respectively V_{RT}, REF32) of the devices.

- Because REF32 is used internally as the black level reference, this signal must be protected from the noise of the others signals and the board.

- Because V_{RT} from the active regulator will drive a lot of current (up to 8 mA for each TDA9965), resistive connections should be avoided.
- It is recommended to add decoupling capacitors for each TDA9965 on the pins V_{RB}, V_{RT} and REF32.

10 APPLICATION DIAGRAM

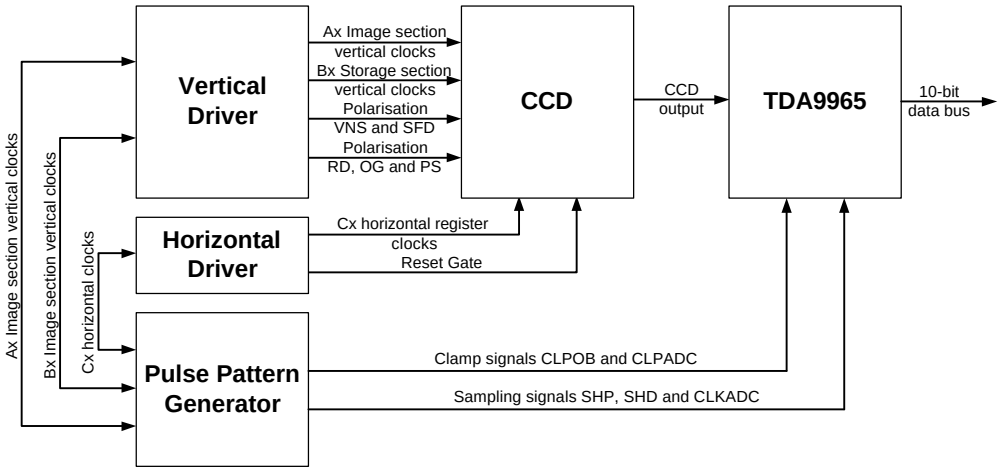

Figure 13. Imaging chipset example

11 LIST OF FIGURES

GLOSSARY

AC Alternative Current
ADC Analog to Digital Converter
CCD Charge Coupled Device
CDS Correlated Double Sampling
DC Direct Current / Continuous level
PGA Programmable Gain Amplifier
DN Digital Number