Junction Field Effect Transistors

InterFET Application Notes

Introduction

The field effect transistor was actually conceived before the more familiar bipolar transistor. Due to limited technology and later the rapid rise of the bipolar device it was not pursued until the early 1960's as a viable semiconductor alternative. At this time further investigation of the field effect transistor and advances in semiconductor process technology lead to the types in use today.

Field effect transistors include the Junction FET (JFET) and the MOSFET. The MOSFET is a metal-oxide semiconductor technology and is sometimes referred to as the IGFET or Insulated Gate FET. All field effect transistors are majority carrier devices. This means that current is conducted by the majority carrier species present in the channel of the FET. This majority carrier consists of hole for p-channel devices and electrons for n-channel devices. The JFET operates with current flow through a controlled channel in the semiconductor material. The MOSFET creates a channel under the insulated gate region which is produced by an electric field induced in the semiconductor by applying a voltage to the gate. The JFET is a depletion mode device whereas the MOSFET can operate as a depletion mode or an enhancement mode device. Depletion mode devices are controlled by depleting the current channel of charge carriers. Enhancement mode devices are controlled by enhancing the channel with additional charge carriers.

The JFET

The junction field effect transistor in its simplest form is essentially a voltage controlled resistor. The resistive element is usually a bar of silicon. For an N-channel JFET this bar is an N-type material sandwiched between two layers of P-type material. The two layers of P-type material are electrically connected together and are called the gate. One end of the N-type bar is called the source and the other is called the drain. Current is injected into the channel from the source terminal, and collected at the drain terminal. The interface region of the P- and the N-type materials forms a P-N junction as shown in Figure 1.

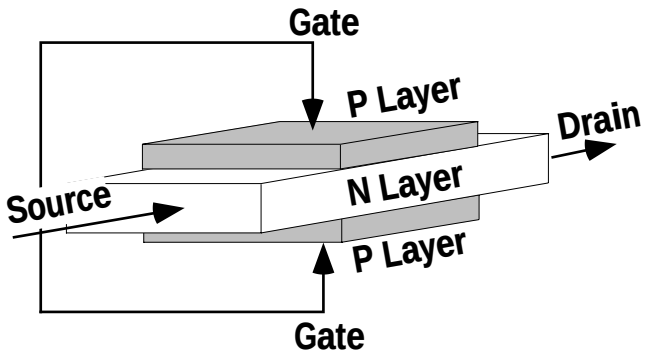


Figure 1

As in any material, the resistance of the conducting channel is defined by:

(1) $R = \rho l / A$

where R = total channel resistance

ρ = resistivity of the silicon

l = length of the conducting path

A = cross sectional area of the conducting path

Figure 2 illustrates a JFET with the two gate areas electrically connected together, as are the source and the drain. Application of a reverse bias voltage on the drain/gate terminals results in the formation of depletion regions at the PN junction. Increasing the voltage causes the depletion regions to reach further into the channel and effectively reduces its cross-sectional area. It can be seen from Equation 1 that this increases the channel resistance. Continuing to increase the voltage will result in the depletion regions touching in the middle of the channel. The channel is then said to be pinched off and the voltage required to cause this is called the pinch-off voltage.

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375
www.interfet.com

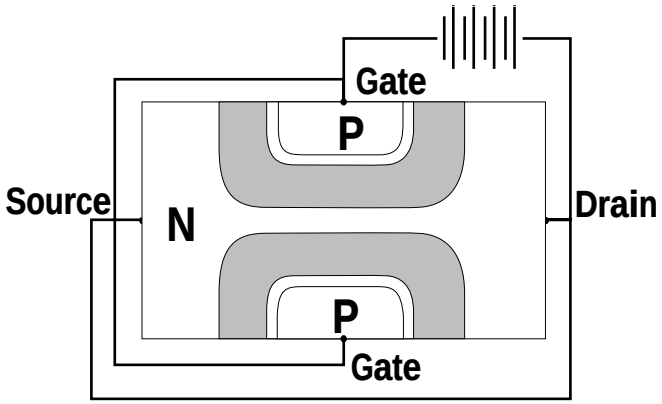


Figure 2

Connecting the gate to the source and applying a voltage between the drain and source also produces the formation of a depletion region at the PN junction. The depletion region is then concentrated at the drain end of the channel, as shown in Figure 3. Once again, increasing the voltage causes the depletion region to spread farther into the channel. This results in a corresponding increase in channel resistance due to the reduction in the cross sectional area of the channel. The voltage at which the two depletion regions just touch in the middle of the channel is called the drain saturation voltage. Operation of the JFET at voltages below and above the drain saturation voltage are referred to the linear (or resistive) and saturation regions, respectively. When operated in the saturated region, changes in voltage cause little change in channel net current. The amount of current which will flow in the channel of a JFET operating in this manner is called the drain saturation current. The JFET is normally operated in the saturated region when used as an amplifier.

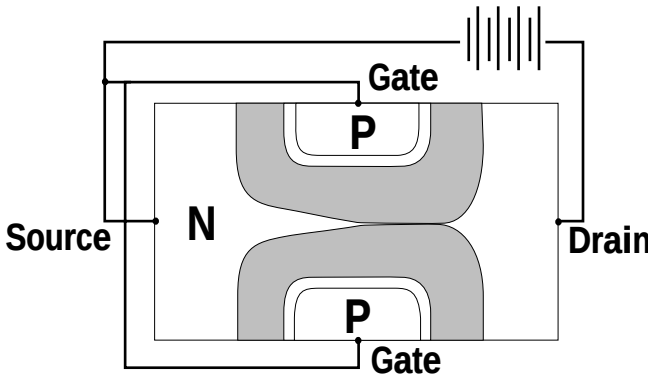


Figure 3

The application of an additional voltage between the gate and the source in reverse bias condition causes the depletion region to become more evenly distributed throughout the channel. This further increases the channel resistance and reduces the amount of channel current with a given drain voltage. Continuing to increase the gate voltage to the pinchoff point will reduce the drain current to a very low value, effectively zero. This illustrates the operation of the JFET by showing that a voltage modulation of the gate results in a corresponding drain current modulation.

A typical set of JFET characteristic curves is shown in Figure 4. The three primary regions shown on the graph are the linear region, the saturated region, and the breakdown region. The linear region is that region where the drain to source voltage is less than the drain saturation voltage. It can be seen that the voltage current relationship is a linear function. At the point where the drain to source voltage reaches the drain saturation voltage, the saturated region begins. The curves illustrate that increasing the gate reverse voltage reduces the drain current as well as the drain saturation voltage. This also shows the manner in which the drain current is modulated when modulating the gate voltage. The final region of interest is the breakdown region. This is the point at which

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

the gate to drain reverse biased depletion region breaks down due to the voltage applied and the current is no longer blocked. When operated in this manner the current flow is essentially uncontrolled and the device could be damaged and destroyed.

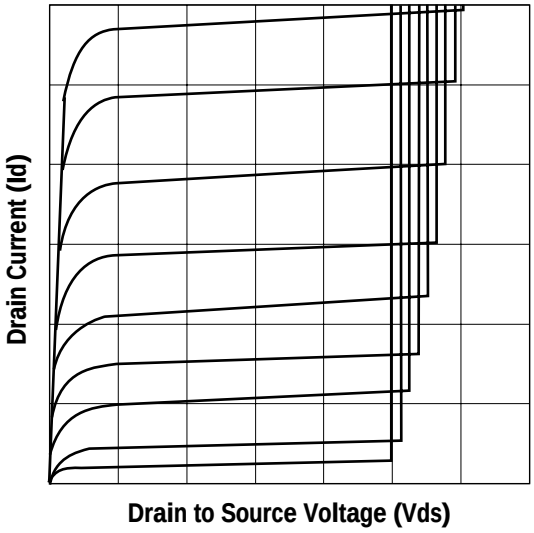


Figure 4

A typical set of JFET characteristic curves.

Conclusions

The previous discussion of the JFET illustrates that:

1. The JFET is basically a voltage controlled resistor,
2. The JFET operates as a depletion mode device, and,
3. The JFET performs as a voltage controlled current amplifier.

The JFET is preferred in many circuit applications due to its high input impedance because it is a reverse biased PN junction. Its operation is that of the flow of majority carriers only and therefore acts as a resistive switch. It also is inherently less noisy than bipolar devices and can be used in low signal level applications.

References:

1. Millman, J. and Halkias, C.: *Integrated Electronics Analog and Digital Circuits and Systems*, McGraw-Hill Book Company, New York, 1972
2. Sevin, L.J.: *Field Effect Transistors*, McGraw Hill Book Co., New York, 1965
3. Grove, A.S.: *Physics and Technology of Semiconductor Devices*, John Wiley And Son, New York, 1967
4. Grebene, A.B.: *Analog Integrated Circuit Design*, Van Nostrand Reinhold, New York, 1972
5. Pierce, J.F. and Paulus, T.: *Applied Electronics*, Charles E. Merrill, Columbus, Ohio, 1972

Introduction

The Junction Field Effect Transistor (JFET) exhibits characteristics which often make it more suited to a particular application than the bipolar transistor. Some of these applications are:

High Input Impedance Amplifier
Low-Noise Amplifier
Differential Amplifier
Constant Current Source
Analog Switch or Gate
Voltage Controlled Resistor

In this application note, these applications, along with a few others, will be discussed. Only the basics will be shown without going into too much technical detail.

Basic JFET Amplifier Configurations

There are three basic JFET circuits: the common source, the common gate, and the common drain as shown in Figure 1. Each circuit configuration describes a two port network having an input and an output. The transfer function of each is also determined by the input and output voltages or currents of the circuit.

Common Source

Common Gate

Common Drain

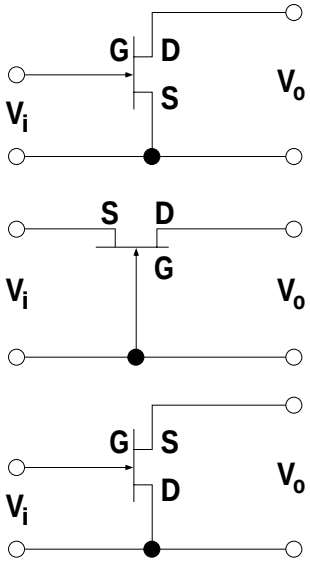


Figure 1

Basic JFET Amplifier Circuit Configurations

The most common configuration for the JFET as an amplifier is the common source circuit. For an N-channel device the circuit would be biased as shown in Figure 2

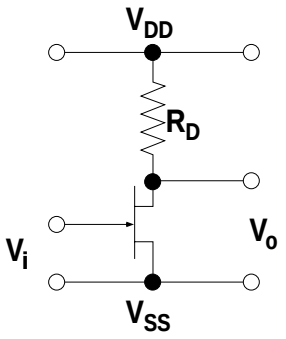


Figure 2

Basic Common Source Amplifier Circuit Biasing Configuration

Since the N-Channel JFET is a depletion mode device and is normally on, a gate voltage which has a negative polarity with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by a single positive power supply using the self biasing method shown in Figure 3. This is accomplished by the voltage which is dropped across the source resistor, Rs, according to the current flowing through it. The gate-to-source voltage is then defined as:

(1) $V_{GS} = I_D \times R_S$

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

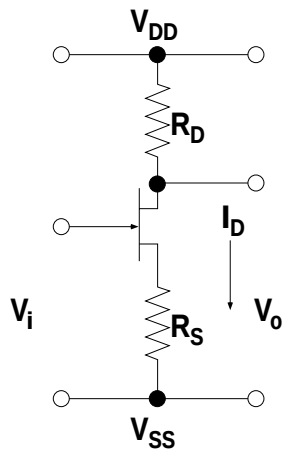


Figure 3

Common Source Amplifier
Using VGS Self-Biasing Method

The circuit of Figure 3 also defines a basic single stage JFET amplifier. The source resistor value is determined by selecting the bias point for the circuit from the characteristic curves of the JFET being used. The value of the drain resistor is then chosen from the required gain of the amplifier and the value of the drain current which was previously selected in determining the gate voltage. The value of this resistor must also allow the circuit to have sufficient dynamic range, or voltage swing, required by the following stage. The following stage could be anything from another identical circuit to a loud speaker for an audio system. The voltage gain of this circuit is then defined as:

(2) $A_V = (g_m \times Z_l) / (1 + g_m \times R_S)$

where A_V = the voltage gain

g_m = the forward transconductance or gain of the JFET

Z_l = the equivalent load impedance

R_S = the value of the source resistor

The effect of the source resistor on the gain of the circuit can be removed at higher frequencies by connecting a capacitor across the source resistor. This then results in an amplifier which has a gain of:

(3) $A_V = g_m \times Z_l$

but only at frequencies above that defined by the resistor-capacitor network in the source circuit. This frequency is defined as:

(4) $f_{lo} = 1 / (2\pi \times R_S \times C_S)$

where f_{lo} = the low frequency corner

π = the constant 3.1418

R_S = the value of the source resistor in ohms

C_S = the value of the source capacitor in farads

This circuit also has a high input impedance, generally equal to the value of the input impedance of the JFET.

A Low-Noise Amplifier

A minor change to the circuit of Figure 3 describes a basic single stage low-noise JFET amplifier. Figure 4 shows that this change only incorporates a resistor from the gate to Vss. This resistor supplies a path for the gate leakage current in an AC coupled circuit. Its value is chosen by the required input impedance of the amplifier and its desired low-noise characteristics. The noise components of this amplifier are the thermal noise of the drain and gate resistors plus the noise components of the JFET. The noise contribution of the JFET is from the shot noise of the gate leakage current, the thermal noise of the channel resistance, and the frequency noise of the channel. These noise characteristics are generally lower than those found in bipolar transistors if the JFET is properly selected for the application. The voltage gain of the circuit is again defined by Equation (3).

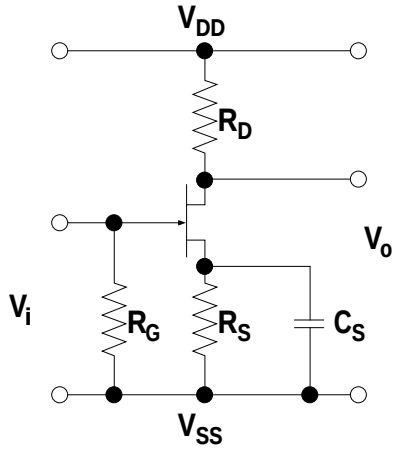


Figure 4

Low-Noise JFET Single Stage Amplifier with Source By-Pass Capacitor, CS

The JFET Differential Amplifier

Another application of the JFET is the differential amplifier. This configuration is shown in Figure 5. The differential amplifier requires that the two transistors be closely matched electrically and physically located near each other for thermal stability. Either input and either output can be used or both inputs and only one output and conversely only one input and both outputs can be used. For the configuration shown the source resistor is chosen to determine the gate to source bias voltage, remembering that the current will be twice that of each of the JFET drain currents. The value of the drain resistors is chosen to provide a suitable dynamic range at the output. The gain of this circuit is defined by:

(5) $A_V = 2x\ (g_m \times R_l) / (1 + g_m \times R_S)$

where all the terms in the equation have previously been defined.

This circuit configuration is very useful as a high input impedance stage to be connected to the input of a low cost operational amplifier, such as the popular 741 Op-Amp

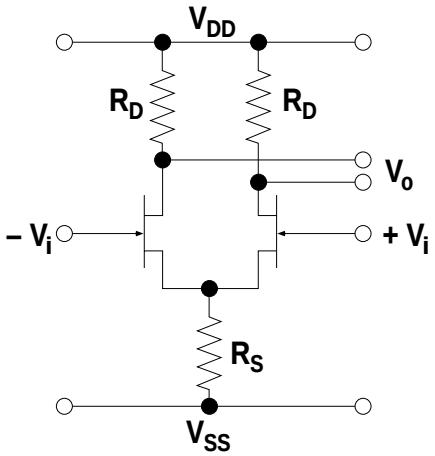


Figure 5

The Matched Pair JFET Differential Amplifier

The JFET Constant Current Source

A constant current source using a JFET is shown in Figure 6. This circuit configuration has many useful applications ranging from charging circuits for integrators or timers to replacing the source resistor in the differential amplifier shown in Figure 5. The current provided by the constant current source of Figure 6 is defined as

(6) $I_D = I_{DSS}\ [1 - (V_{GS} / V_p)]^2$

where I_D = the drain current or magnitude of current sourced

I_{DSS} = the drain saturation current of the JFET

V_{GS} = $I_D \times R_S$

V_p = the JFET pinch-off voltage

2 = the squared value of the term in brackets.

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

It can be readily seen that the use of this circuit in the source circuit of the differential amplifier of Figure 5 would improve the circuit voltage gain as well as reduce the amplifier noise and enhance the CMRR of the amplifier.

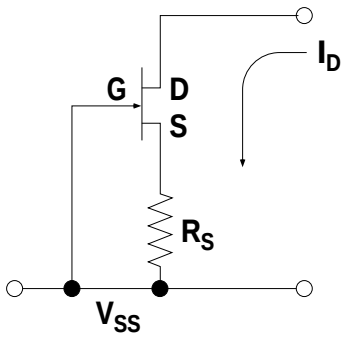


Figure 6

JFET Constant Current Source

The JFET Analog Switch

Figures 7, 8, and 9 show three different applications for the JFET to be used as an analog switch or gate. Figures 7 and 8 both demonstrate methods for realizing programmable gain amplifiers, while Figure 9 shows an analog multiplexer circuit using JFETs and a common op-amp integrated circuit.

It can be seen from Figure 7 that the gain of the stage can be changed by switching in any combination of feedback resistors R1 through Rn. The JFET in series with the input resistor should be of the same type as those in the feedback paths and is used for thermal stability of the circuit gain. The transfer function of the circuit of Figure 7 is approximated by:

(7) $V_o / V_i = 1 / [(1 / R_1) + (1 / R_2) + ... + (1 / R_n)] / R_i$

where R_1 through R_n = the feedback resistors

R_i = the input resistors

V_o = the output voltage

V_i = the input voltage

Note that only those feedback resistors which are switched into the circuit are to be included in the the transfer function equation.

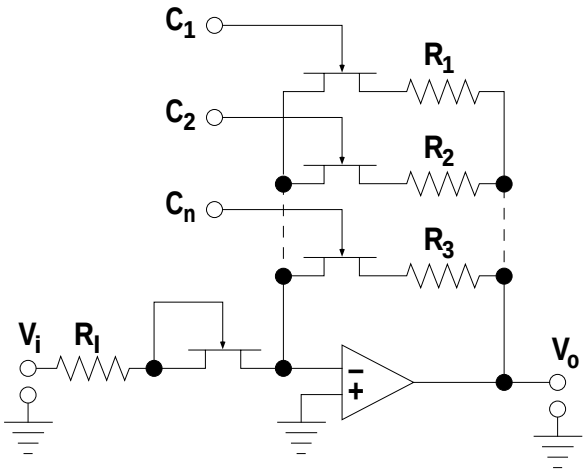


Figure 7

Programmable Gain Amplifier

The circuit of Figure 8 shows another method to realize a programmable gain amplifier using a common op-amp, four resistors, and only two JFETs. The gain of this circuit can also be changed by switching in the desired resistors by turning off the appropriate JFET thus switching in the parallel resistor. The transfer function of this circuit is approximated by:

(8) $V_o / V_i = (R_3 + R_4) / (R_1 + R_2)$

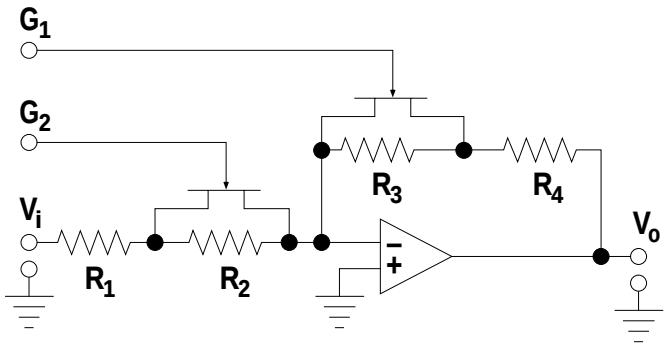


Figure 8

Programmable Gain Amplifier with 4 Resistors and 2 JFETs

It should be noted that only those resistors which are switched into the circuit are to be included in the transfer function equation.

Figure 9 shows a circuit in which the JFETs are acting as analog switches to multiplex several input signal sources to a single output source. The transfer function of this circuit is then approximated by:

(9) $V_o / V_i = R_f / R_n$

where R_f = the feedback resistor

R_n = any one of the input resistors

Further examination of this circuit shows that it can also be used as a programmable summing amplifier by switching in any combination of input signals. The transfer function is then approximated by:

(10) $V_o / V_i = (R_f / R_1) + (R_f / R_2) + ... + (R_f / R_n)$

Again in this application only those resistors which are switched into the circuit are to be included in the transfer function equation.

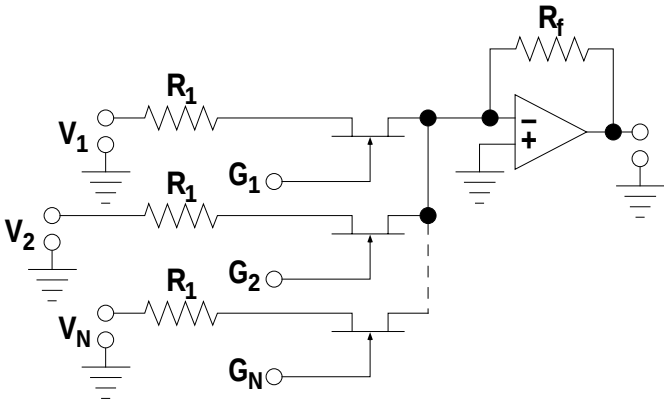


Figure 9

Analog Multiplexer Circuit which can also be used as a Programmable Summing Amplifier

The JFET Voltage Controlled Resistor

Another common application for the JFET is as a voltage controlled resistor. The JFET action in normal operation simply changes the cross sectional dimensions of the channel. When the JFET is biased in the resistive or linear region as shown in Figure 10, a change in gate voltage and the corresponding change in channel dimensions simply changes the drain to source resistance of the device.

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

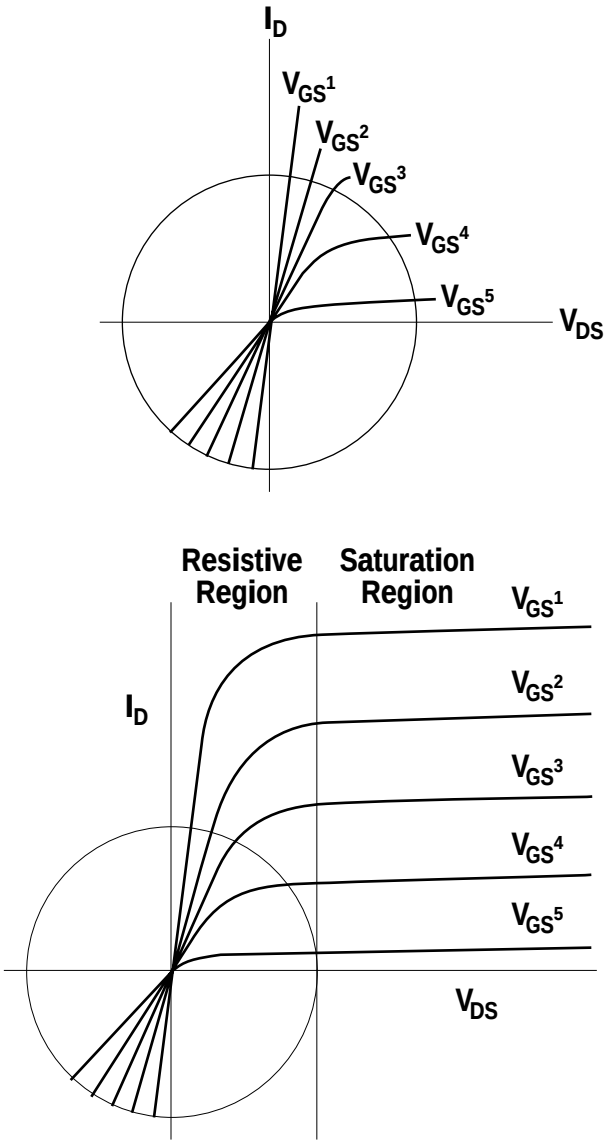


Figure 10

JFET Family of Characteristic Curves of I_D vs. V_{DS} and V_{GS}

Figure 11 depicts a JFET being used as a voltage controlled resistor (VCR). The resistance is determined from the bias point conditions selected from the curves of Figure 10. The resistance is then defined as

(11) $R_{DS} = V_{DS} / I_{DS}$

where R_{DS} = the drain to source resistance

$V_{DS} = V_o$ or the output voltage

I_{DS} = the drain current

It can readily be seen from the curves of Figure 10 that any change in the input voltage (Vi) or the gate to source voltage will cause a corresponding change in the drain current. Equation (11) indicates that there is a corresponding change in the drain to source resistance (RDS). Therefore, the resistance is controlled by the voltage applied to the gate, resulting in a voltage controlled resistor.

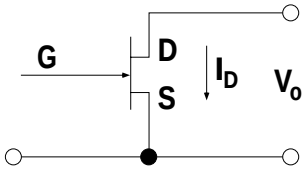


Figure 11

JFET used as a Voltage Controlled Resistor, where $R_{DS} = V_o / I_D$

Conclusions

This application note describes several useful junction field effect transistor circuit configurations. The high input impedance and low-noise circuits are often used as input stages to voltage measurement instruments such as oscilloscopes and digital volt meters.

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375
www.interfet.com

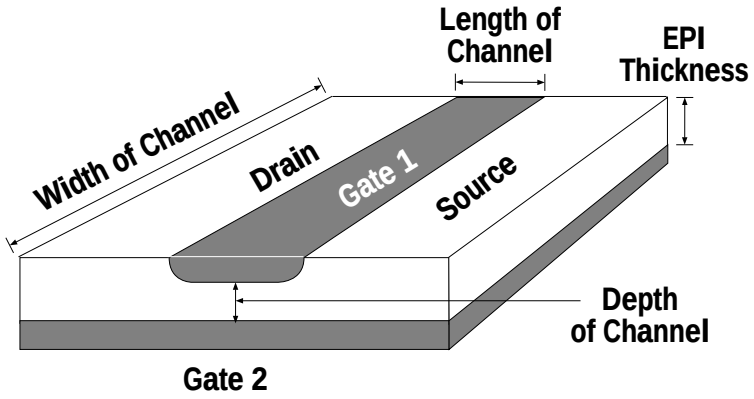
The differential amplifier is a very widely used circuit in applications where the difference between two voltages is to be measured, such as the input stage of an operational amplifier. The use of JFETs in this application provides high input impedance and low input leakage current. Constant current sources have many uses such as setting bias conditions for many other circuits in a system and as charging circuits for integrators and timing circuits. The analog switch is most often used in an analog multiplexer and in sample and hold circuits. Voltage controlled resistors are normally found in automatic gain control circuits and voltage controlled tuning circuits.

Therefore it is clearly seen that many applications for Junction Field Effect Transistors exist. Those discussed in this application note have many variations, refinements, and other uses. It should be noted that these applications were described in the simplest detail and additional study of the particular application should be considered before using any of the circuits presented.

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

JFET Parameter - Geometry Relationships

InterFET Application Notes



Increasing Dimension will (Inc)rease, (Dec)rease, or have Ø Effect		Channel Length	Channel Width	Channel Depth	EPI Thickness	EPI Resistivity
Breakdown Voltage	BV_{GSS}	Dec	Ø	Ø	Inc	Inc
Transconductance	G_m	Dec	Inc	Inc	Dec	Dec
Max Drain Current	I_{dss}	Dec	Inc	Inc	Dec	Dec
Pinch Off Voltage	V_p	Ø	Ø	Inc	Ø	Ø
ON Resistance	r_{ds}	Inc	Dec	Dec	Inc	Inc
Input Capacitance	C_{iss}	Inc	Inc	Ø	Inc	Dec
Gate Leakage	I_{gss}	Inc	Inc	Ø	Ø	Ø
Short Circuit Input Noises	eN	Inc	Dec	Dec	Inc	Inc
Input Current Noise	I_n	Inc	Inc	Ø	Ø	Inc

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375
www.interfet.com