[3] Power MOSFET in Detail

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1. Part Number Format (transistors and accessories)

1.1 Transistors

(example) 2SK 2232 A
1st 2nd 3rd

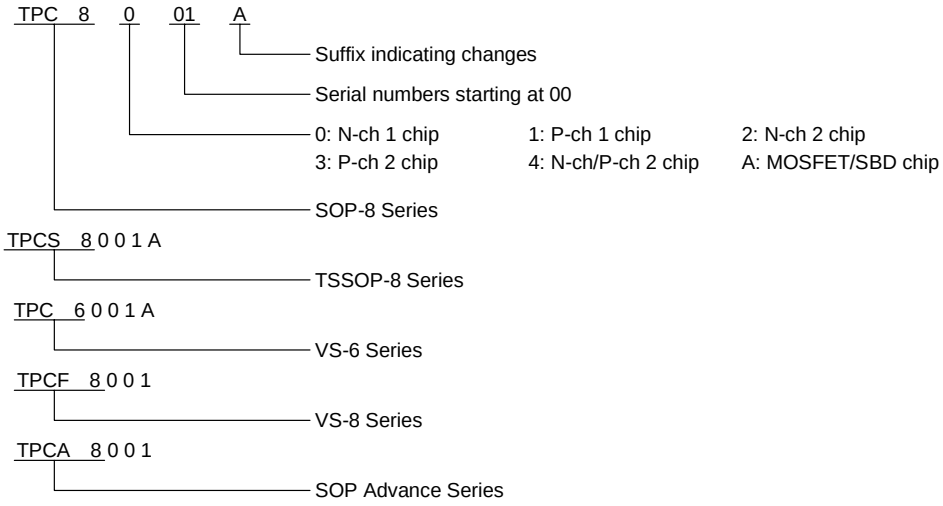
1st group: transistor types are indicated as shown in the table immediately below.

1st character group	Type
2SJ	P-channel field effect transistor
2SK	N-channel field effect transistor

2nd group: serial numbers starting at 11 (JEITA)

3rd group: suffix indicating changes (alphabetical order)

1.2 Multipin Transistors



1.3 Accessories

(example) AC 23 A
1st 2nd 3rd

1st group: AC.... accessory

2nd group: serial numbers

3rd group: suffix indicating changes

2. Construction and Characteristics

Since Power MOSFETs operate principally as majority carrier devices, adverse influences are relatively small magnitude or importance. This is in contrast to the situation with minority carrier devices, bipolar transistors, where such effects create more serious design problems. Also, the input impedance of power MOSFETs is basically higher than that of junction type FETs.

Even though the power MOSFETs have high speed, at the beginning of their development it was thought to be difficult to make devices characterized by low resistance, high breakdown voltage and high power. However, in recent years power MOSFETs from 60 V/70 A to 1000 V/12 A become available and are widely used as ideal switching devices.

2.1 Power MOSFET Construction

Power MOSFETs are classified into three major types as shown in Figure 2.1.

Figure 2.1 (a) shows a type of construction which is an extension of the small-signal MOSFET and with which high breakdown voltage is obtained using ion junction technology and the offset gate construction. However, this approach is disadvantageous from the viewpoint of the long channel required and the consequent loss in efficiency of surface area utilization.

Figure 2.1 (b) shows the product of a method called D-MOS (double diffusion MOS) which is used to form the channels by using double diffusion. High breakdown voltage can be obtained by using this technology.

This D-MOS construction uses double diffusion on a high-resistance drain substrate, which diffuses the gate area and the source area. The difference in depth of diffusion between the gate and the source area is used as the channel. When the gate-drain junction is formed in this way, there are fewer impurities on the drain side.

When drain voltage is applied, the depletion area extends considerably to the drain side but cannot easily extend to the channel side; therefore, breakdown voltage drop due to punch-through is prevented, and this structure makes possible high breakdown voltage even with an extremely short channel.

D-MOS takes the drain electrode from the back surface of the substrate, achieving high integration and high power. In addition, the cascade connection of a power MOSFET and a junction FET makes it possible to reduce the reverse transfer capacitance of the power MOSFET.

High breakdown voltage and large current are easier to achieve with this D-MOS construction than with the former two methods Figure 2.1 (a) and (c). Mass production at low cost is also possible; therefore, the technique portrayed in Figure 2.1 (b) is now widely used as the basic construction for power MOSFETs for ordinary power amplification applications.

Figure 2.1 (c) is the trench power MOSFET structure. High-integration is achieved by connecting channel vertically and this structure is capable of low ON-resistance.
Low-voltage power MOSFETs use this structure.

(a) Lateral construction (b) Double diffusion construction (c) Trench construction

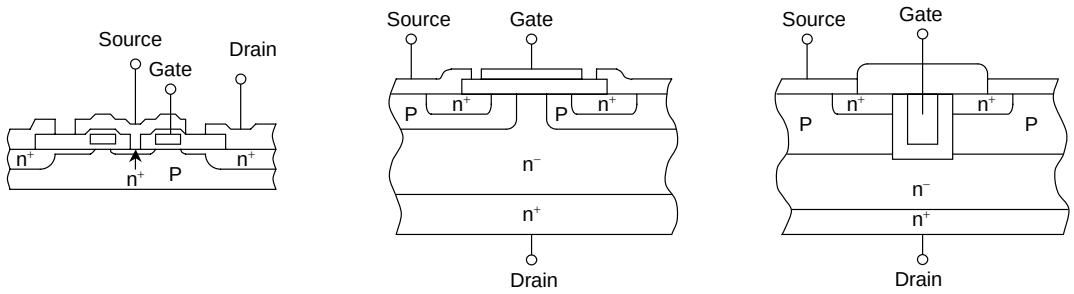


Figure 2.1 Power MOSFET Construction

2.2 Power MOSFET Features

Main features of power MOSFETs are shown as follows:

a) MOS type FETs are basically majority carrier devices; consequently, they differ greatly from bipolar transistors which are minority carrier devices.

b) MOS type FETs are not current controlled devices as are bipolar transistors. They are voltage controlled devices and are controlled by the voltage applied between the gate and source.

c) Since they are majority carrier devices, high-frequency switching operation is possible because there is no storage time-lag due to the carrier storage effect.

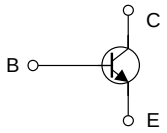
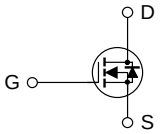
d) With bipolar transistors, current concentration occurs in the high-voltage area and junction failure occurs due to secondary breakdown. Therefore, bipolar transistors require considerable derating. Power MOSFETs, on the other hand, have a negative temperature coefficient which makes it difficult for secondary breakdown to occur, making these devices highly resistant to failure and thus enabling use right up to the maximum rating.

e) When power MOSFETs are used for switching operations, their switching times, that is, the rise and fall times, of power MOSFETs are one order of magnitude faster than those of bipolar transistors; therefore, turn-ON and turn-OFF loss are much smaller than those of bipolar transistors.

Incidentally, the ON resistance of power MOSFETs has a positive temperature coefficient; therefore, heat sink and thermal expansion design is necessary, taking into consideration the $R_{DS\ (ON)}$ at high temperatures.

Table 2.1 shows a comparison between bipolar transistor and MOSFET as to drive method, switching time, safe operation area, breakdown voltage, ON voltage, parallel connection and temperature stability.

Table 2.1 Comparison between Bipolar Power Transistors and Power MOSFETs

	Bipolar Power Transistor	Power MOSFET
Symbol		
Products in use	Very numerous	Growing rapidly
Product cost	Construction is relatively simple, an advantage in the long term.	Construction is more complex than that of bipolar transistors. This and the slightly larger chip size increases cost.
Drive	Fairly complex due to current drive. Also it influences switching time and makes selection of drive conditions difficult.	Voltage drive, so extremely simple. Load current and safe operation range are unrelated.
Switching time	Minority carrier device, therefore slow.	Much faster than bipolar transistors. No storage time and no influence from temperature.
Safe operation area	Restricted due to risk of secondary breakdown.	Basically restricted by power dissipation (equal power lines).
Breakdown voltage (collector-emitter, drain-source)	Determined by V_{CEX} (V_{CBO}) for most circuits. Rating is 1.2 to 2.0 × V_{CE}.	Limited by V_{DSS} except when the gate of a trench-structure MOSFET is inversely biased with V_{GS} (limited by V_{DSX})
ON voltage	Extremely low, even for high breakdown voltage devices. Temperature coefficient is normally negative.	Can be extremely low for low breakdown voltage devices, but is somewhat higher for high breakdown voltage devices. Positive temperature coefficient.
Parallel connection	Difficult due to current balance relationship.	Some caution required, including equalization of oscillation or switching time, but parallel connection is possible.
Temperature stability	h_{FE} rises and V_{BE} falls along with temperature rise, so some caution is required.	Extremely high stability in relation to the temperatures of various parts.

3. Maximum Ratings

3.1 Definition

The maximum current, voltage, and allowable power dissipation are specified as maximum ratings for power MOSFETs.

When designing a circuit, it is very important to understand the maximum ratings to ensure the most effective operation and reliability of the power MOSFETs for the required period of time.

The maximum ratings are the values which must not be exceeded to ensure the power MOSFET's life and reliability. Note that the maximum ratings mean the absolute maximum ratings.

The absolute maximum ratings are the values which must never be exceeded during operation even for a moment.

If the maximum ratings are exceeded, some characteristics may be deteriorated in an unrecoverable manner. Therefore, pay much attention to fluctuations of supply voltage, characteristics of electrical components, ambient temperature, and input voltage, as well as maximum rating violation during circuit adjustment so that no maximum rating value is exceeded.

Parameters that must be specified for the maximum ratings include current for power MOSFET's drain, voltage between each pair of pins, power dissipation, channel temperature, and storage temperature. These parameters cannot be considered individually since they are closely related to each other, and they are subject to change due to the circuit's environmental conditions.

3.2 Voltage Ratings

3.2.1 Maximum Drain-Source Voltage Rating

There are four methods of specifying the drain-source breakdown voltage of a power MOSFET in accordance with gate-source bias conditions.

Figure 3.1 shows the various drain-source breakdown voltage modes.

(1) V_{DSS}: the drain-source voltage with zero gate-source bias (the last "S" means short).

(2) V_{DSX}: the drain-source voltage with reverse bias (for example, when a voltage of V_{GS} = –3 V is applied with an N-channel MOSFET).

(3) V_{DSR}: the drain-source voltage with resistance shunted between the gate and source (the "R" means shunt resistance).

When a Power MOSFET, except a trench type MOSFET, is the enhanced type, the relationship $V_{DSS} \simeq V_{DSX}$ is established in the above three breakdown voltage modes. In addition, there is almost no difference in breakdown voltage from the V_{DSX} mode, even when the drain-source breakdown voltage (V_{DSR} mode) is measured with a large resistance inserted between the gate and source, and the relationship $V_{DSS} \simeq V_{DSX} \simeq V_{DSR}$ is established.

For a trench type MOSFET, the relationship $V_{DSS} \geqq V_{DSX}$ is established because breakdown voltage at V_{DSX} mode fall depending on applied voltage to gate-source.

Consequently, there is no method for regulating a drain-source breakdown voltage larger than the V_{DSS} value, which is therefore used as the maximum rating. Thus, caution must be exercised to avoid exceeding the V_{DSS} value, even instantaneously.

(4) V_{DSO}: drain-source voltage with the gate open

The input impedance of a power MOSFET is extremely high; therefore, bias is applied between the gate and source by static electricity inductance, etc., and the device is destructed because of malfunction. Avoid use in this mode.

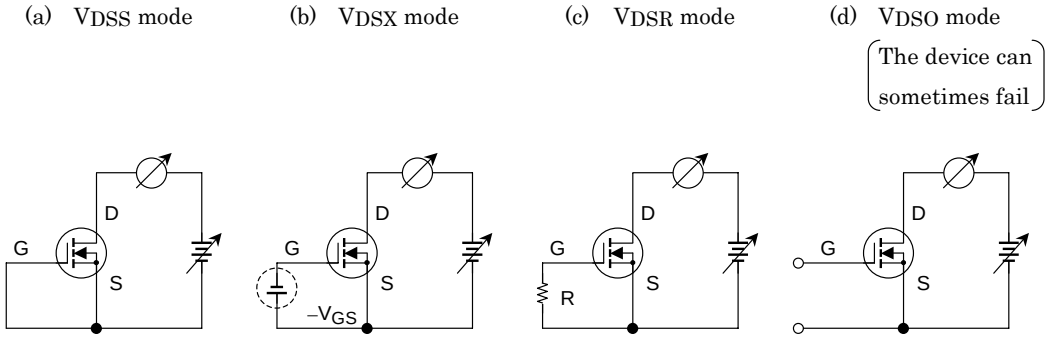


Figure 3.1 Drain-Source Breakdown Voltage

3.2.2 Maximum Gate-Source Voltage Rating

V_{GSS}: the gate-source voltage when the drain and source are shorted, which is determined by the degree of withstand of the gate oxide film. The maximum rating for a MOSFET should be based on the side of the maximum sustainable practical voltage or, in consideration of reliability.

3.3 Current Ratings

For power MOSFETs, the DC current that flows in the forward direction is referred to as I_D and the pulse current that flows is referred to as I_{DP}. The values of the reverse-direction (diode direction) DC current (I_{DR}) and pulse current (I_{DRP}) are defined as the same as the corresponding currents flowing in the forward direction under the ideal heat radiation condition.

The forward-direction DC and pulse currents are subject to the effects of the power loss caused by drain-source ON-resistance. The reverse-direction currents are subject to the effects of power dissipation caused by the diode's forward voltage. Hence, current ratings are determined by the heat radiation conditions; the channel temperature maximum rating value (T_{ch}) must not exceed 150°C.

3.4 Temperature Ratings

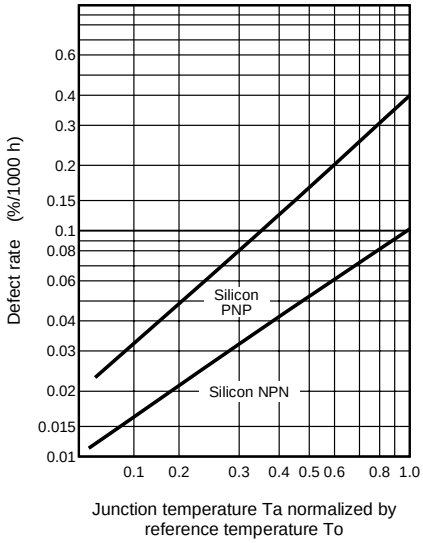
Maximum channel temperature T_{ch} is defined according to the constituent material and reliability requirements. It must be considered not only in terms of device operation, but also in conjunction with such factors as allowable degradation and minimum service life.

Degradation of power MOSFETs generally accelerates as the channel temperature increases. The following relationship is known to exist between the mean service life L_m (hours) and channel temperature T_{ch} (K)

$$\log L_m \simeq A + \frac{B}{T_j} \quad \text{.....(1)}$$

Where A and B are constants inherent to power MOSFETs

For a power MOSFET required to have a long-term guaranteed service life, the upper limit of the allowable channel temperature is defined according to the power MOSFET defect rate and reliability. Generally, the channel temperature is below 150°C.



$$Ta = \frac{T_j - To}{T_{jmax} - To}$$

Figure 3.2 Relationship between Lifespan and Junction Temperature of Bipolar Transistor (source: MIL-HDBK-217A)

Storage temperature T_{stg} is the temperature range within which non-operating power MOSFETs can be safely stored. This rating is also defined by the power MOSFET's constituent material and reliability. Figure 3.2 shows a typical relationship between the lifespan and junction temperature of a bipolar transistor.

3.5 Power Ratings

The power dissipation in a power MOSFET is converted into thermal energy which in turn causes the power MOSFET internal temperature to rise.

Internal power dissipation of a power MOSFET operating at a certain point is represented by the equation $P_D = (I_D \cdot V_{DS})$.

The primary parameters limiting maximum power dissipation P_{Dmax} in a power MOSFET are maximum channel temperature T_{chmax}, described above, and reference temperature To (ambient temperature Ta or case temperature Tc). These parameters are known to be correlated by thermal resistance θ (or R_{th}).

$$P_{Dmax} = \frac{T_{chmax} - To}{\theta} \quad \text{.....(2)}$$

Thermal resistance represents the ratio at which the channel temperature increases per unit amount of power dissipation. That is, it is a physical quantity that indicates a difficulty in radiating heat. To allow for large power dissipation, therefore, it is necessary to choose a power MOSFET with a large P_{Dmax}. Knowing how to design for heat radiation in power MOSFETs is especially important.

The rated value of P_{Dmax} is normally defined with respect to Ta = 25°C, or with respect to Tc = 25°C when the use of a heat sink is anticipated. In either case, Equation (2) can be used to determine thermal resistance between a power MOSFET channel and the external air or between the channel and the case.

3.6 Safe Operating Area

3.6.1 Forward Bias Safe Operating Area (SOA)

Because current concentration does not readily occur in power MOSFETs due to their structure, in principle, unlike in bipolar transistors, secondary breakdown does not occur in the high-voltage area. Thus, for power MOSFETs the safe operating area (SOA) can be expressed by a constant-power line which is limited by thermal resistance with pulse width as a parameter (Figure 3.3). The device can be safely operated over a very wide range within the breakdown voltage between the drain and source without narrowing the high-voltage area in the SOA.

Along with the higher precision of cells developed, some power MOSFETs exhibit a phenomenon similar to secondary breakdown.

The safe operating areas of these power MOSFETS are defined individually. Figure 3.4 shows the safe operating areas which are different from the typical safe opeating areas limited by the constant-power lines as shown in Figure 3.3.

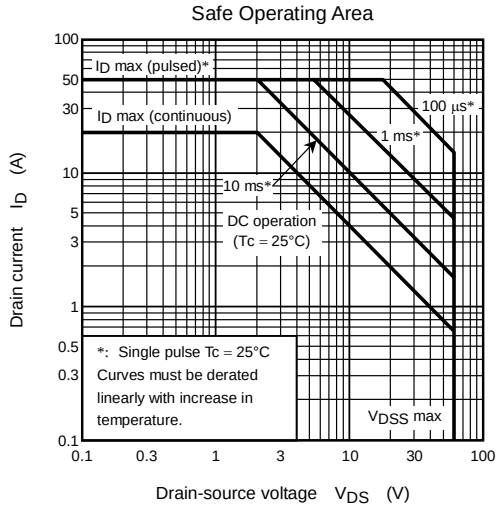


Figure 3.3 Power MOSFET Safe Operating Area (2SK2782)

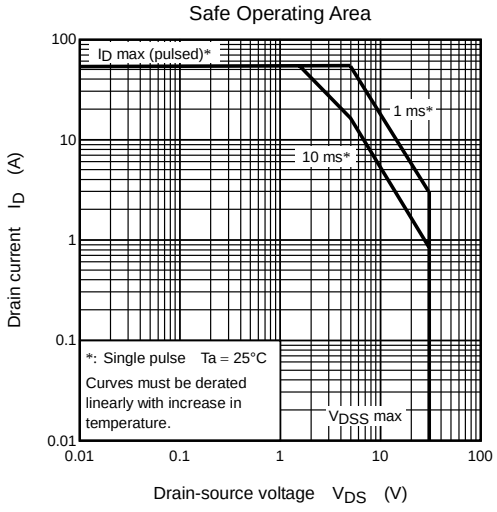


Figure 3.4 Power MOSFET Safe Operating Area (TPC8009-H)

3.6.2 Reverse Bias Safe Operating Area

When a switching device is used in the field of power switching for applications such as switching power supplies, the load becomes inductive. In this case, both the forward and reverse safe operation ranges become a problem.

Normally, when bipolar transistors are used in switching power supplies, forced reverse bias is applied between the base and emitter to reduce switching loss, base reverse current I_{B2} is applied, and t_{stg} and t_f are shortened. However, if I_{B2} is increased, the reverse bias safe operating area becomes narrow, as shown in Figure 3.5, and the load curve operation range is restricted during turn OFF.

With power MOSFETs, on the other hand, t_f and t_{off} can be shortened by applying reverse bias between the gate and source. However, since power MOSFETs are majority carrier devices and there is essentially no carrier storage effect, the reverse bias SOA does not become narrow even if gate reverse voltage $-V_{GS}$ increases. (However, breakdown voltage for trench type power MOSFET falls depending on an applied V_G; hence, reverse bias SOA becomes narrow.)

(a) Reverse safe operating area

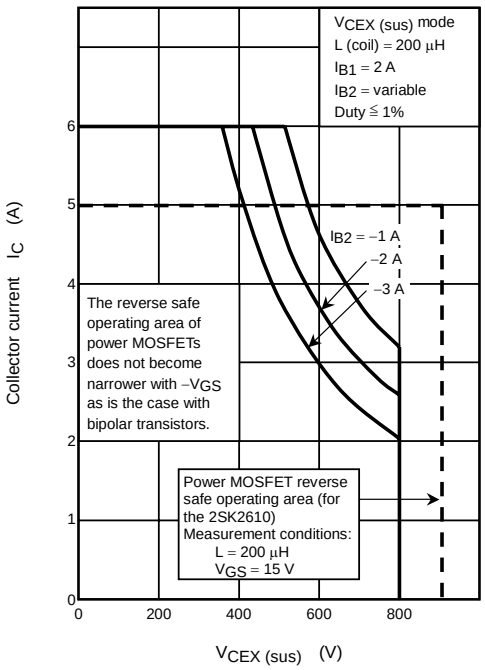


Figure 3.5 Reverse Safe Operating Area

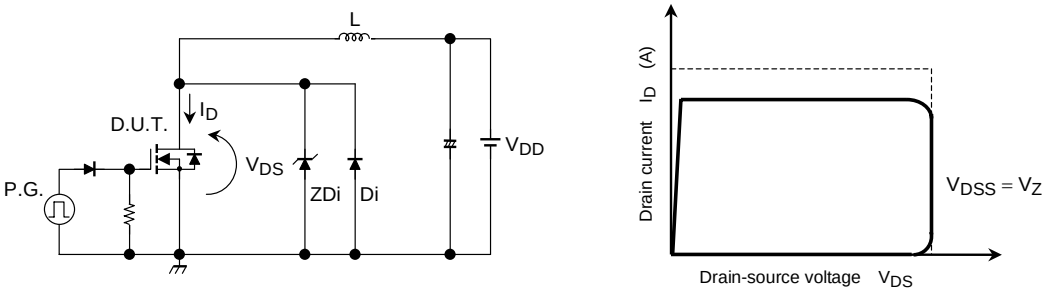


Figure 3.6 Measurement Circuit for Reverse Safe Operating Area

3.7 Derating

When designing power MOSFET circuits, you determine the appropriate heat radiation condition from the absolute maximum ratings (maximum ratings) listed in the technical datasheets to ensure that the parameters-voltage, current and power (channel temperature)-are each within the maximum rating. However, it is a common practice to derate these maximum values in consideration of reliability requirements prior to using them in a circuit design.

To balance maximum ratings against reliability and economy, the following derating methods are generally recommended:

- Voltage: The worst-case voltage (including surge) must be no greater than 80% of the maximum rated voltage.
- Current: The worst-case current (including surge) must be no greater than 80% of the maximum rated current.
- Power: The worst-case power (including surge) must be no greater than 50% of the derated maximum power dissipation at the maximum ambient temperature of the equipment in which the device is used.
- Temperature: The maximum operating channel temperature T_{ch} (including surge) must be 70% to no greater of the 80% of the T_{chmax}.

The power dissipation of power MOSFETs used in switching circuits must be such that the peak values (including surges) of voltage, current, power and channel temperature do not exceed the absolute maximum ratings (maximum rating). However, when using these power MOSFETs under derated conditions, with respect to reliability, power dissipation can be considered in terms of average values. Safe operating areas before and after derating are expressed as the formulas shown in Figure 3.7.

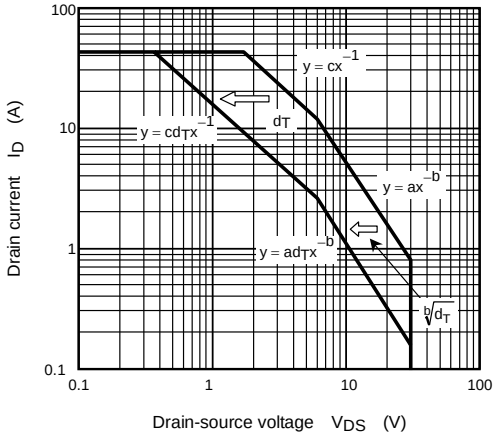


Figure 3.7 Temperature Derating in Safe Operating Range

The derating ratio d_T of the constant-power line is expressed by using the following definition equation:

$$P_D = \frac{T_{chmax} - Ta}{r_{th(ch-a)}} \quad \text{..... (3)}$$

as follows:

$$d_T = \frac{P_{D(T_{ch}\,°C)}}{P_{D(25°C)}} = \frac{T_{chmax} - T_{ch}}{T_{chmax} - 25} \quad \text{..... (4)}$$

When $T_{ch} = 25°C$, the constant-power line is:

$$y = cx^{-1} \quad \text{..... (5)}$$

The constant-power line after derating is:

$$y = cd_Tx^{-1} \quad \text{..... (6)}$$

When the line limited by the phenomenon similar to secondary breakdown at $T_{ch} = 25°C$ is:

$$y = ax^{-b} \quad \text{..... (7)}$$

The derating ratio and the equation after derating are expressed as follows:

$$d_{PS/B} = \sqrt[b]{d_T} \quad \text{..... (8)}$$

$$y = ad_Tx^{-b} \quad \text{..... (9)}$$

<Example of derating (TPC8108)>

Using TPC8108 as an example, derate the safe operating area from Ta (= T_{ch}) = 25°C to Ta = 125°C.

Read the coordinates of the points marked with a circle (o) in the safe operating area (in the individual technical data) at Ta = 25°C. Substitute the read coordinates for the values in equations (3) and (5). The constant-power lines are calculated as follows:

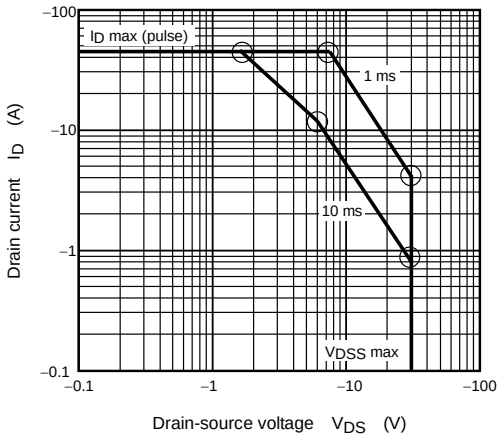


Figure 3.8 TPC8108 Safe Operating Area (Ta = 25°C)

$$y = 470_x^{-1} \quad (Ta = 25°C,\ t = 1\ ms) \quad \text{..... (8)}$$

$$y = 76.2_x^{-1} \quad (Ta = 25°C,\ t = 10\ ms) \quad \text{..... (9)}$$

Lines limited by the phenomenon similar to secondary breakdown are calculated as follows:

$$y = 1500_x^{-1.73} \quad (Ta = 25°C,\ t = 1\ ms) \quad \text{..... (10)}$$

$$y = 282_x^{-1.73} \quad (Ta = 25°C,\ t = 10\ ms) \quad \text{..... (11)}$$

When derating from Ta = 25°C to Ta = 125°C, the derating ratio d_T of the constant-power line is $d_T = 0.2$.

Constant-power lines at Ta = 125°C are calculated as follows:

$$y = 407_x^{-1} = 81.4_x^{-1} \quad (Ta = 125°C,\ t = 1\ ms) \quad \text{..... (8)}$$

$$y = 76.2_x^{-1} = 15.2_x^{-1} \quad (Ta = 125°C,\ t = 10\ ms) \quad \text{..... (9)}$$

Lines limited by the phenomenon similar to secondary breakdown are calculated as follows:

$$y = 1500d_x^{-1.73} = 300_x^{-1.73} \quad (Ta = 125°C,\ t = 1\ ms) \quad \text{..... (10)}$$

$$y = 282d_x^{-1.73} = 56.4_x^{-1.73} \quad (Ta = 125°C,\ t = 10\ ms) \quad \text{..... (11)}$$

Figure 3.9 shows the safe operating area plotted using equations from (8) to (10).

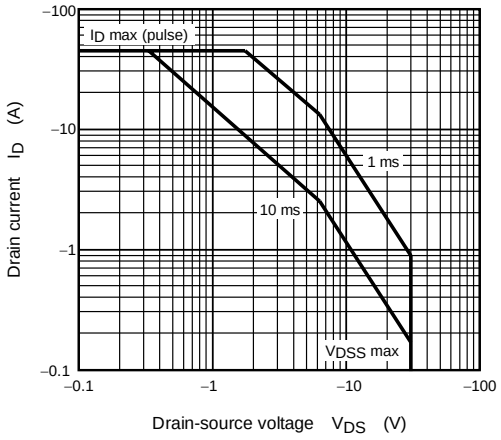


Figure 3.9 TPC8108 Safe Operating Area (Ta = 125°C)

4. Electrical Characteristics

4.1 Terminology

The following is an explanation of main items used to evaluate power MOSFET performance.

(1) $|Y_{fs}|$: forward transfer admittance

$|Y_{fs}| = \Delta I_D / \Delta V_{GS}$

$|Y_{fs}|$ expresses power MOSFET amplification factor

(2) V_{th}: gate threshold voltage

If $V_{GS\ (OFF)}$ is the gate-source voltage in the cut-off state, and $V_{GS\ (ON)}$ is the gate-source bias voltage when drain current is flowing, then the following relationship can be established.

$V_{GS\ (OFF)} < V_{th} < V_{GS\ (ON)}$

(3) $R_{DS\ (ON)}$: drain-source ON resistance

This is the equivalent of the collector-emitter saturation voltage $V_{CE\ (sat)}$ of a bipolar transistor, and is used as a criterion for determining dissipation in the ON status.

(4) $V_{DS\ (ON)}$: drain-source ON voltage

This is a criterion for determining dissipation in the ON status, as with $R_{DS\ (ON)}$, and is expressed as a voltage value.

(5) C_{iss}, C_{rss}, C_{oss}: capacitances

C_{iss}, C_{rss} and C_{oss} are input capacitance, reverse transfer capacitance and output capacitance, respectively. These capacitances restrict the usable frequency and switching speed when a power MOSFET is used for switching operations.

The index = $|Y_{fs}|/C_{iss}$ (s^{-1}) is the equivalent of the cutoff frequency f_T of a bipolar transistor.

However, normally the following expression is used to define the theoretical cutoff frequency:

$f_{(max)} = |Y_{fs}|/2\pi \{C_{iss} + (1 + Av)\ C_{rss}\}$

4.2 Power MOSFET Temperature Characteristics

The transfer function of power MOSFETs is shown by the differential coefficient of the $I_D - V_{GS}$ curves shown in Figure 4.1.

In the large current area, the temperature coefficient of the transfer function is negative, therefore, the forward transfer admittance $|Y_{fs}|$ decreases when the internal (channel) temperature increases; so current concentration and failure due to thermal run-away don't occur easily even if a large drain current flows due to the output fluctuates.

Caution must be exercised concerning the temperature dependence of the drain-source ON resistance. This ON resistance approximately doubles for a temperature increase of 100°C (Figure 4.2). Thus, it is necessary to account for an induced temperature increase to select a heat sink with an appropiate thermal resistance ϕ_f.

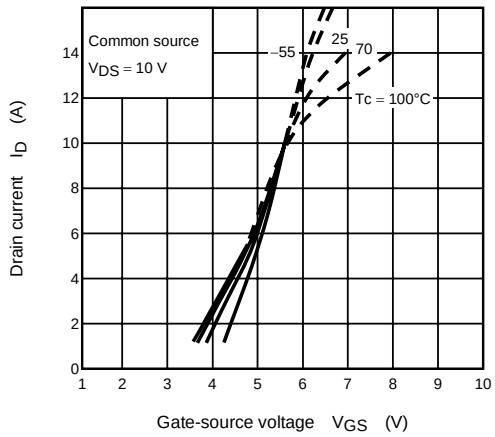


Figure 4.1 $I_D - V_{GS}$ Characteristics

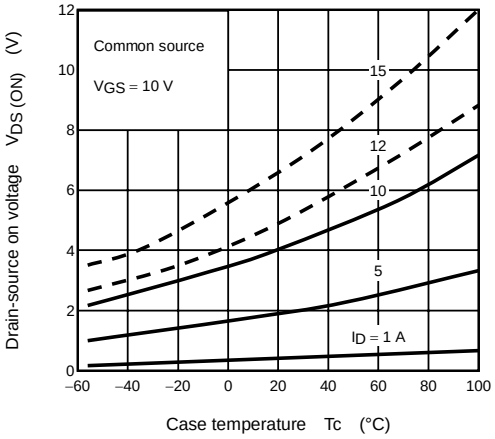


Figure 4.2 $V_{DS\ (ON)} - Tc$ Characteristics

4.3 Power MOSFET Electrostatic Capacitance Characteristics

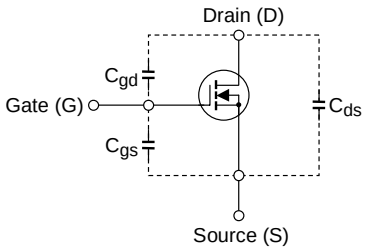
The physical construction of a power MOSFET is such that the gate is completely isolated from the silicon oxide film; therefore, the capacitances between the drain, gate and source terminals are as shown in Figure 4.3 (a).

Gate-drain capacitance C_{gd} and gate-source capacitance C_{gs} are determined by the gate electrode construction. In addition, drain-source capacitance C_{ds} is determined by the junction capacitance of the PN junction based on the double diffusion construction.

Input capacitance $C_{iss} = C_{gd} + C_{gs}$, output capacitance $C_{oss} \simeq C_{ds} + C_{gd}$, and reverse transfer capacitance $C_{rss} = C_{gd}$ are important characteristics for power MOSFETs.

Figure 4.4 shows the dependence of C_{iss}, C_{rss} and C_{oss} on drain-source voltage V_{DS}.

(a) Power MOSFET capacitance

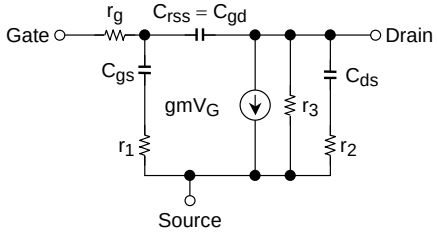


Input capacitance: $C_{iss} = C_{gd} + C_{gs}$

Output capacitance: $C_{oss} = C_{ds} + C_{gd}$

Reverse transfer: $C_{rss} = C_{gd}$

(b) Simple equivalent circuit including parasitic devices



r_g: gate electrode parasitic resistance

r_1: equivalent resistance of the source and channel areas

r_2: equivalent resistance of the high resistance layer adjacent to the drain

r_3: modulated part of the channel resistance

Input capacitance: $C_{in} = C_{gs} + (1 + A_V)\ C_{rss}$

Figure 4.3

In the driving of a power MOSFET, the switching characteristics fluctuate due to the input capacitance C_{iss} and the drive circuit impedance.

Since gate current flows between the gate and source to charge the input capacitor, the lower the drive circuit impedance the faster the switching speed.

Also, there is almost no temperature dependence of the capacitors (C_{iss}, C_{rss}, C_{oss}).

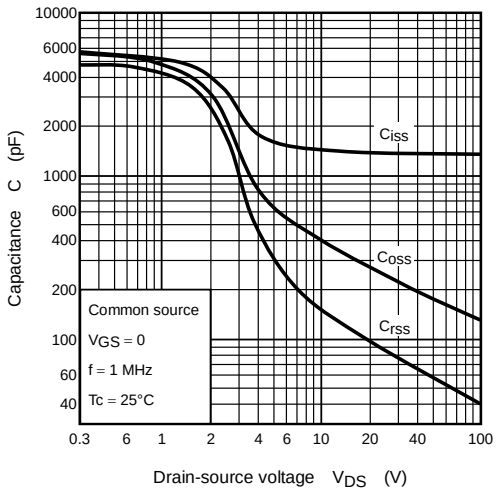


Figure 4.4 Capacitance – V_{DS} Characteristics

4.4 Power MOSFET Switching Characteristics

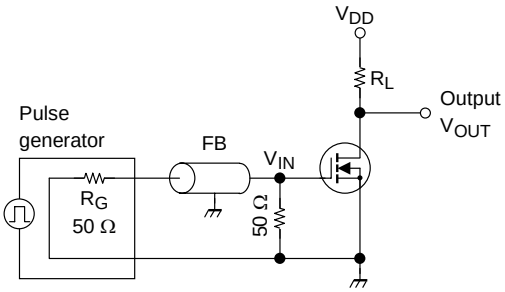
Since power MOSFETs are majority carrier devices, switching performance is their main characteristic of interest. The switching speed of a power MOSFET is much faster than that of a bipolar transistor and its high-speed, high-frequency operation is outstanding.

This characteristic is utilized in switching regulators (f = 1 kHz to 1 MHz) and in motor controls.

As mentioned before, two important features of power MOSFETs are that they have no storage time dependence, and that their capacitance doesn't depend on temperature; therefore, their switching characteristics are not hardly influenced by temperature fluctuations.

Figure 4.5 shows a typical switching time measurement circuit and input/output waveforms.

(a) Measurement circuit



(b) Input/output waveforms

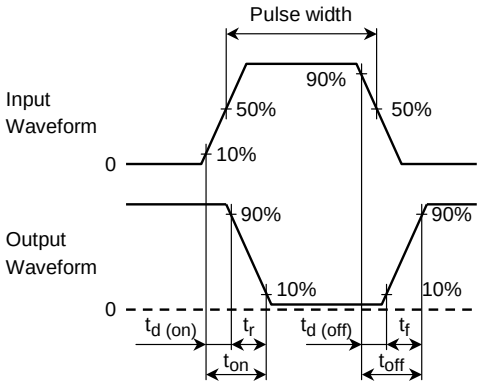


Figure 4.5 Switching Time Measurement Circuit and Input/Output Waveforms

The definitions of the symbols used for input and output waveforms for switching time are explained below.

(1) $t_{d\ (on)}$: turn-ON delay time

The charging time required to raise the voltage of input capacitance C_{iss} to the value of the threshold voltage V_{th}.

(2) t_r: rise time

The charging time required to raise the gate-source voltage from the value of gate threshold voltage V_{th} to the specified V_{GS} level.

(3) $t_{d\ (off)}$: turn-OFF delay time

The discharge time required to lower the gate-source voltage from the drive voltage of the saturation area to the specified V_{GS} level of the linear area.

(4) t_f: fall time

The time required to lower the gate-source voltage from the level of the drive voltage of the saturation area to the value of the gate threshold voltage level V_{th}, and to raise the output voltage to the supply voltage level.

As described above, the switching time can be divided into four different times. In addition, it should be noted that t_{on} is expressed by adding the turn-ON delay time $t_{d\ (on)}$ to the rise time t_r, and that t_{OFF} is expressed by adding the turn-OFF delay time $t_{d\ (off)}$ to the fall time t_f.

$t_{d\ (on)} + t_r = t_{on}$

$t_{d\ (off)} + t_f = t_{off}$

Figure 4.6 shows the switching characteristics (switching time versus drain current I_D).

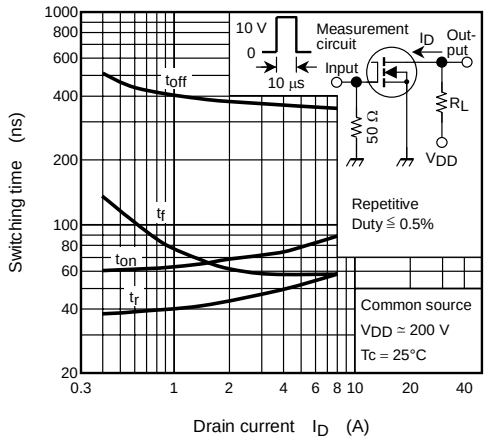


Figure 4.6 Switching Characteristics

4.5 Gate Charge

4.5.1 Gate Charge Characteristics

Power MOSFETs are driven by a voltage applied between the gate and source, and the ease with which a power MOSFET can be driven is expressed by the size of the charge stored in the gate.

$t_{d\ (on)}$ is the time required for an input signal to be applied, the input capacitor to be charged through the signal and gate resistors, and the gate voltage V_{GS} to exceed the threshold voltage. This is expressed as

$$t_{d\ (on)} \propto C_{gs} \times (r_g + R_G)$$

Here R_G is the signal resistance and r_g is the gate electrode parasitic resistance.

At $t_{d\ (on)}$, the gate charge is expressed as

$$Q_{gs\ (on)} \simeq C_{gs} \cdot V_{GS'}$$

During the interval t_r, the power MOSFET starts to operate; the input capacitance increases due to the mirror effect and t_r becomes longer than $t_{d\ (on)}$, as follows:

$$t_r \propto \{C_{gs} + (1 + A_V)\ C_{rss}\} \times (r_g + R_G)$$

During the t_r interval, the gate charge increases by the amount of reverse transfer capacitance C_{rss}, as follows:

$$Q_{on} \simeq \{C_{gs} + (1 + A_V)\ C_{rss}\} \cdot V_G$$

If the transient flow of gate charging current is i_G (t), then the total charge Q_{total} can be determined by using the following equation:

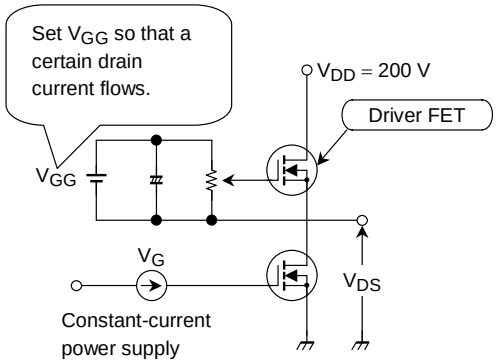
$$Q_{total} = \int_0^t i_G\ (t)\ dt$$

4.5.2 Calculating the Total Gate Charge

When the power MOSFET is switched ON, the gate current i_G (t) flows to charge the gate-source and gate-drain capacitors.

To determine the total gate charge under the circuit conditions shown in Figure 4.7, consider allowing a small gate current of i_G (t) = 1 mA (constant) to flow for 12 μs and then stopping the flow of this gate current.

(a) Total gate charge measurement circuit



(b) i_G (t), V_{GS} (t), V_{DS} (t) waveforms

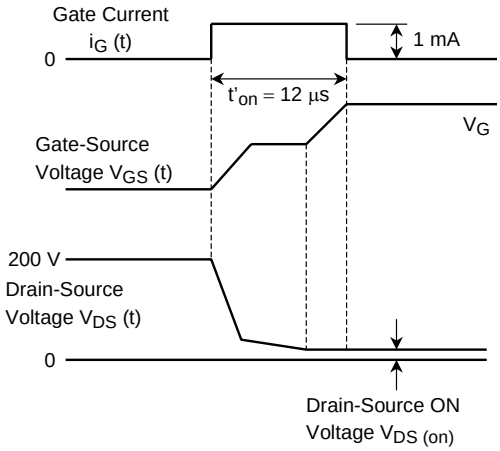


Figure 4.7 Total Gate Charge

The total gate-source charge Q_{total} will be as follows:

$$Q_{total} = \int_0^{t'_{on}} i_G\,(t)\,dt$$

From the constant current i_G (t) = 1 mA, the gate current is determined as follows.

i_G (t) = I_G = 1 mA = 1×10^{-3} A

Also, if t'_{on} = 12 μs = 12×10^{-6} s, then

$$Q_{total} = \int_0^{t'_{on}} i_G\,(t)\,dt = I_G \cdot t'_{on}$$

$$= 1 \times 10^{-3} \times 12 \times 10^{-6}$$

$$= 12 \times 10^{-9}\ (C)$$

This Q_{total} indicates the charge required to switch the MOSFET ON.

4.6 Source-Drain Diode

Due to their construction, double-diffusion-construction power MOSFETs have a parastic diode between the source and drain.

The ratings for the forward current I_{DR} (Figure 4.8) and the reverse breakdown voltage for this parastic diode are the same as for drain current I_D and drain-source voltage V_{DSS} for a power MOSFET under the ideal heat radiation condition.

The reverse recovery time t_{rr} for this diode is similar to that for a Fast Recovery Diode (FRD). Figure 4.9 shows a reverse recovery time measurement circuit for the parastic diodes of power MOSFETs.

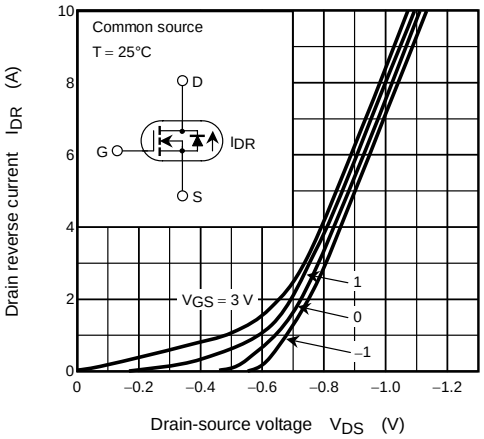
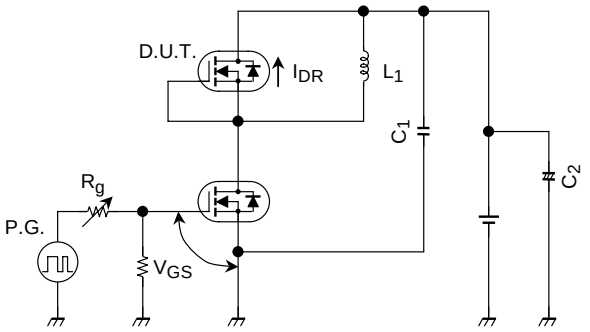


Figure 4.8 I_{DR} – V_{DS} Characteristics

(a) Reverse recovery time measurement circuit



(b) Reverse recovery time (t_{rr}) and charge (Q_{rr})

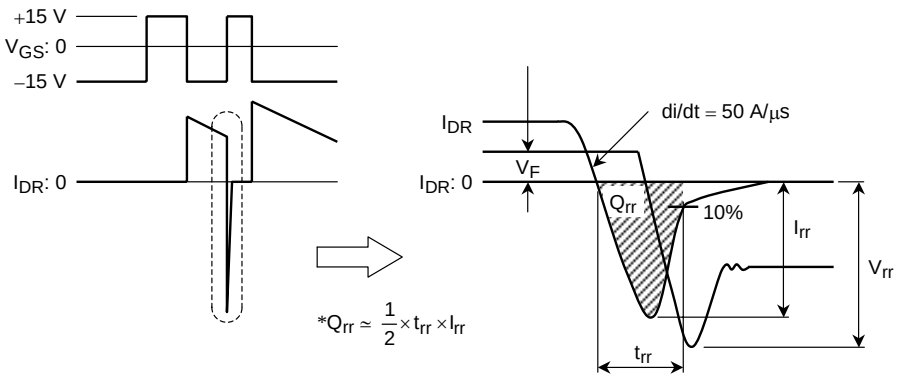


Figure 4.9 Reverse Recovery Time Measurement Circuit for the Parastic Diodes of Power MOSFETs

5. Application Precautions

5.1 Precautions Concerning Drive Conditions for Shortening Switching Time

Bipolar transistors require a large base current to maintain the saturation area; however, power MOSFETs are voltage-controlled devices and can therefore be driven by merely applying a small power to the gate.

However, since the input capacitance C_{iss} of power MOSFETs is somewhat high, it is necessary to quickly charge the input capacitor with low-impedance signal sources, especially for high-speed switching.

Low-impedance drive is necessary to shorten the turn-ON time; however, the input capacitance Ciss is overcharged when the voltage applied is increased and, conversely, $t_{d\ (off)}$ becomes longer.

It is possible to turn OFF power MOSFETs by dropping the gate voltage to zero but, as with bipolar transistors, it is also possible to turn a Power MOSFET OFF quickly by reducing the value of the charge Q to zero. The charge Q which is built up by the gate-source and gate-drain voltage, will quickly fall to zero after applying a reverse bias between the gate and source voltage ($i_g = dQ/dt$).

Figure 5.1 shows the relationship between the magnitude of the reverse bias and the switching time.

In the case of N-channel MOSFETs, it is possible to decrease the switching times t_f and t_{off} by using a negative power supply, that is, by configuring a low-impedance circuit.

To operate power MOSFETs at high speed, it is necessary to add a speed-up circuit to increase the speed at which the equivalent input capacitance between the gate and source is charged.

Figure 5.2 shows a speed-up circuit.

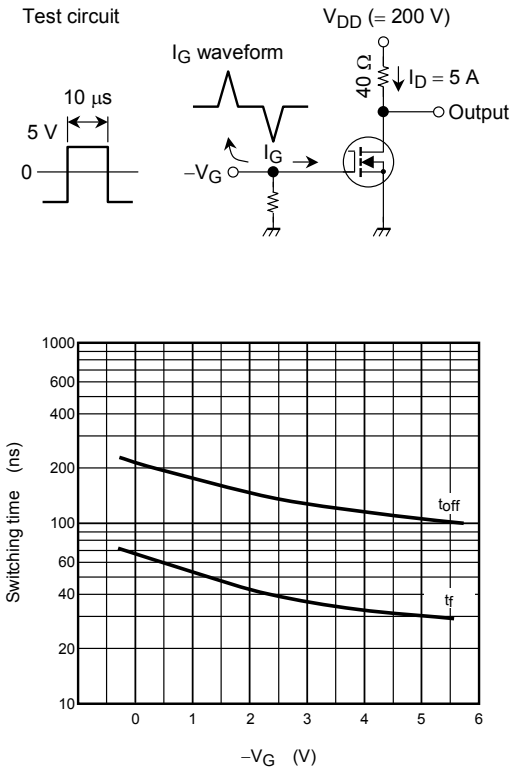


Figure 5.1 Switching Time – V_G Characteristics

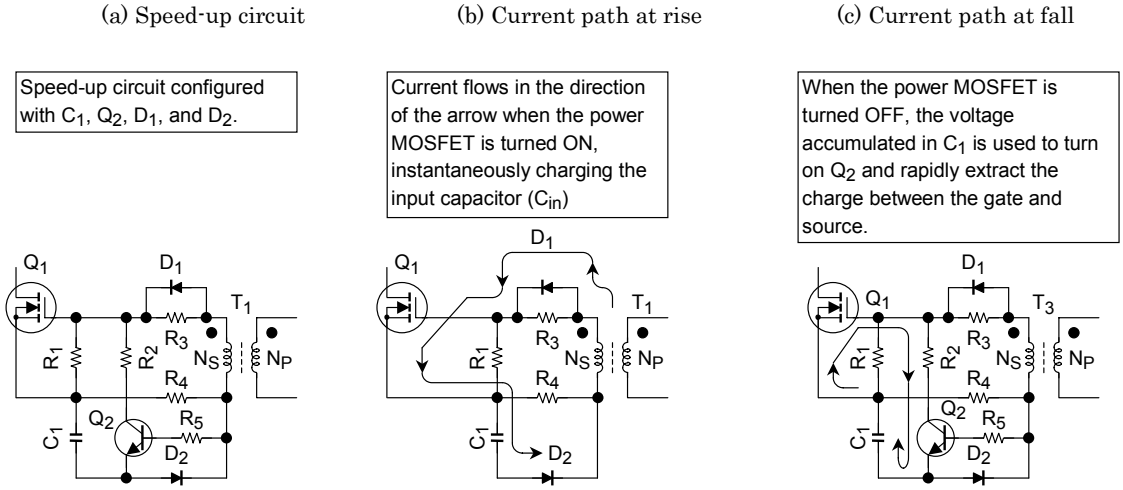


Figure 5.2 Gate Drive Speed-Up Circuit

5.2 The Influence of Wiring Inductance

Since the switching time for power MOSFETs is at least one order of magnitude faster than that of bipolar transistors, they are very effective in fields where high-speed switch is required. However, unless some countermeasure is taken in the circuitry, this high-speed switching characteristic may give rise to a voltage surge due to stray inductance L_S, which is impressed on the MOSFET. The magnitude of this surge, V_{surge}, is determined as follows:

$$V_{surge} = -(L_S + L'_S) \cdot di/dt + V_{DD}$$

It is necessary that this value be given sufficient margin in relation to drain-source breakdown voltage V_{DSS}. To reduce this surge voltage, it is necessary to reduce either di/dt or the stray inductance; however, since the reduction of di/dt does not agree with the original purpose of high-speed switching, it is necessary to reduce the stray inductance. This can be done by using copper plates instead of wires, because copper has lower inductance. Inserting the capacitors shown in Figure 5.3 is also an effective way of reducing the magnitude of the generated voltage surge.

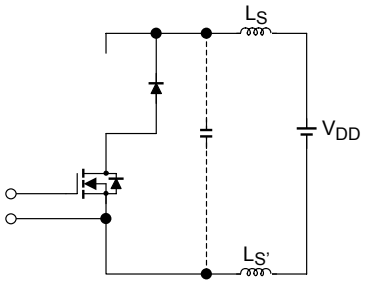


Figure 5.3 Circuit Stray Inductance

5.3 Parasitic Oscillation

Parasitic oscillation is more prone to occur with power MOSFETs than with bipolar transistors. This is caused by the high-frequency gain which is characteristically high with power MOSFETs. Parasitic oscillation may occur when impedance became negative resistance for input which is caused by strong coupling of input and output depending on gate-drain capacitance and stray capacitance. The following methods can be used to avoid this situation.

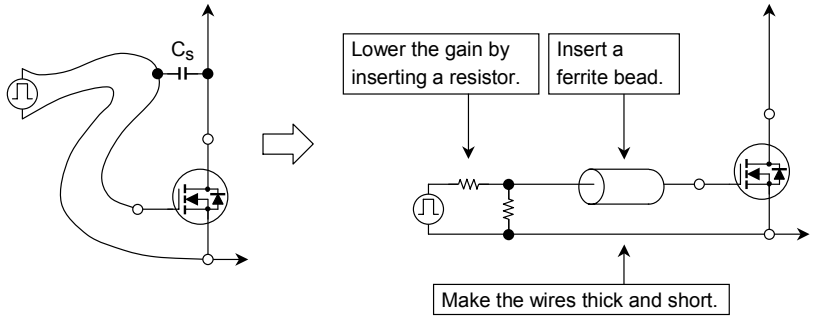


Figure 5.4 How to Prevent Parasitic Oscillation

(1) Make the wires thick and short. Twisted wires should be used not to connect the circuit to other wiring.
(2) Insert a ferrite bead as close to the gate as possible.
(3) Insert a series resistor at the gate.

5.4 Source-Drain Diode Withstand Capability

Normally, for motor control circuits, power MOSFETs are used in a bridge configuration in which the top and bottom power MOSFETs are turned ON and OFF alternately.

Now, Q_1 and Q_4 of the power MOSFETs shown in Figure 5.5 are turned ON and the current flows as indicated by A. Next, when FET Q_1 is turned OFF to control the motor speed, the current is fed back through the freewheeling diode of FET Q_2, as indicated by B. If FET Q_1 is again turned ON after that, a shorting current flows from FET Q_1 to FET Q_2 during the time (t_{rr}) until the freewheeling diode of FET Q_2 reverse recovers, and heat is generated due to the resulting power dissipation. Thus, when a power MOSFET is used for motor control, the t_{rr} of the parasitic diode should be minimized. Basically, it is possible to use the parasitic diode of a power MOSFET as a freewheeling diode; however, depending on the usage conditions, it may be necessary to install an external diode, as shown in Figure 5.6.

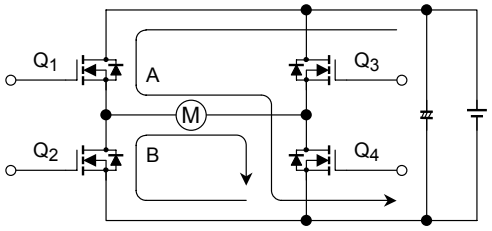


Figure 5.5 Motor Control Circuit Using Power MOSFET

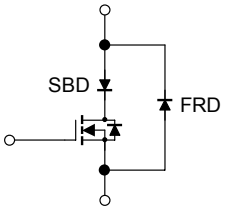


Figure 5.6 External Diode Connection Method

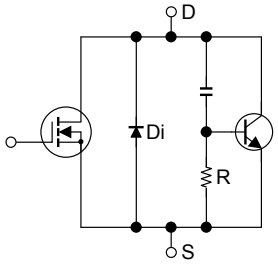
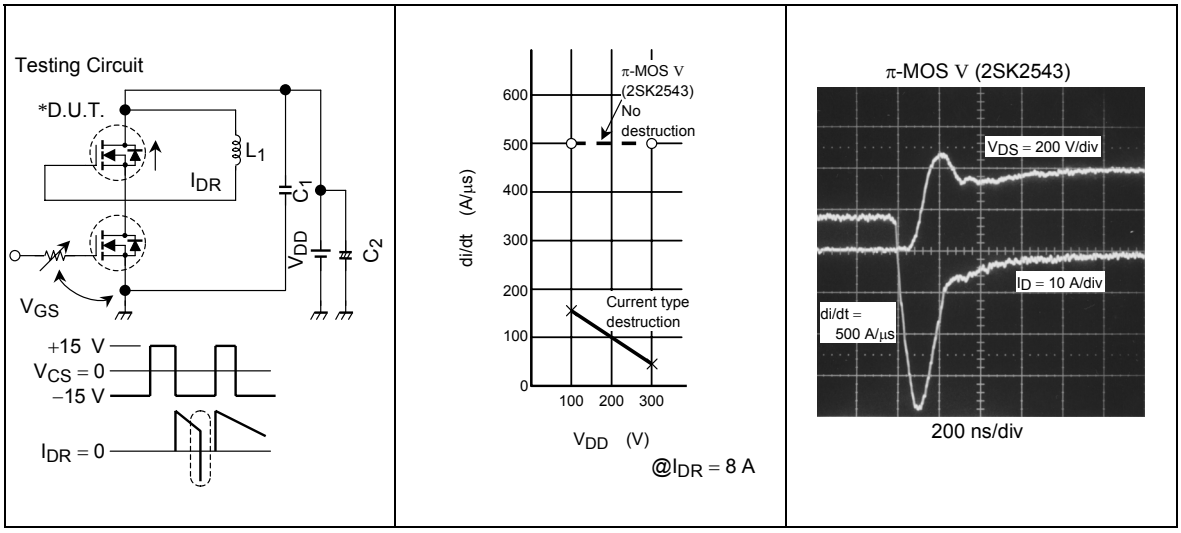


Figure 5.7 Parasitic Transistor of a Power MOSFET

Also, in a power MOSFET, the equivalent of a parasitic bipolar transistor exists between drain and source (see Figure 5.7). Note that this parasitic transistor may be turned 'ON' by the base-emitter resistor R's voltage drop, during the transitional state while a power MOSFET switches from 'ON' to 'OFF', and the device may break down.

As illustrated in Figure 5.5, when using parasitic diodes between drain and source in motor control circuits, power supply circuits and illumination circuits, it is recommended to use high-breakdown-voltage devices (example: π-MOS V series and similar).

Parasitic Diode Breakdown Voltage (for high-performance parasitic-diode type device)



*: D.U.T. = Device under test

5.5 Avalanche Resistance

At turn-OFF in power MOSFETs used as high-speed switching devices, high surge voltage can occur between the drain and the source, caused by the inductance of the circuits themselves and by drifting inductance. This voltage can exceed the maximum ratings of the MOSFET.

Previously, a surge absorption circuit was required to protect the MOSFET. Now, however, the reduction in the number of components and the miniaturization of equipment are creating a growing need to eliminate the absorption circuit and to absorb any surge in a power MOSFET even if it exceeds the maximum ratings.

In response to this need, Toshiba has developed a product line of power MOSFETs usable up to the point of self-breakdown voltage.

(1) Avalanche resistance guaranteed series

The following series guarantees avalanche resistance.

Voltage	Series
16 to 200 V	L^2-π-MOS V π-MOS V U-MOS I to IV
400 to 600 V	π-MOS V to VI
800 to 1000 V	π-MOS III to IV

(2) Guarantee method

The avalanche energy when $T_{ch\ (max)}$ reaches 150°C is listed in the maximum ratings column of the individual product specifications.

When using the product, check that the actual energy impinging on the device does not exceed its maximum rating.

Use the following procedure to check.

a) Calculate the channel temperature $T_{ch\ (max)}$

Calculate the total rise at avalanche in the channel temperature resulting from steady power loss and switching loss according to the following equations, and confirm that the maximum channel temperature value at avalanche doesn't exceed $T_{ch\ (max)}$ = 150°C.

A. For a single pulse:

$$\Delta T_{ch} = 0.473 \cdot V_{(BR)\ DSS} \cdot I_{AR} \cdot \theta_{ch\text{-}a}$$

in which

$V_{(BR)\ DSS}$: Breakdown voltage between drain and source

I_{AR}: Avalanche current

$\theta_{ch\text{-}a}$: Thermal resistance from channel to ambient air at avalanche

B. For a continuous pulse:

$$\Delta T_{chpeak} = P_0\left[\frac{T_1}{T}\theta_{ch\text{-}a} + \left(1-\frac{T_1}{T}\right)\cdot r_{th(T+T_1)} - r_{th(T)} + r_{th(T_1)}\right]$$

in which

P_0: Peak value

T_1: Pulse width

T: Cycle

$\theta_{ch\text{-}a}$: Thermal resistance from channel to ambient air

Note 1: For details of how to calculate T_{chpeak} of the continuous pulse see 6, Heat Sink Design.

b) Calculating avalanche energy E_{AS}

Check that the energy at avalanche during actual operation does not exceed the maximum rating, using the following equation:

$$E_{AS} = \frac{1}{2}\cdot L\cdot I_{AR}{}^2\cdot\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS}-V_{DD}}\right)$$

in which

E_{AS}: Avalanche energy

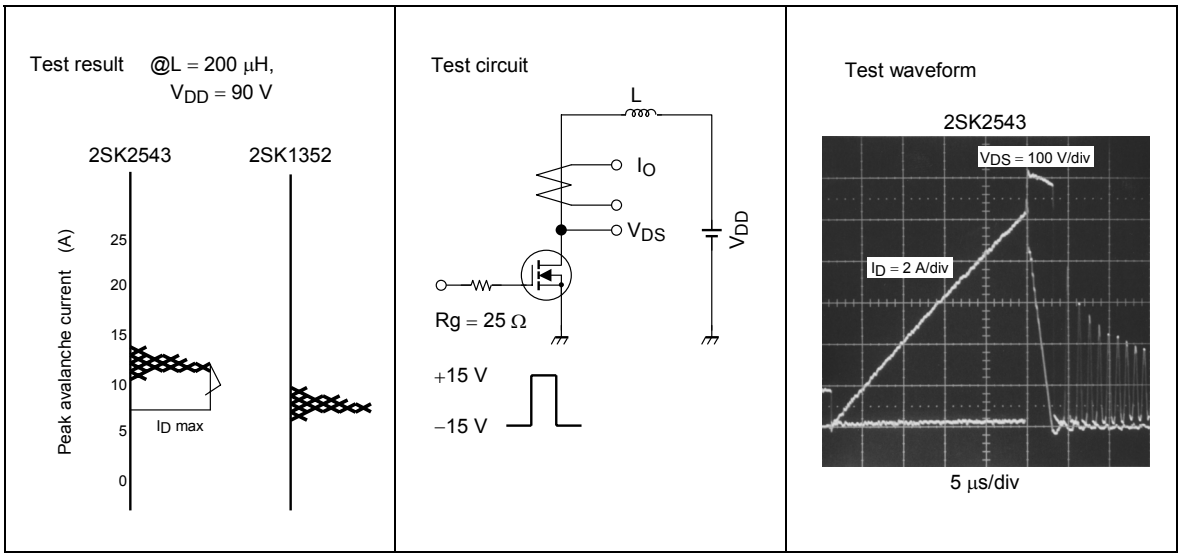
I_{AR}: Avalanche current

$V_{(BR)DSS}$: Breakdown voltage between drain and source

V_{DD}: Power supply voltage

Satisfying equations a) and b) above ensures that the device is used within its maximum ratings.

Avalanche Voltage



5.6 Parallel Connections

Power MOSFETs have outstanding thermal stability and do not suffer thermal runaway; therefore, parallel connection of them is easier than that of bipolar transistors.

Bipolar transistors are operated by the flow of base current; therefore, the current balance is disrupted by fluctuations of the base-emitter voltage V_{BE}, making parallel connections difficult. Power MOSFETs, on the other hand, are voltage driven. Therefore it is only necessary to supply drive voltage to each FET connected in parallel, making parallel connections relatively easy. However, when controlling high power at high speeds, it is necessary to carefully consider selection of devices and the range of possible fluctuations in their characteristics. The most important things to remember when making parallel connections are to avoid current concentration, including overcurrent during the transitional state, and to assure a well balanced, uniform flow of current to all devices under all possible load conditions.

Normally, current imbalance appears during switching ON and OFF; however, this is caused by differences in the switching times of the power MOSFETs. It is known that fluctuations in switching times are largely dependent on the value of the gate-source threshold voltage V_{th}. That is, the smaller the value of V_{th} the faster the switching ON; and the larger the value of V_{th} the slower the switching ON. Conversely, when turning OFF, the larger the value of V_{th} the faster the cutoff. Because of this, current imbalance occurs during both switching ON and OFF when the current concentrates in an FET with a small V_{th}. This current imbalance can apply an excessive load to a device and result in failure. Thus, when considering fluctuation in switching time during transition, it is preferable that the V_{th} values of all power MOSFETs connected in parallel should be the same.

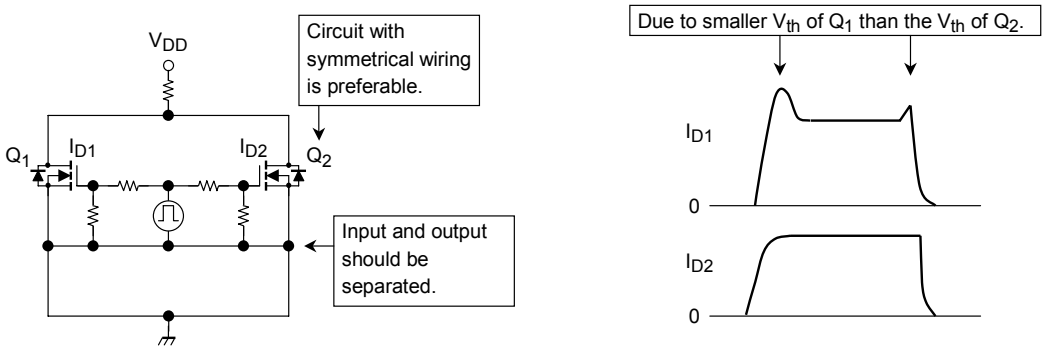


Figure 5.8 Imbalance of Current in Parallel Connection

6. Heat Sink Design

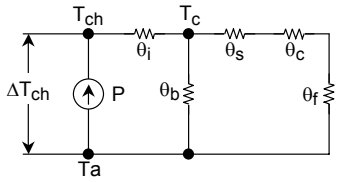
6.1 Maximum Allowable Power Dissipation and Radiation Equivalent Circuits

When the circuit has been designed for fully adequate thermal stability, the maximum allowable power dissipation (P_{Dmax}) for power MOSFETs can be determined based on the power MOSFET's ambient (external) air temperature (Ta), the maximum temperature in the power MOSFET's channel section (T_{chmax}), and the total thermal resistance ($\theta_{ch\text{-}a}$, sometimes denoted as R_{th}) from the channel to ambient air, that is determined by the radiating condition described below, as shown in the following equation (1).

$$P_{Dmax}(Ta) = \frac{T_{chmax} - Ta}{\theta_{ch\text{-}a}},\quad P_{Dmax}(Tc) = \frac{T_{chmax} - Tc}{\theta_{ch\text{-}c}} \quad \text{.....(1)}$$

With regard to the path by which thermal energy produced in the power MOSFET's channel section is transferred to the outside, we can think of such thermal transfer as similar to the conduction of electrical current except that the thermal conditions are expressed in terms of thermal resistance and thermal capacitance.

Figure 6.1 shows a radiation equivalent circuit under normal thermal conditions.



θ_i: Internal thermal resistance (from channel to case)

θ_b: External thermal resistance (from case direct to ambient air)

θ_s: Isolation plate's thermal resistance

θ_c: Contact thermal resistance (at point of contact with heat sink)

θ_f: Heat sink's thermal resistance (from the heat sink to ambient)

Figure 6.1 Equivalent Circuit

The total thermal resistance ($\theta_{ch\text{-}a}$) from channel to ambient air can be determined for the equivalent circuit shown in Figure 6.1 via equation (2) below.

$$\theta_{ch\text{-}a} = \theta_i + \frac{\theta_b(\theta_s + \theta_c + \theta_f)}{\theta_b + \theta_s + \theta_c + \theta_f} \quad \text{.....(2)}$$

Because medium-output and low-output transistors generally do not use heat sinks, in such cases $\theta_{ch\text{-}a}$ is expressed as shown in equation (3) below.

$$\theta_{ch\text{-}a} = \theta_i + \theta_b \quad \text{.....(3)}$$

In catalogs for medium-output and low-output transistors, the maximum allowable power dissipation is specified at Ta = 25°C. However, when this power dissipation value is not specified, we can calculate it using the $\theta_{ch\text{-}a}$ value from equation (3) and the T_{chmax} value, as shown below.

$$P_{Dmax}(Ta = 25°C) = \frac{T_{chmax} - 25}{\theta_{ch\text{-}a}}$$

The thermal resistance θ_b from the case to ambient air depends on the material and configuration of the case, but it is a considerably larger value than those of θ_i, θ_c, θ_s and θ_f. Therefore, expression (2) is simplified and the following expression can be used in practice.

$$\theta_{ch\text{-}a} = \theta_i + \theta_c + \theta_s + \theta_f \quad \text{.....(4)}$$

In dealing with direct current dissipation, it is possible to realize a radiation design satisfying the maximum rating by finding expression (4). In using power MOSFETs in a pulse circuit or similarly fluctuating application, great care must be taken so that the peak value of T_{ch} never exceeds T_{chmax}.

6.2 Pulse Response of Channel Temperature

In general, the thermal impedance of a power MOSFET is given by a distributed constant circuit as shown in Figure 6.2.

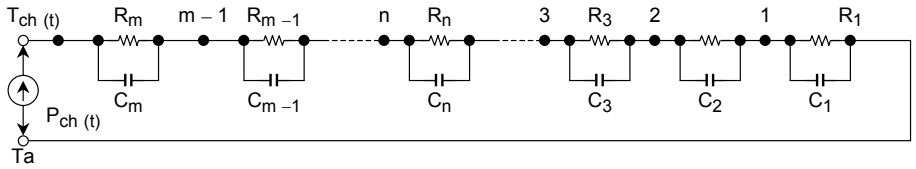


Figure 6.2 Power MOSFET Thermal Impedance

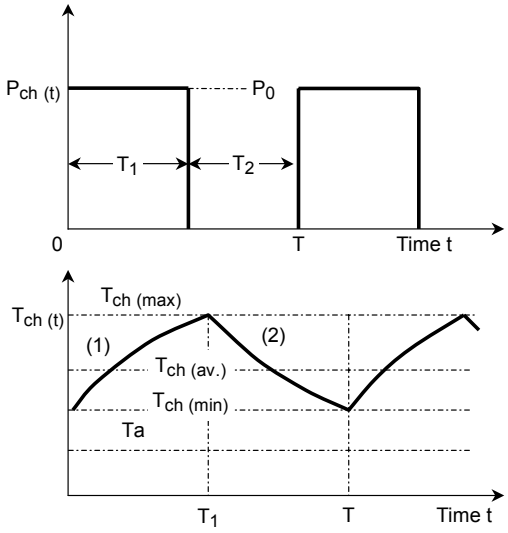


Figure 6.3 Temperature Change when Pulse Loss is Applied.

If pulse loss $P_{ch\ (t)}$ shown in Figure 6.3 is added to the circuit shown in Figure 6.2, the thermal variation $T_{ch\ (t)}$ that occurs in the m-th CR parallel circuit under stable thermal conditions can be calculated as follows:

(1) In areas where $P_{ch\ (t)} = P_0$,

$$T_{ch\ (t)} = \sum_{n-1}^{m} \left\{ (P_0 R_n) - T_{n\ (min)} \right\} \left\{ 1 - \exp\left(-t/C_n R_n\right) \right\} + T_{n\ (min)} \quad \cdots\cdots (5)$$

(2) In areas where $P_{ch\ (t)} = 0$,

$$T_{ch\ (t)} = \sum_{n-1}^{m} T_{n\ (max)} \exp\left(-t/C_n R_n\right) \quad \cdots\cdots (6)$$

For ordinary power MOSFETs, we can approximate the actual value of $T_{ch\ (t)}$ by assuming that n = approximately 4, but it is difficult to determine the T_{ch} value if the C and R values are not clear. Therefore, we generally estimate the T_{chpeak} using transient thermal resistance as described below.

In Figure 6.4, the characteristics of the 2SK2698 are shown as a typical example of transient thermal resistance characteristics. When a single rectangular pulse (with pulse width T_1 and peak value P_0) is added to this circuit, we can determine the T_{ch} peak by using the transient thermal resistance $r_{th\ (T1)}$ for the pulse width T_1. The T_{chpeak} is expressed according to equation (7) below.

$$T_{chpeak} = r_{th\ (T_1)} \cdot P_0 + Ta \quad \cdots\cdots (7)$$

When continuous pulses of cycle T are added (as shown in Figure 6.3), the T_{chpeak} under stable thermal conditions can be determined as indicated in equation (8) below.

$$T_{chpeak} = P_0 \left[\frac{T_1}{T} \theta_{ch\text{-}a} + \left(1 - \frac{T_1}{T}\right) \cdot r_{th(T+T_1)} - r_{th(T)} + r_{th(T_1)} \right] + Ta \quad \cdots\cdots (8)$$

When carrying out radiation design for pulse circuits, we must be careful so that the T_{chpeak} value shown in equation (8) does not exceed the power MOSFET's T_{chmax} value.

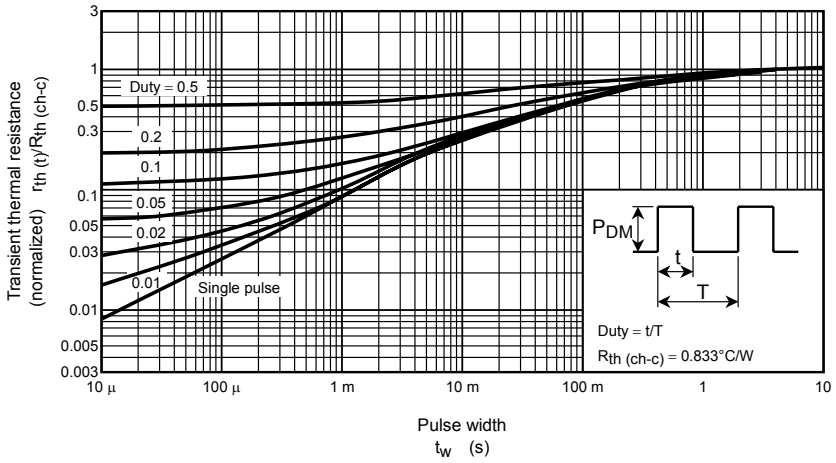


Figure 6.4 Transient Thermal Resistance (2SK2698)

The above analysis assumes that a rectangular wave is being applied. When using power MOSFETs in real equipment, in most cases the P_{ch} (t) is not a rectangular wave.

Usually in such cases the dissipation waveform approaches to a rectangular wave as shown in Figure 6.5, so that the T_{chpeak} value can still be obtained by using equation (8).

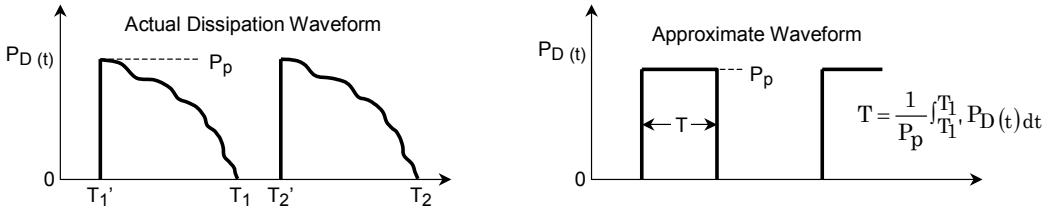


Figure 6.5 Approximate Power Loss Waveform

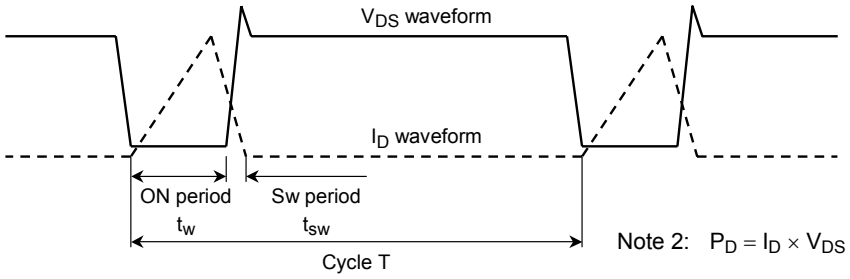
≪Calculation Example≫

The data needed for the calculation are: the waveform of the voltage between the drain and source, the drain current waveform, the ambient temperature, the heat sink thermal resistance data, and the operating conditions. Based on the formula (8), this data can be used to calculate the channel temperature.

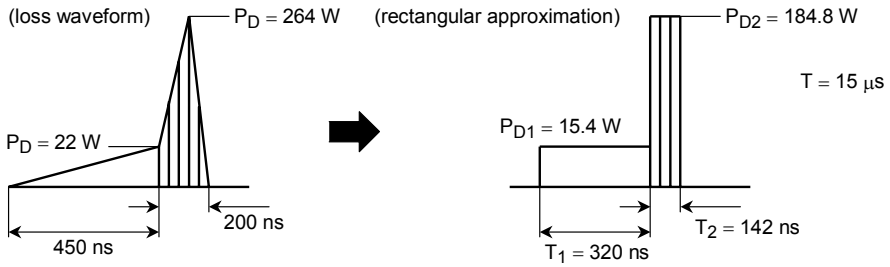
If the calculated temperature is within the maximum rating ($T_{ch\ (max)}$ = 150°C), the device can be used.

The following is a calculation example based on a typical waveform obtained under continuous operation for a switching power supply for example.

< Typical Waveform> Device Used: 2SK2837 (no heat sink)

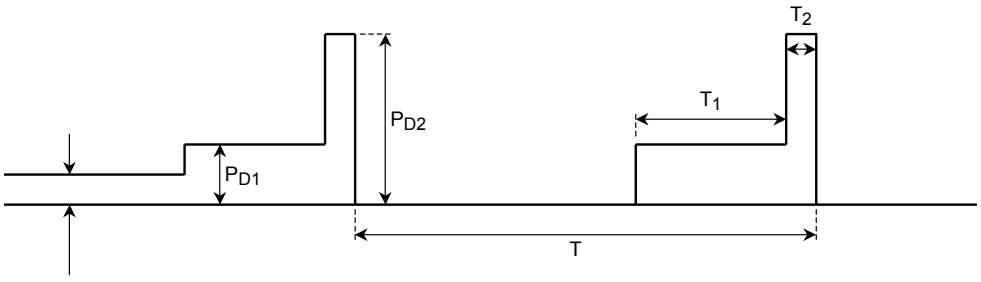


Using a rectangular approximation of the power loss (Note 2) of the above waveform, calculate the channel temperature by using formula (8). The loss waveform obtained from the above waveform and the rectangular approximation derived from the loss waveform are shown below.



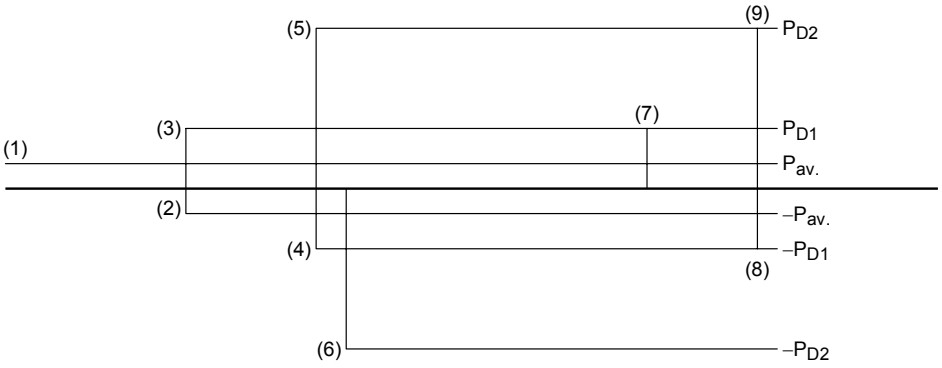
Applying a regularly repeating rectangular wave like the one in Figure 6.3, the peak of the channel temperature rise can be calculated by using formula (8). However, as mentioned the above, if multiple rectangular waves are applied cyclically, the calculation formula must be used with a different model.

In this model, repeating rectangular waves are treated as the sun of the average power dissipation and other two waves. Accordingly, in the case of the above rectangular wave, use the following type of approximation model to calculate the power loss.



$$P_{av.} = \frac{1}{T}\int_0^T (P_{D1} + P_{D2})\,dt = \frac{1}{T}(T_1 P_{D1} + T_2 P_{D2})$$

Calculate as below; that is, consider that the repetitive waveforms for two cycles follow the average power loss Pav applied for an infinite period.



$$\Delta T_{ch\text{-}a\,(peak)} = P_{av.} \times R_{th\,(ch\text{-}a)} - P_{av.} \times r_{th\,(T+T_1+T_2)} + P_{D1} \times r_{th\,(T+T_1+T_2)}$$

(1) (2) (3)

$$-P_{D1} \times r_{th\,(T+T_2)} + P_{D2} \times r_{th\,(T+T_2)} - P_{D2} \times r_{th\,(T)} + P_{D1} \times r_{th\,(T_1+T_2)}$$

(4) (5) (6) (7)

$$-P_{D1} \times r_{th\,(T_2)} + P_{D2} \times r_{th\,(T_2)} \quad \cdots\cdots (9)$$

(8) (9)

To calculate the channel temperature, the $R_{th\,(ch\text{-}a)}$, $r_{th\,(t)}$ thermal resistances are required, as in formula (9).

$r_{th\,(t)}$ value: Use the value derived from the transient thermal resistance graph included in the individual technical datasheet. Use the following formula to calculate the short pulse whose value is not included in the individual technical datasheet.

$$r_{th\,(t)} = r_{th\,(1ms)} \times \sqrt{t/1ms}$$

Read the values from datasheet 2SK2837 and calculate a rise in the channel temperature.

$$\Delta T_{ch\text{-}a\,(peak)} = P_{av.} \times R_{th\,(ch\text{-}a)} - P_{av.} \times r_{th\,(T+T_1+T_2)} + P_{D1} \times r_{th\,(T+T_1+T_2)} - P_{D1} \times r_{th\,(T+T_2)} + P_{D2} \times r_{th\,(T+T_2)} - P_{D2} \times r_{th\,(T)} + P_{D1} \times r_{th\,(T_1+T_2)} - P_{D1} \times r_{th\,(T_2)} + P_{D2} \times r_{th\,(T_2)} \simeq 104°C$$

$P_{av.}$ = 2.08 W

P_{D1} = 15.4 W

P_{D2} = 184.8 W

$R_{th\,(ch\text{-}a)}$ = 50°C/W

$r_{th\,(T+T_1+T_2)}$ = 0.0068°C/W

$r_{th\,(T+T_2)}$ = 0.0067°C/W

$r_{th\,(T)}$ = 0.0066°C/W

$r_{th\,(T_1+T_2)}$ = 0.0012°C/W

$r_{th\,(T_2)}$ = 0.0006°C/W

At an ambient temperature of 25°C, the peak channel temperature is:

$T_{ch\text{-}a\,(peak)} \simeq 104 + 25 = 129°C$

The thermal resistance in the radiation equivalent circuit shown in Figure 6.1 is explained as follows:

(1) Thermal resistance between channel and case (internal resistance) θ_i

Because the internal thermal resistance (θ_i) between the channel and case is directly determined by factors such as the power MOSFET's structure and materials, methods of mounting the power MOSFET chip in its case, and kind of case filler materials, each power MOSFET has its own thermal resistance characteristics.

To actually measure this value, the power MOSFET's case must be force-cooled to maintain a constant temperature.

Assuming that the case is force-cooled to a constant 25°C, the maximum allowable dissipation (P_{Dmax}) can be calculated as shown in equation (10) below.

$$P_{Dmax} = \frac{T_{chmax} - Tc}{\theta_i} = \frac{T_{chmax} - 25}{\theta_i} \quad \text{.....(10)}$$

In catalogs for large-output power MOSFETs, the maximum allowable drain dissipation is given for a constant case temperature of 25°C on the assumption of using infinite heat sinks. As was clearly demonstrated in equation (10), this value can also be based on the power MOSFET's internal thermal resistance value.

(2) Contact thermal resistance (θ_c)

The contact thermal resistance (θ_c) is determined by the condition of the contact surface between the power MOSFET case and the heat sink. This contact surface condition is greatly influenced by factors such as flatness, coarseness, contact area, and fastening method. For example, if silicon grease is applied to the contact surface, it can reduce the influence of factors such as surface flatness and coarseness. If the case is designed to be attached directly to the heat sink, such as in the TO-3 (L), TO-3P (N), and TO-220 types, to fasten a screw after applying silicon grease will reduce the contact thermal resistance to 0.5°C per W. However, medium-output and low-output power MOSFETs are not designed to be attached directly to heat sinks, due to their smaller size and the costs of their fabrication. Therefore even though heat sinks are used for these smaller power MOSFETs, they have a relatively high contact thermal resistance in case of poor attachment to the heat sink.

6.3 Insulation Plate's Thermal Resistance (θ_S)

In cases in which the power MOSFET must be insulated from the heat sink, we must insert an isolation material between the two.

The thermal resistance (θ_S) of this insulation barrier is determined by factors such as the type of insulation material and the material's surface area and thickness. Sometimes the thermal resistance value (θ_S) can be appreciable, so it must not be ignored.

Mica is the best type of insulation material in view of its high thermal transfer rate, and it can be used under high-temperature conditions. However, mica insulation material has disavantage in that it is fragile and difficult to fabricate in even thickness. Mylar is somewhat inferior to mica in terms of its thermal transfer rate, but it can be fabricated in thin plates of uniform thickness.

Table 6.1 Values of Thermal Resistance between Case and Heat Sink ($\theta_C + \theta_S$)

Case	Insulation Plate	$\theta_C + \theta_S$ [°C/W]	
		Silicon Grease	
		Greased	Ungreased
TO-220AB	No insulation plate	0.3 to 0.5	1.5 to 2.0
	Mica (50 to 100 μ)	2.0 to 2.5	4.0 to 6.0
TO-220 (IS)	No insulation plate	0.4 to 0.6	1.0 to 1.5
(TO-3P) 2-16C1B	No insulation plate	0.1 to 0.2	0.5 to 0.9
	Mica (50 to 100 μ)	0.5 to 0.8	2.0 to 3.0
(TO-3P (L)) 2-21F1B	No insulation plate	0.1 to 0.2	0.4 to 1.0
	Mica (50 to 100 μ)	0.5 to 0.7	1.2 to 1.5

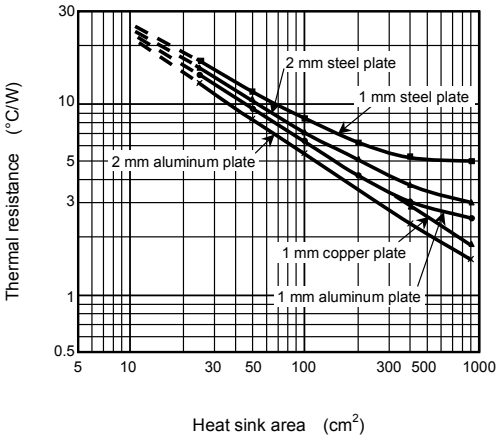


Figure 6.6 Heat Sink Area and Thermal Resistance (θ_f)

6.4 Heat Sink Thermal Resistance (θ_f)

The thermal resistance of a heat sink can be thought of as the distributed constant thermal resistance along the path of thermal transfer from the surface of the heat sink to the ambient air. Although the thermal resistance is influenced by factors such as the ambient air conditions, the temperature difference between the sink and the ambient air, and the heat sink's effective surface area, it is difficult to express these factors in a mathematical equation, and so the effects of these factors are currently determined by actual measurement.

Figure 6.6 shows the thermal resistance values of a heat sink measured with one power MOSFET standing vertically at the center of the heat sink.

Recently, manufacturers of heat sinks have announced various new heat sink models, and the above data may prove useful when putting these new models to practical use.

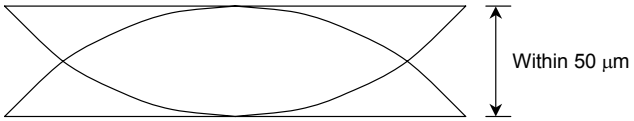
For descriptions of accessories required for mounting power MOSFETs on heat sinks, and of the correct mounting method, please refer to Section 6, "Accessories".

6.5 Attaching the Heat Sink

It is recommended to attach the heat sink in accordance with the following points. If these are ignored, for example if the heat sink has burrs, bumps or hollows, if its attachment profile is the wrong size, or if it is attached with the wrong torque, the device can be skewed, the pellet or resin can be damaged, or the adhesion between the resin and the frame can be weakened.

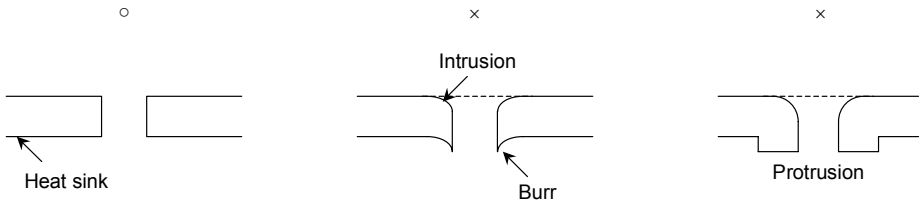
(1) Heat sink

The surface where the device is attached must be sufficiently smooth. Warps, large bumps or hollows in the surface, or foreign bodies such as punching burrs or chips lodged between the device and the attachment face can cause device failure in the worst case. To avoid these problems, the flatness of the surface where the device is attached should be within 50 μm.



(2) Attachment holes

Intrusion resulting from punch processing around attachment holes should be no more than 50 μm. The holes for attaching the device should be no larger than necessary. If intrusion does occur around a hole or if the diameter of the hole is larger than normal, be sure to fit a square washer.



(3) Screws

The screws to attach the device are generally classified as machine screws and tapping screws. If tapping screws are used, note that it is easy to exceed the maximum tightening torque. Also, avoid using special screws such as countersunk screws and round countersunk screws as these may place excessive stress on the device.

(4) Insulating spacers

Use mica or mechanically strong insulating spacers.

(5) Insulating washers

Use insulating washers that snugly fit the devices.

(6) Grease

Use Toshiba's silicon YG6260 grease as this does not easily separate from its base oil and will not adversely affect the interior of the devices.

(7) Tightening torque

Use torque values less than those shown in Table 6.2 to obtain good thermal resistance and to avoid applying stress to the device.

Table 6.2 Package Mounting Torque Values

Package		Screw Tightening Torque (max, Unit: N • m)
JEDEC	Toshiba Name	
TO-220AB	2-10P1B	0.6
TO-220 (IS)	2-10L1B 2-10R1B	0.6
TO-3P (N)	2-16C1B	0.8
TO-3P (NIS)	2-16F1B	0.6
TO-3P (L)	2-21F1B	0.8

Screws, insulation spacers and insulation washers are also available from Toshiba as accessories.

7. Power Dissipation

7.1 Cautions About Drain Power Dissipation (constant state)

Power dissipation varies according to mounting conditions such as board sizes, materials and pad areas. Changes in drain power dissipation with respect to temperature for representative package types are described below.

7.1.1 PW-MINI Package

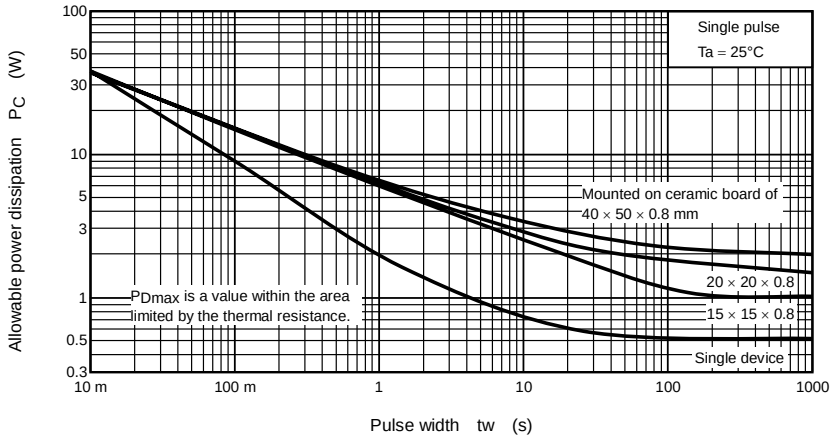


Figure 7.1 Allowable Power Dissipation in the Transient State (2SK2615)

7.1.2 PW-MOLD Package

The allowable power dissipation in a transient state is higher for pulse operation than in a saturation state. Allowable power dissipation vs. pulse width characteristic for the 2SK2399 is shown in Figure 7.2.

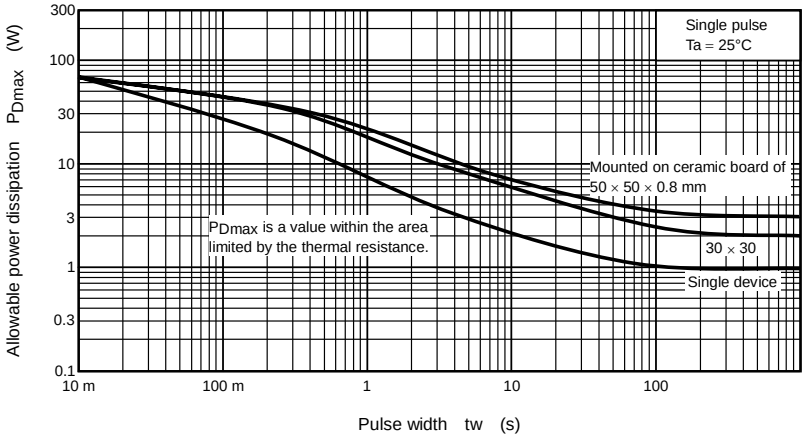


Figure 7.2 Allowable Power Dissipation vs. Pulse Width (2SK2399)

8. Minimum Pad Dimensions

8.1 PW-MINI

Figure 8.1 shows minimum pad dimensions and lead-attachment layout of a PW-MINI package. Drain power dissipation is greatly affected by the size of the drain-connection pad area; the largest size should be used for effective heat radiation.

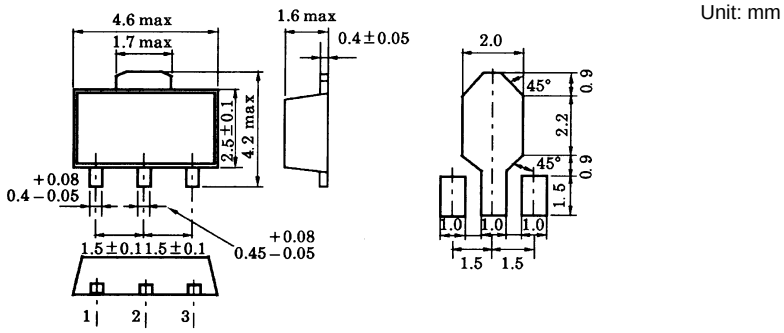


Figure 8.1 Minimum Pad Dimensions for a PW-MINI Package

8.2 PW-MOLD and DP

Thermal radiation from PW-MOLD and DP packages occurs mainly from the drain-fin, and if the conductive area of the device that contacts the fin is increased, drain power dissipation will also increase. Therefore, the conductive pattern of the drain section should be as large as possible.

Figure 8.2 shows the minimum pad dimensions for PW-MOLD and DP packages.

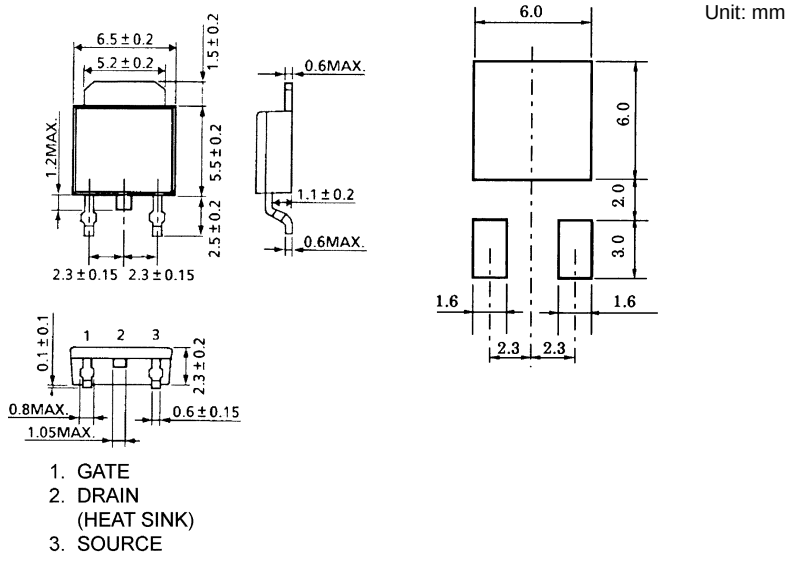
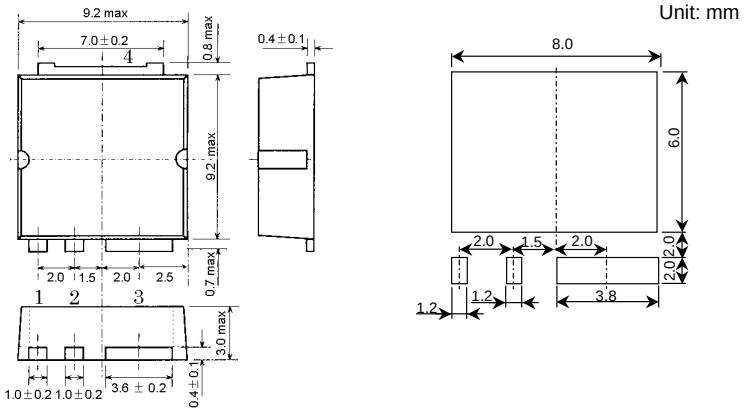


Figure 8.2 Minimum Pad Dimensions for PW-MOLD and DP Packages

8.3 TFP

The mounting-pad area of the drain fin should be as large as possible because the TFP package disperses heat mainly through the drain fin. Thus, the larger the mounting-pad area, the larger the power dissipation.

Figure 8.3 shows the minimum pad dimensions for a TFP package.



1. Gate: G
2. Source1: S1
3. Source2: S2
4. Drain: D

Figure 8.3 Minimum Pad Dimensions for a TFP Package

8.4 TO-220SM

The mounting-pad area of the drain fin should be as large as possible because the TO-220SM package disperses heat mainly through the drain fin. Thus, the larger the mounting-pad area, the larger the power dissipation.

Figure 8.4 shows the minimum pad dimensions for a TO-220SM package.

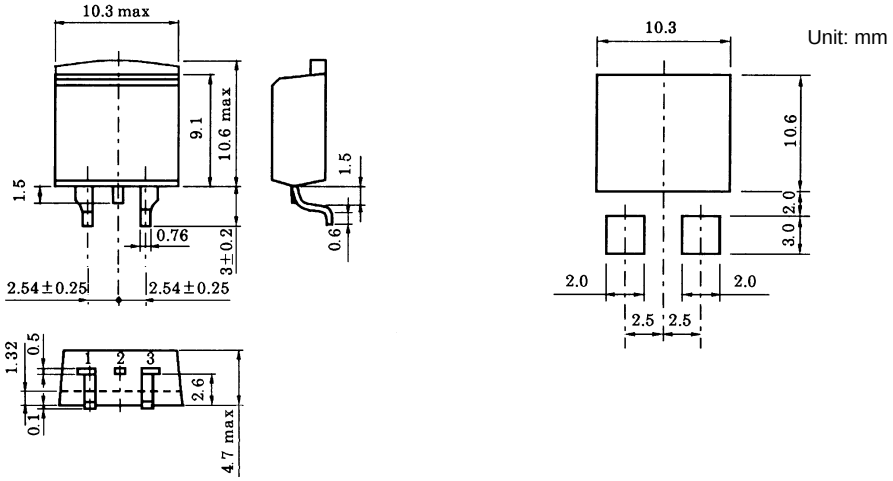


Figure 8.4 Minimum Pad Dimensions for a TO-220SM Package

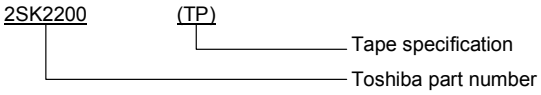
9. Tape Specifications

9.1 TPS Tape

9.1.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is given immediately below. (however, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Indicative Example]



9.1.2 Tape Specification

9.1.2.1 Tape Dimensions

The tape dimensions are as shown in Figure 9.1 and Table 9.1.

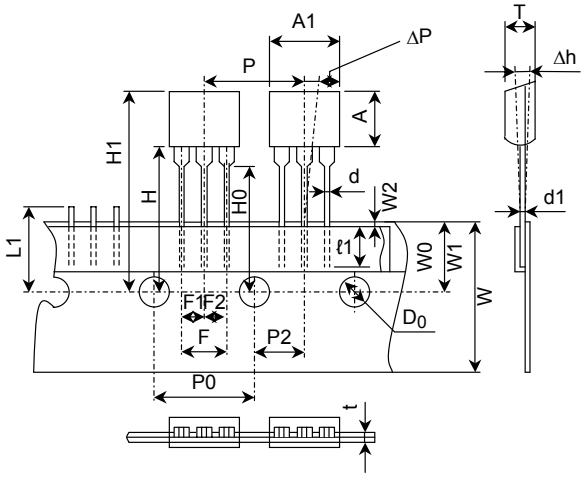


Figure 9.1 Tape Layout

Table 9.1 Tape Dimensions **Unit: mm**

Name	Symbol	Dimension	Note	Name	Symbol	Dimension	Note
Product width	A1	8.0±0.2		Tape width	W	$18.0^{+1.0}_{-0.5}$	
Product height	A	7.0±0.2		Attaching tape width	W0	6.0±0.5	
Product thickness	T	3.5±0.2		Carrier hole dislocation	W1	$9.0^{+0.75}_{-0.5}$	
Lead width	d	$0.5^{+0.15}_{-0.05}$		Attaching tape dislocation	W2	1.0 max	
Lead thickness	d1	$0.5^{+0.15}_{-0.05}$		Product bottom surface position	H	$17.5^{+0.75}_{-0.5}$	
Lead length attached to tape	ℓ1	4.0 min		Lead clinch height	H0	16.0±0.5	
Product pitch	P	12.7±1.0		Product upper-limit position	H1	32.25 max	
Feed hole pitch	P0	12.7±0.2	3	Carrier hole diameter	D_0	4.0±0.2	
Feed hole center to lead center	P2	6.35±0.5		Tape thickness	t	0.6±0.3	4
Lead spacing	F1/F2	$2.5^{+0.4}_{-0.1}$		Off-spec item cutting position	L1	11.0 max	
Product misalignment (1)	Δh	0±2.0					
Product misalignment (2)	ΔP	0±1.3					

Note 3: Cumulative pitch error tolerance is ±1 mm for 20 pitches.

Note 4: Board thickness is 0.4 ± 0.1 mm.

9.1.2.2 Packed Device Quantity

2000/pack

9.1.2.3 Ammo Pack Instruction

Device–bearing tapes are folded in an ammo pack with 24 devices in each row as shown in Figure 9.2.

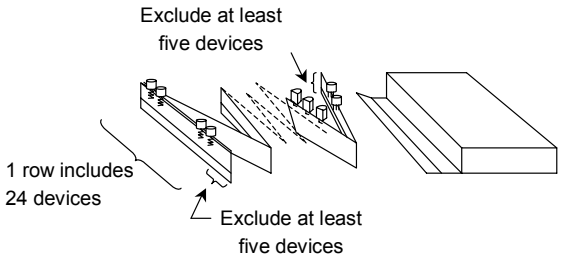


Figure 9.2 Ammo Pack Instruction

9.1.2.4 Leader and Trailer

There must be empty sections for at least 5 devices at the beginning and end of the tape.

9.1.2.5 Polarity of First-out of the Lead

The polarity of first-out of the lead is as shown in Figure 9.3.

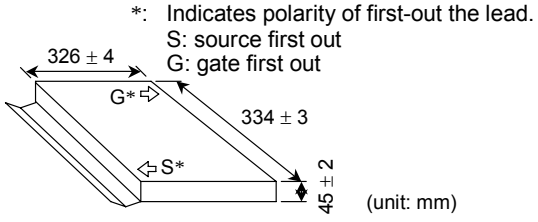


Figure 9.3 Ammo Pack Package

9.1.2.6 Ammo Pack Package

1: Material = paper

2: Dimensions are shown as in Figure 9.3.

9.1.2.7 Tape Splicing Method

The tape splicing method (at the end of a tape or when one is cut) is shown in the figure below—cut the tape and connect the ends with the splicing tape.

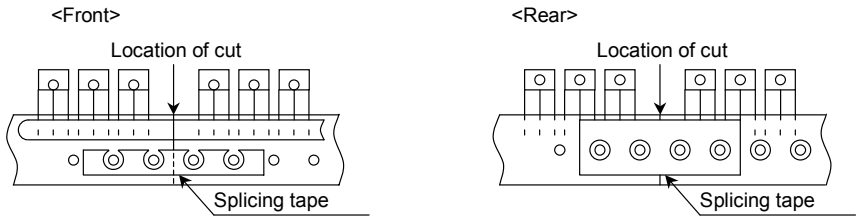


Figure 9.4 How to Splice a Tape

9.1.2.8 Joint Alignment

Dimension 'a' must be within 1 mm/20 pitches.

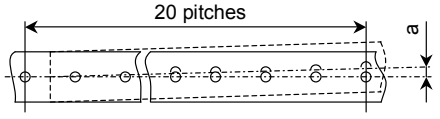
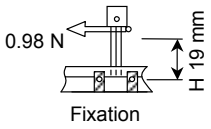
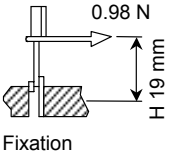
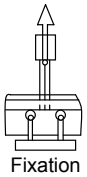


Figure 9.5 Joint Accuracy

9.1.2.9 Fall-out

Device fall-out should be not more than three consecutively.

9.1.2.10 Taped Device Attachment Security Test

Item	Testing Method	Required Performance
Skew resistance	(a) Lengthwise direction Apply 1 N load in the direction of the arrow for 3 ± 1 seconds. 	Fulfills tape packing specifications.
	(b) Transverse direction Apply 1 N load in the direction of the arrow for 3 ± 1 seconds. 	Fulfills tape packing specifications.
Extraction resistance	(a) Intensity test Apply a load of at least 4.9 N in the direction of the arrow. 	There should be no lead dislocation.
	(b) Life test Leave open for 6 months in a normal temperature and normal humidity.	Required to satisfy extraction resistance performance standard '(a)' above.

9.1.3 Others

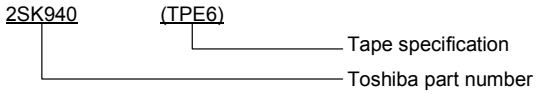
The electrical characteristics of taped devices are given in relevant technical datasheets.

9.2 TO-92 MOD Type Ammo Tape

9.2.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is listed below. (however, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Indicative Example]



9.2.2 Tape Specifications

9.2.2.1 Tape Dimensions

The tape dimensions are as shown in Figure 9.6 and Table 9.2.

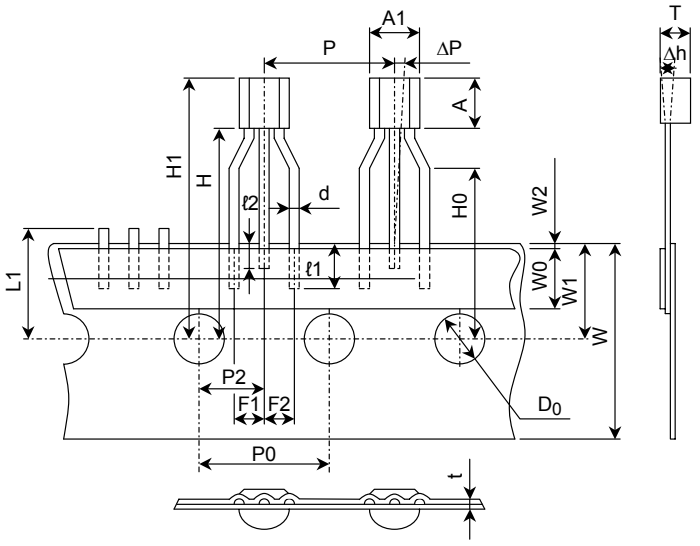


Figure 9.6 Tape Layout

Table 9.2 Tape Dimensions **Unit: mm**

Name	Symbol	Dimension	Note	Name	Symbol	Dimension	Note
Product width	A1	5.1 max		Tape width	W	$18.0^{+1.0}_{-0.5}$	
Product height	A	8.2 max		Attaching tape width	W0	6.0 ± 0.3	
Product thickness	T	4.1 max		Carrier hole dislocation	W1	9.0 ± 0.5	
Lead width	d	0.65□ max		Attaching tape dislocation	W2	0.5 max	
Lead length attached to tape	ℓ1	3.5 min		Product bottom surface position	H	20.0 max	
Product pitch	P	12.7 ± 0.5		Lead clinch height	H0	$16.3^{+0.2}_{-0.8}$	
Feed hole pitch	P0	12.7 ± 0.15	5	Product upper-limit position	H1	28.0 max	
Feed hole center to lead center	P2	6.35 ± 0.4		Carrier hole diameter	D_0	4.0 ± 0.2	
Lead spacing	F1/F2	$2.5^{+0.5}_{-0.3}$		Tape thickness	t	0.6 ± 0.2	6
Product misalignment (1)	Δh	0 ± 2.0		Off-spec item cutting position (total thickness)	L1	11.0 max	
Product misalignment (2)	ΔP	0 ± 1.0		Length of overlap between center lead and cover tape	ℓ2	2.1 typ.	

Note 5: Cumulative pitch dimension error tolerance is ±1 mm for 20 pitches.

Note 6: Board thickness is 0.4 ± 0.1 mm.

9.2.2.2 Packed Device Quantity

2000/pack

9.2.2.3 Ammo Pack Instruction

Device–bearing tapes are folded in an ammo pack with 25 devices in each row as shown in Figure 9.7.

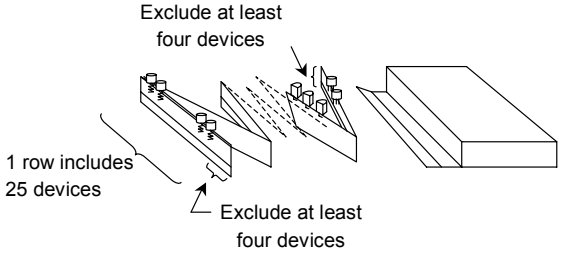


Figure 9.7 Ammo Pack Instructions

9.2.2.4 Leader and Trailer

There must be empty sections for at least 4 devices at the beginning and end of the tape.

9.2.2.5 Polarity of First-out of the Lead

The polarity of first-out of the lead is as shown in Figure 9.8.

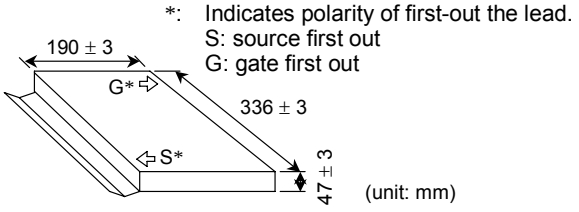


Figure 9.8 Ammo Pack Package

9.2.2.6 Ammo Pack Package

1: Material = paper

2: Dimensions are shown as in Figure 9.8.

9.2.2.7 Tape Splicing Method

The tape splicing method (at the end of a tape or when one is cut) is shown in the figure below—cut the tape and connect the ends with the splicing tape.

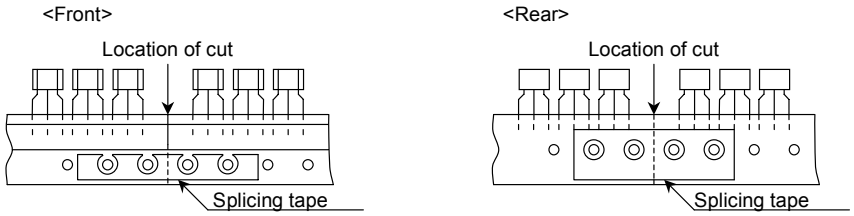


Figure 9.9 How to Splice a Tape

9.2.2.8 Joint Alignment

Dimension 'a' must be within 1 mm/20 pitches.

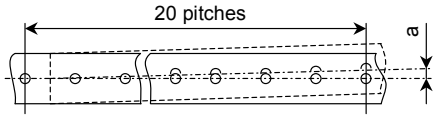
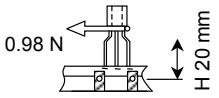
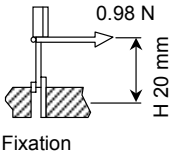
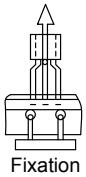


Figure 9.10 Joint Accuracy

9.2.2.9 Fall-out

Device fall-out should be not more than three consecutively.

9.2.2.10 Taped Device Attachment Security Test

Item	Testing Method	Required Performance
Skew resistance	(a) Lengthwise direction Apply 0.9 N load in the direction of the arrow for 3 ± 1 seconds. 	Fulfills tape packing specifications.
	(b) Transverse direction Apply 0.9 N load in the direction of the arrow for 3 ± 1 seconds. 	Fulfills tape packing specifications.
Extraction resistance	(c) Intensity test Apply a load of at least 4.9 N in the direction of the arrow. 	At least 4.9 N. There should be no lead dislocation.
	(d) Life test Leave open for 6 months in a normal temperature and normal humidity.	Required to satisfy extraction resistance performance standard '(a)' above.

9.2.3 Others

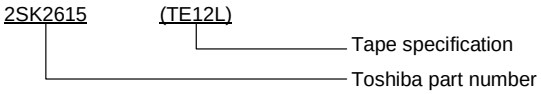
The electrical characteristics of taped devices are given in relevant technical datasheets.

9.3 Tape Specifications for PW-MINI Package

9.3.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is listed below. (However, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Indicative Example]



9.3.2 Tape Specification

9.3.2.1 Tape Specification is as Shown in Table 9.3.

Table 9.3 Tape Specification

Tape Type	L or R
TE12L	L
TE12R	R

9.3.2.2 Device Orientation

Device orientation on the carrier tape is as shown in Figure 9.11.

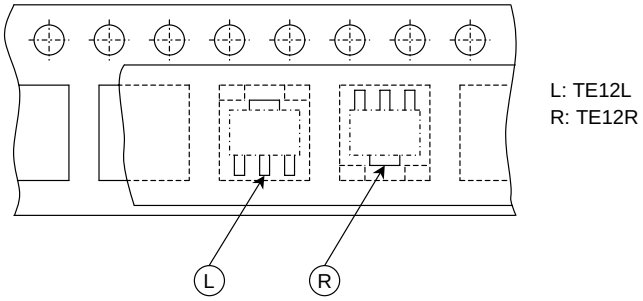


Figure 9.11 Device Orientation

9.3.2.3 Tape Dimensions

1: Cumulative pitch error tolerance is ±0.2 mm or less / 10 pitches

2: The tape material is plastic with carbon (black).

3: The tape dimensions are as shown in Figure 9.12.

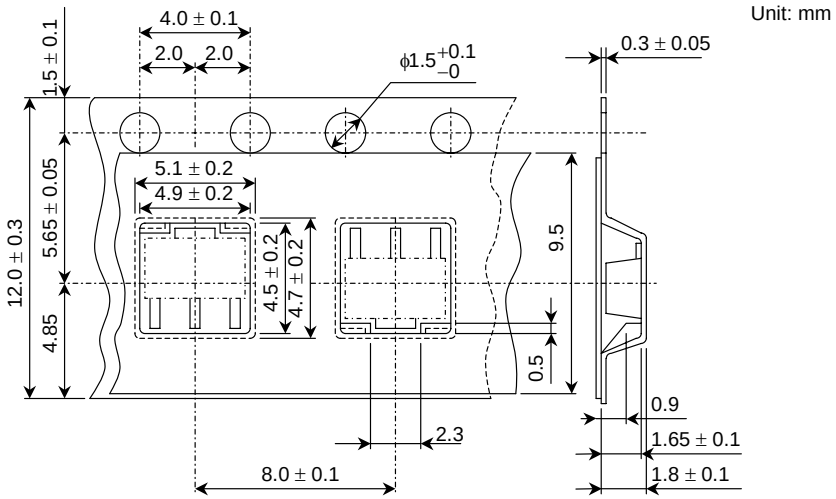


Figure 9.12 Tape Form and Dimensions

9.3.2.4 Packing Quantity

1000/reel

9.3.2.5 Empty Device Recesses Are as Shown in Table 9.4.

Table 9.4 Empty Device Recess

Parameters	Specification
Occurrences of 2 or more successive empty device recesses	0
Single empty device recesses	0.2% max/reel

9.3.2.6 Reel

1: Material: Plastic

2: Dimensions are as shown in Figure 9.13

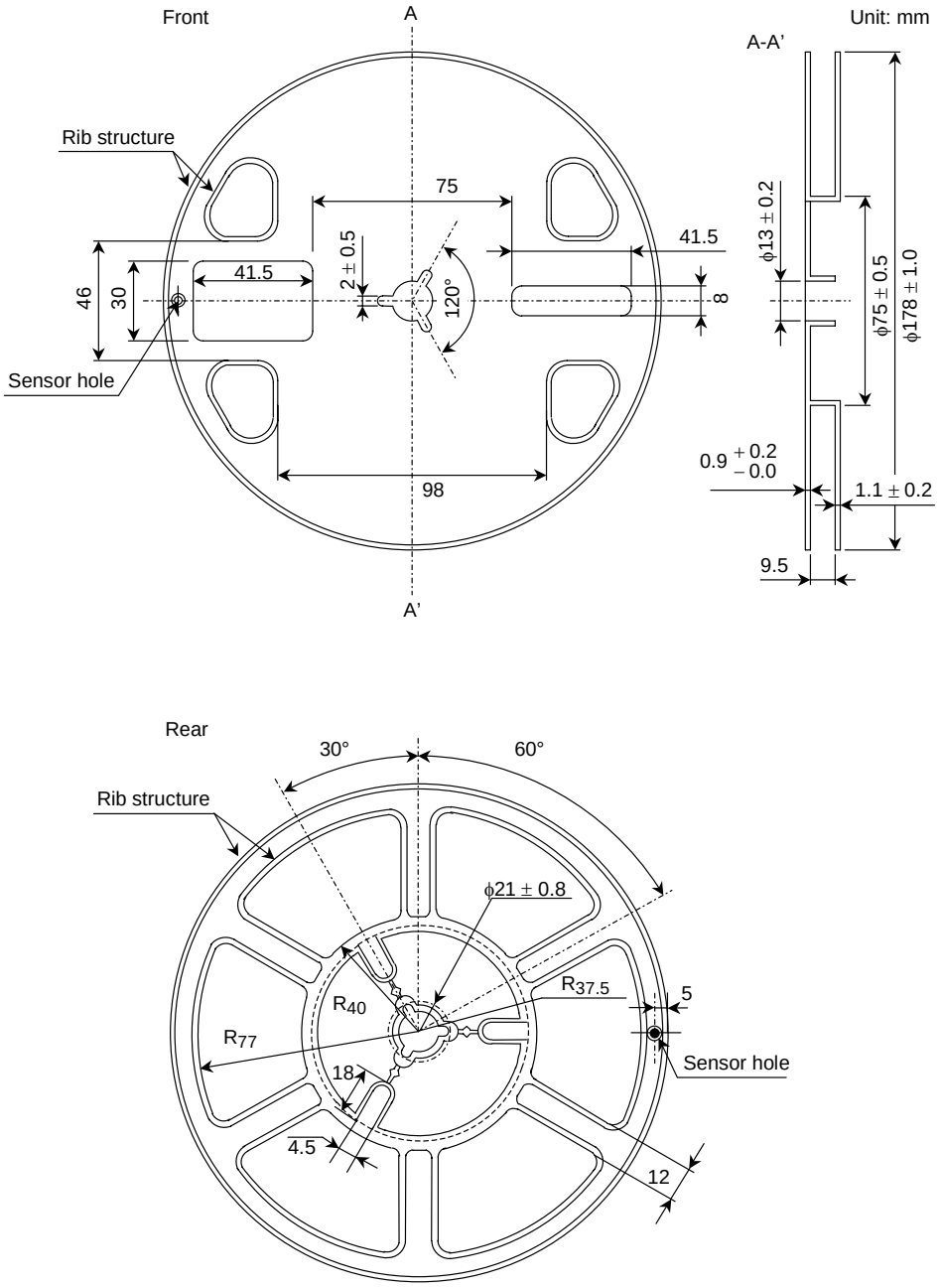


Figure 9.13 Reel Form and Dimensions

9.3.3 Label

The label markings may include the product number; tape type, quantity, lot number, Toshiba logo and country of origin. The position of the label is as shown in Figure 9.14.

Label example: 2SK2615 (TE12L)

TYPE	2SK2615		
ADDC	(TE12L)	Q'ty	pcs
NOTE			

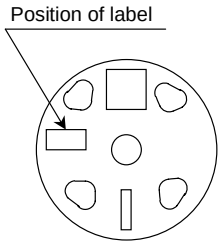
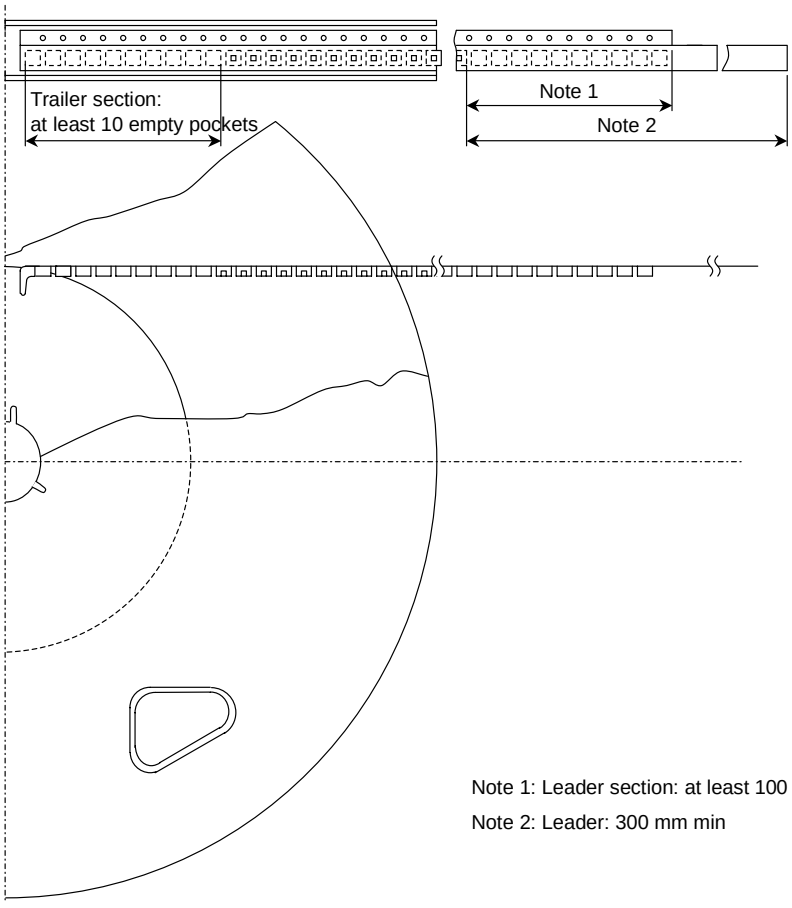


Figure 9.14 Reel Front

9.3.4 Leader and Trailer



Note 1: Leader section: at least 100 mm of carrier tape

Note 2: Leader: 300 mm min

9.3.5 Others

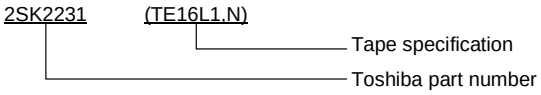
The electrical characteristics of taped devices are given in the relevant technical datasheets.

9.4 Tape Specifications for PW-MOLD Package

9.4.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is listed below. (However, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Indicative Example]



9.4.2 Tape Specification

9.4.2.1 Tape Specification is as Shown in Table 9.5.

Table 9.5 Tape Specification

Tape Type	L or R
TE16L1	L
TE16R1	R

9.4.2.2 Device Orientation

Device orientation on the carrier tape is as shown in Figure 9.15.

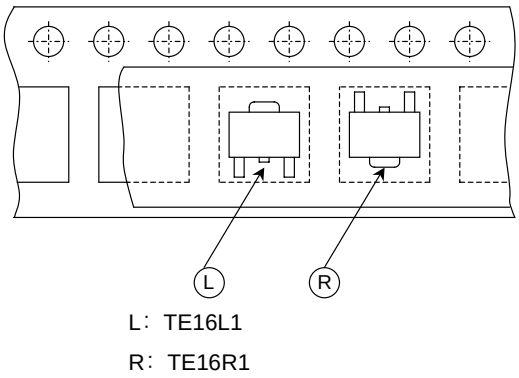


Figure 9.15 Device Orientation

9.4.2.3 Tape Dimensions

1: Cumulative pitch error tolerance is ±0.2 mm or less / 10 pitches

2: The tape material is plastic with carbon (black).

3: The tape dimensions are as shown in Figure 9.16.

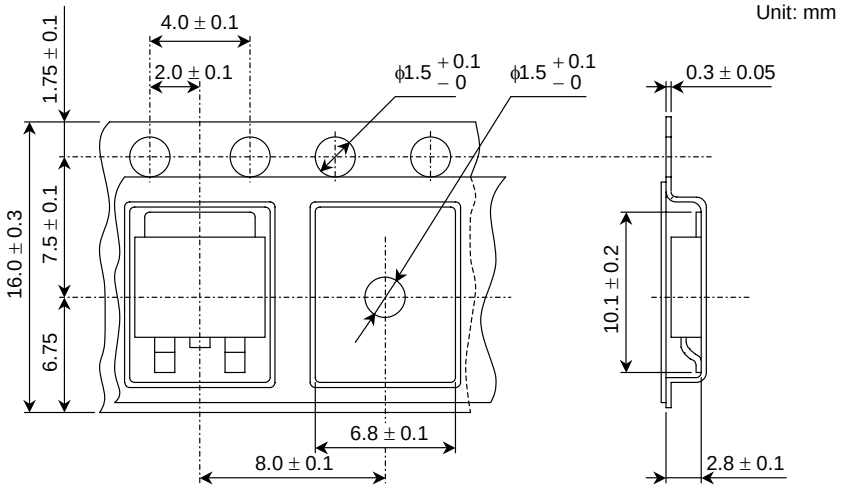


Figure 9.16 Tape Form and Dimensions

9.4.2.4 Packing Quantity

2000/reel

9.4.2.5 Empty Device Recesses Are as Shown in Table 9.6.

Table 9.6 Empty Device Recess

Parameters	Specification
Occurrences of 2 or more successive empty device recesses	0
Single empty device recesses	0.2% max/reel

9.4.2.6 Reel

1: Material: Plastic with carbon

2: Dimensions are as shown in Figure 9.17

Unit: mm

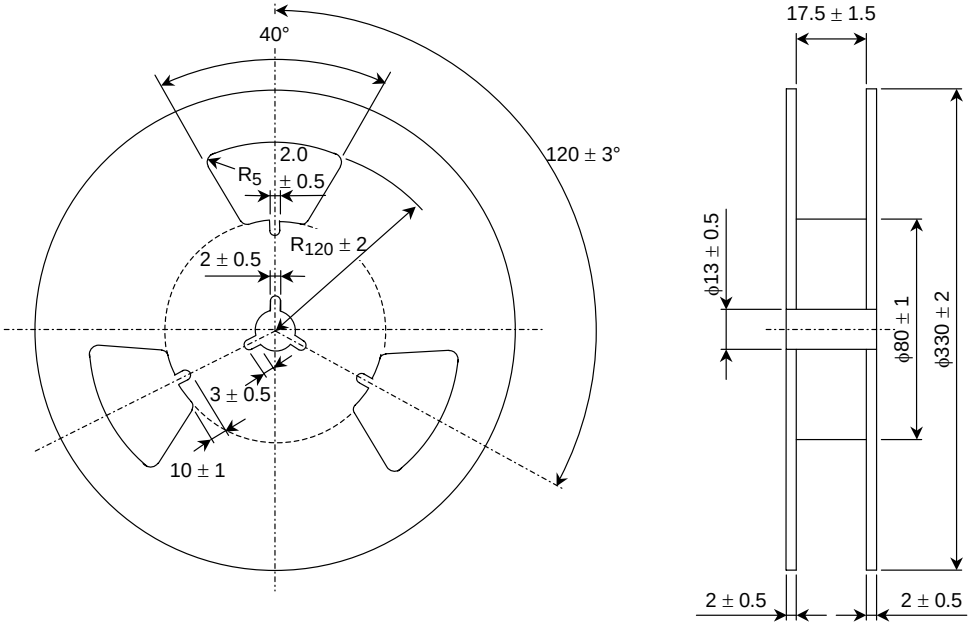


Figure 9.17 Reel Form and Dimensions

9.4.3 Label

The label markings may include the product number; tape type, quantity, lot number, Toshiba logo and country of origin. The position of the label is as shown in Figure 9.18.

Label example

TYPE	2SK××××		
ADDC	(TE16□1, N)	Q'ty	pcs
NOTE			

Label on the reel may also include ADD.CODE PART Number.

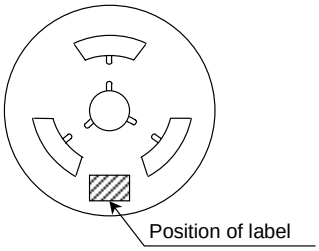
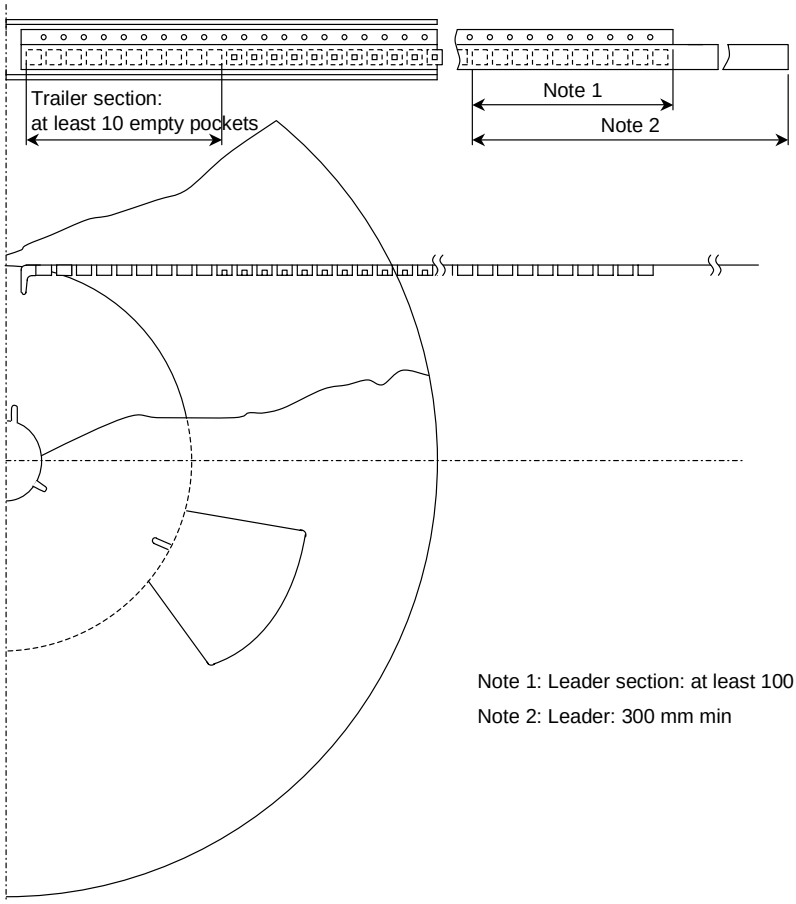


Figure 9.18 Reel Front

9.4.4 Leader and Trailer



Note 1: Leader section: at least 100 mm of carrier tape

Note 2: Leader: 300 mm min

9.4.5 Others

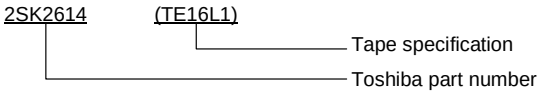
The electrical characteristics of taped devices are given in the relevant technical datasheets.

9.5 Tape Specifications for DP Package

9.5.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is listed below. (However, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Example]



9.5.2 Tape Specification

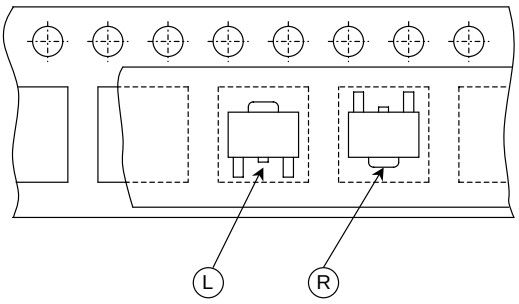
9.5.2.1 Tape Specification is as Shown in Table 9.7.

Table 9.7 Tape Specification

Tape Type	L or R
TE16L1	L
TE16R1	R

9.5.2.2 Device Orientation

Device orientation on the carrier tape is as shown in Figure 9.19.



L: TE16L1

R: TE16R1

Figure 9.19 Device Orientation

9.5.2.3 Tape Dimensions

1: Cumulative pitch error tolerance is ±0.2 mm or less / 10 pitches

2: The tape material is plastic with carbon (black).

3: The tape dimensions are as shown in Figure 9.20.

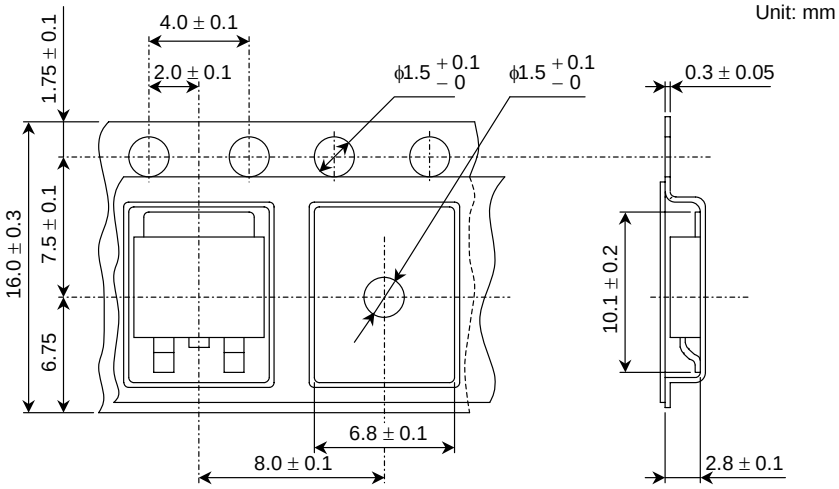


Figure 9.20 Tape Form and Dimensions

9.5.2.4 Packing Quantity

2000/reel

9.5.2.5 Empty Device Recesses Are as Shown in Table 9.8.

Table 9.8 Empty Device Recess

Parameters	Specification
Occurrences of 2 or more successive empty device recesses	0
Single empty device recesses	0.2% max/reel

9.5.2.6 Reel

1: Material: Plastic with carbon

2: Dimensions are as shown in Figure 9.21

Unit: mm

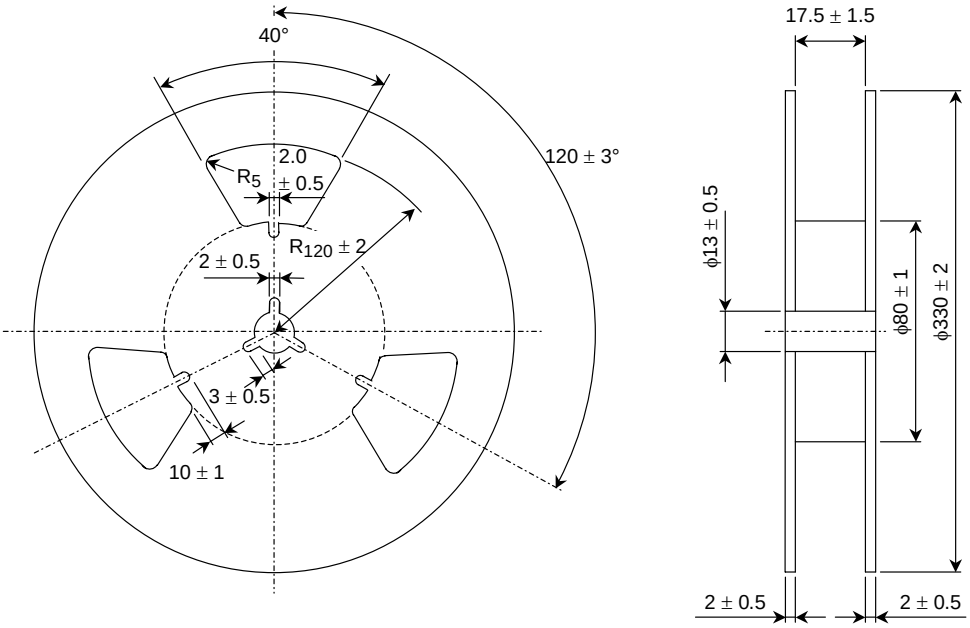


Figure 9.21 Reel Form and Dimensions

9.5.3 Label

The label markings may include the product number; tape type, quantity, lot number, Toshiba logo and country of origin. The position of the label is as shown in Figure 9.22.

Label example

TYPE	2SK××××		
ADDC	(TE16□1)	Q'ty	pcs
NOTE			

Label on the reel may also include ADD.CODE PART Number.

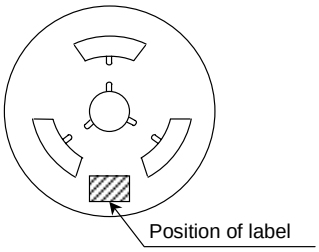
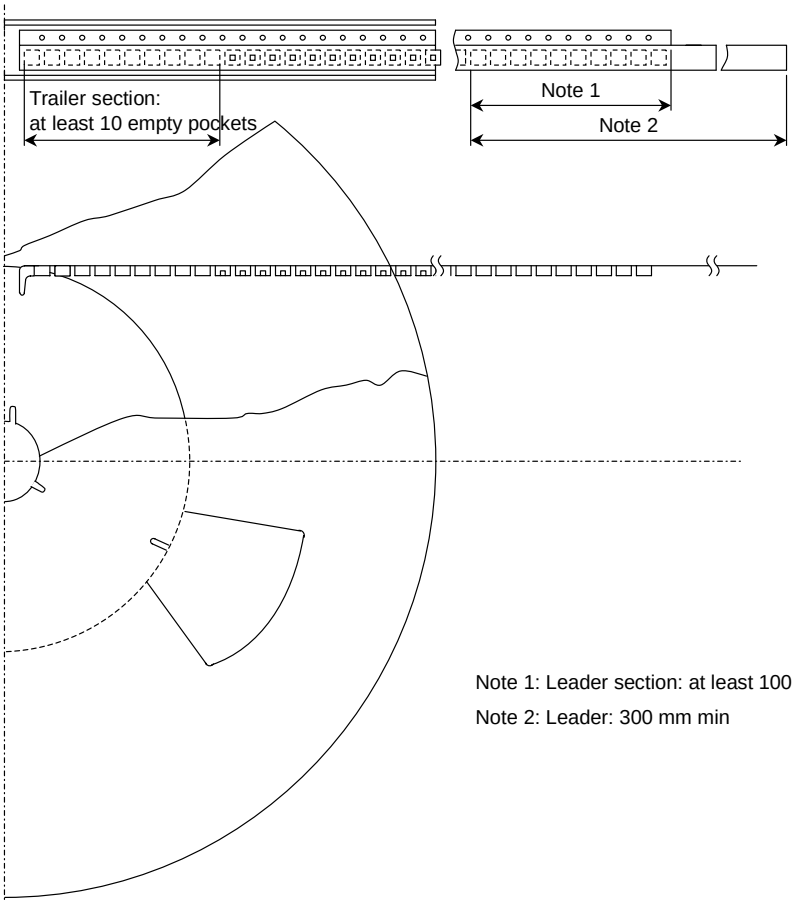


Figure 9.22 Reel Front

9.5.4 Leader and Trailer



Note 1: Leader section: at least 100 mm of carrier tape

Note 2: Leader: 300 mm min

9.5.5 Others

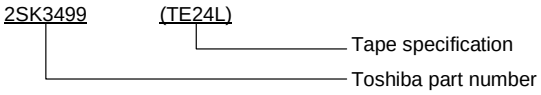
The electrical characteristics of taped devices are given in the relevant technical datasheets.

9.6 Tape Specifications for TFP Package

9.6.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is listed below. (However, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Example]



9.6.2 Tape Specification

9.6.2.1 Tape Specification Is as Shown in Table 9.9.

Table 9.9 Tape Specification

Tape Type	L or R
TE24L	L
TE24R	R

9.6.2.2 Device Orientation

Device orientation on the carrier tape is as shown in Figure 9.23.

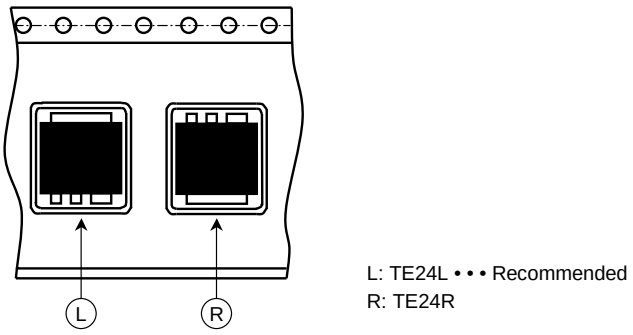


Figure 9.23 Device Orientation

9.6.2.3 Tape Dimensions

1: Cumulative pitch error tolerance is ±0.2 mm or less / 10 pitches

2: The tape material is plastic with carbon (black).

3: The tape dimensions are as shown in Figure 9.24.

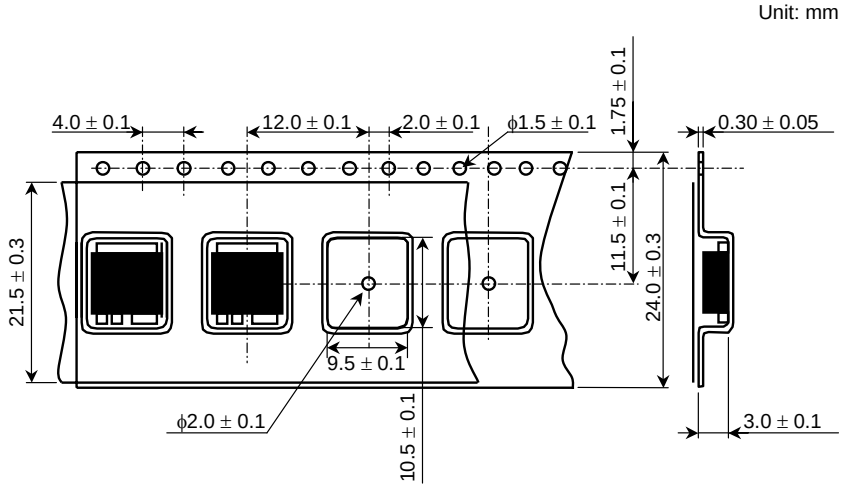


Figure 9.24 Tape Form and Dimensions

9.6.2.4 Packing Quantity

1500/reel

9.6.2.5 Empty Device Recesses Are as Shown in Table 9.10.

Table 9.10 Empty Device Recess

Parameters	Specification
Occurrences of 2 or more successive empty device recesses	0
Single empty device recesses	0.2% max/reel

9.6.2.6 Reel

1: Material: Plastic with carbon

2: Dimensions are as shown in Figure 9.25

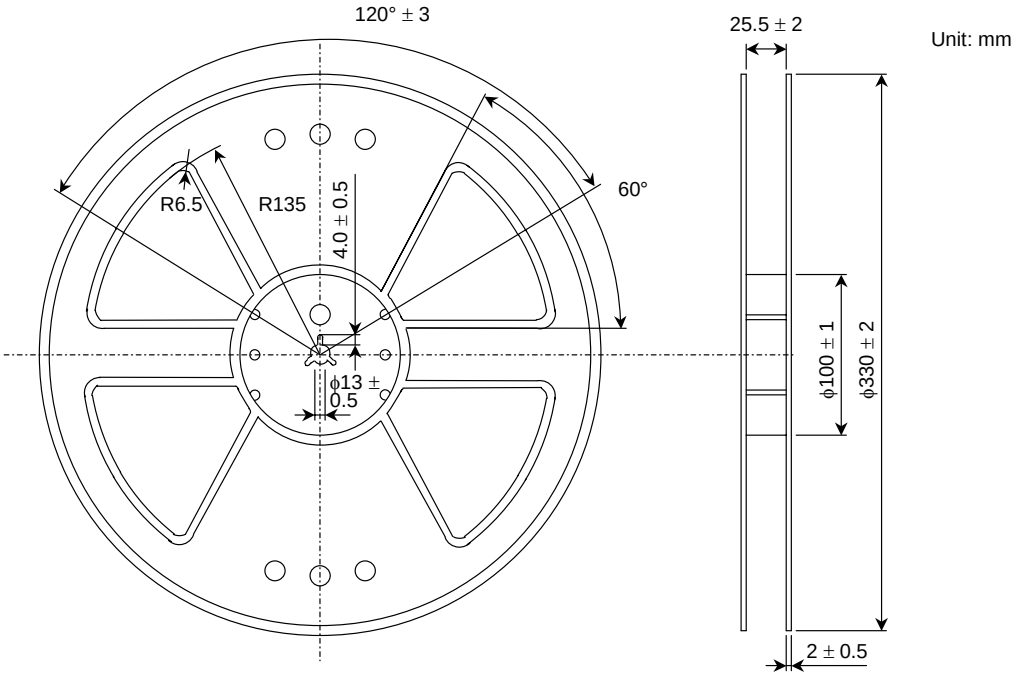


Figure 9.25 Reel Form and Dimensions

9.6.3 Label

The label markings may include the product number; tape type, quantity, lot number, Toshiba logo and country of origin. The position of the label is as shown in Figure 9.26.

Label example

TYPE	2SK××××		
ADDC	(TE24□)	Q'ty	pcs
NOTE			

Label on the reel may also include ADD.CODE PART Number.

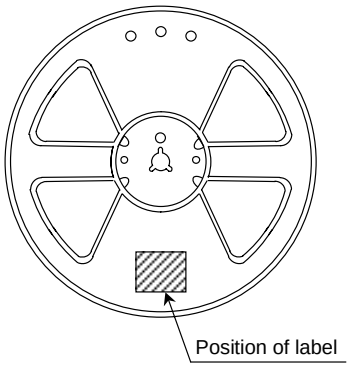
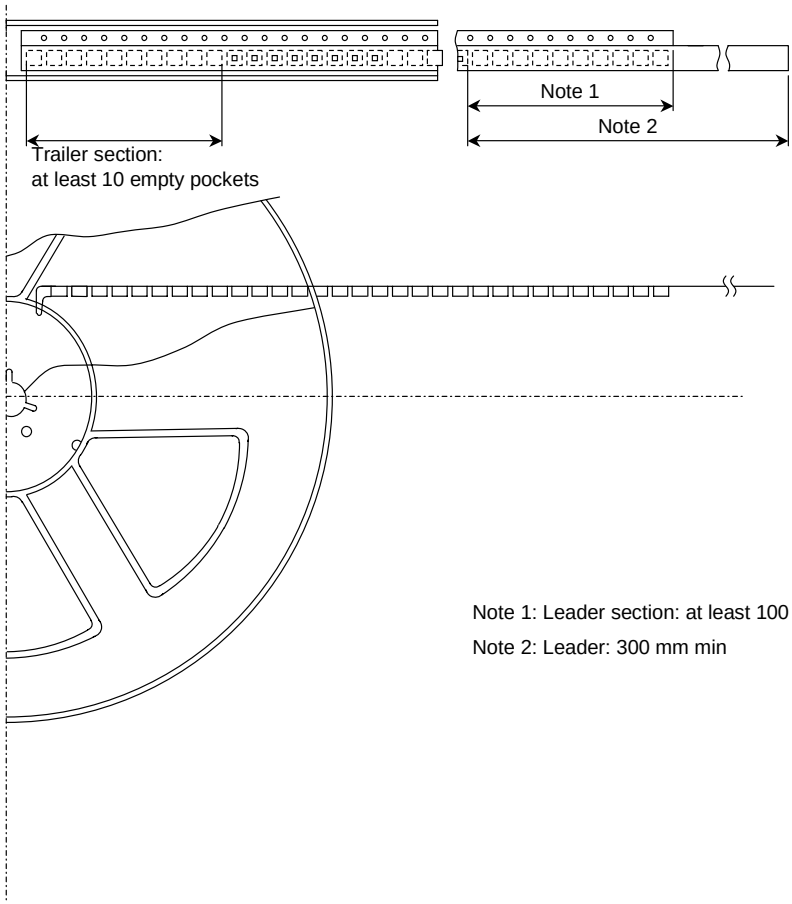


Figure 9.26 Reel Front

9.6.4 Leader and Trailer



Note 1: Leader section: at least 100 mm of carrier tape

Note 2: Leader: 300 mm min

9.6.5 Others

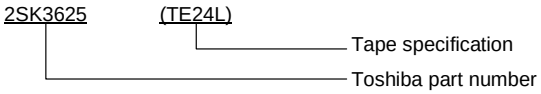
The electrical characteristics of taped devices are given in the relevant technical datasheets.

9.7 Tape Specifications for TO-220SM Package

9.7.1 Product Naming

Symbols indicated after product numbers are for specifying packing classification. A typical indication is listed below. (However, this classification does not apply to products that are not subject to Toshiba standard specifications for their electrical characteristics.)

[Example]



9.7.2 Tape Specification

9.7.2.1 Tape Specification is as Shown in Table 9.11.

Table 9.11 Tape Specification

Tape Type	L or R
TE24L	L
TE24R	R

9.7.2.2 Device Orientation

Device orientation on the carrier tape is as shown in Figure 9.26.

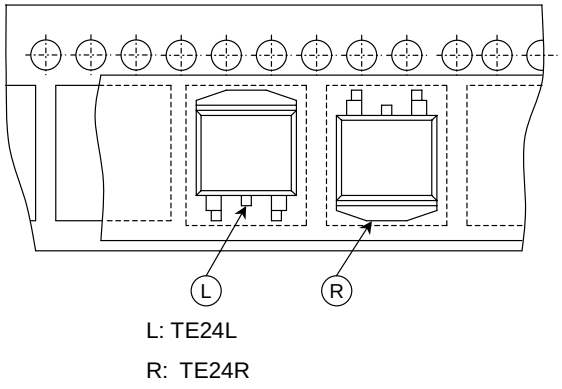


Figure 9.26 Device Orientation

9.7.2.3 Tape Dimensions

1: Cumulative pitch error tolerance is ±0.2 mm or less / 10 pitches

2: The tape material is plastic with carbon (black).

3: The tape dimensions are as shown in Figure 9.27.

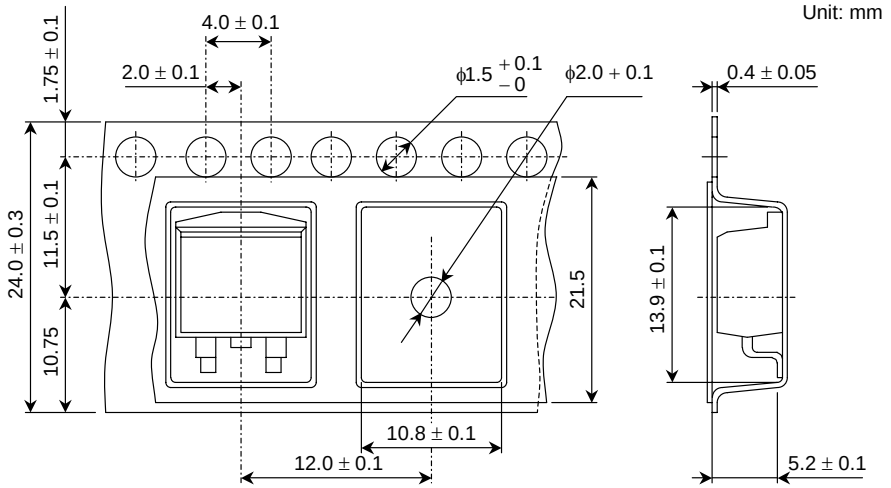


Figure 9.27 Tape Form and Dimensions

9.7.2.4 Packing Quantity

1000/reel

9.7.2.5 Empty Device Recesses Are as Shown in Table 9.12.

Table 9.12 Empty Device Recess

Parameters	Specification
Occurrences of 2 or more successive empty device recesses	0
Single empty device recesses	0.2% max/reel

9.7.2.6 Reel

1: Material: Plastic with carbon

2: Dimensions are as shown in Figure 9.28

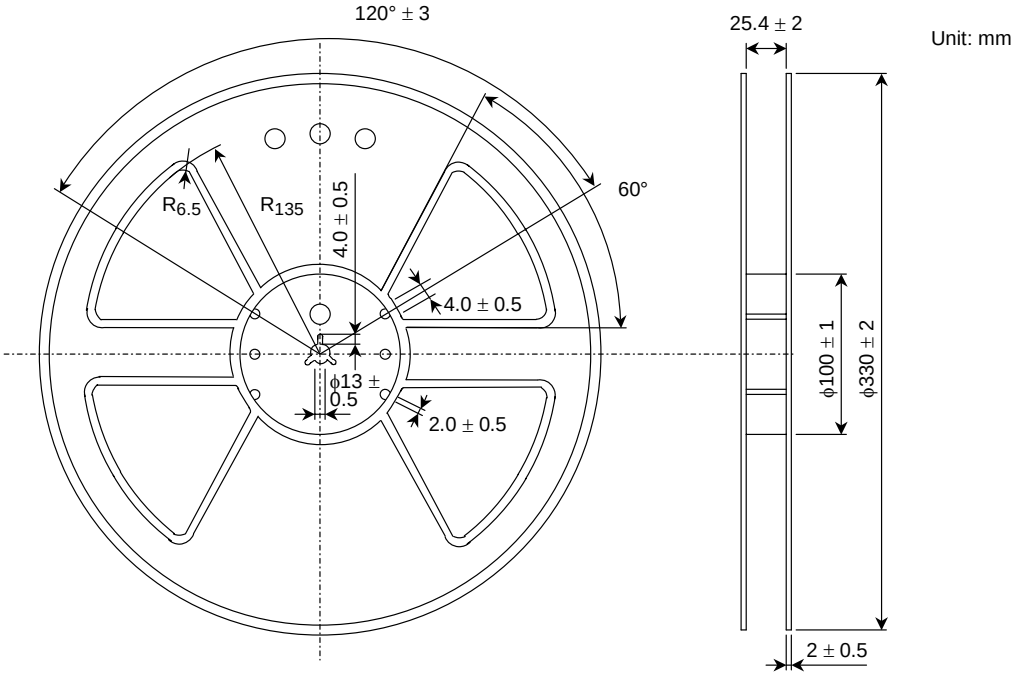


Figure 9.28 Reel Form and Dimensions

9.7.3 Label

The label markings may include the product number; tape type, quantity, lot number, Toshiba logo and country of origin. The position of the label is as shown in Figure 9.29.

Label example

TYPE	2SK××××		
ADDC	(TE24□)	Q'ty	pcs
NOTE			

Label on the reel may also include ADD.CODE PART Number.

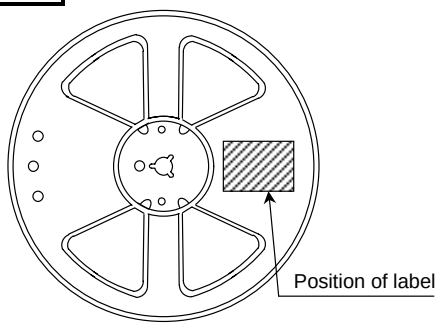
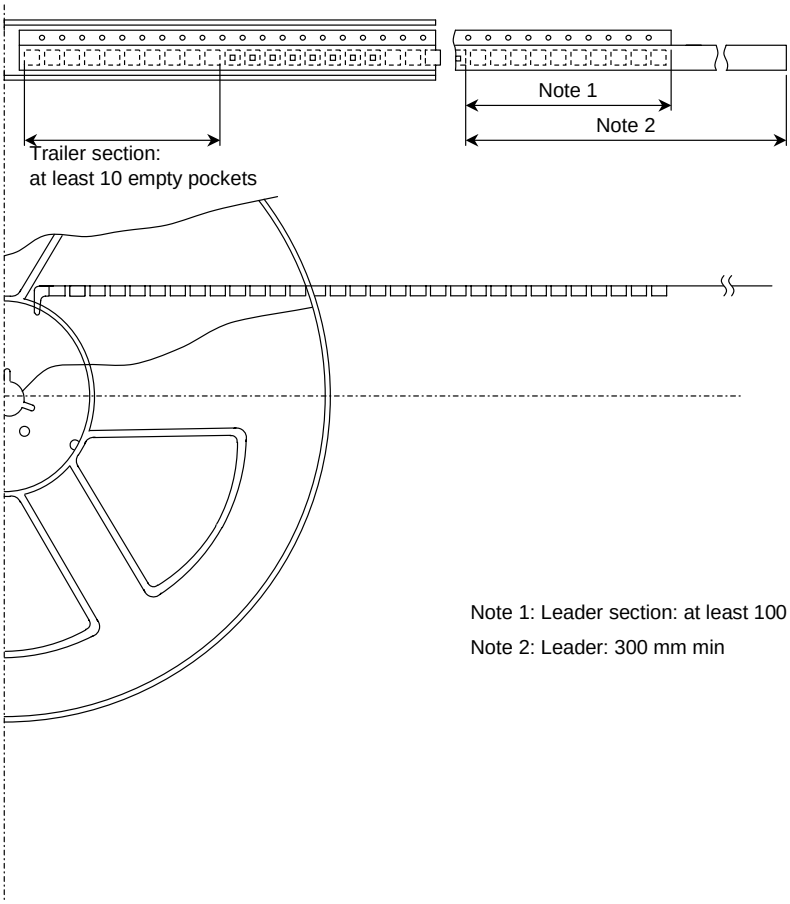


Figure 9.29 Reel Front

9.7.4 Leader and Trailer



Note 1: Leader section: at least 100 mm of carrier tape

Note 2: Leader: 300 mm min

9.7.5 Others

The electrical characteristics of taped devices are given in the relevant technical datasheets.

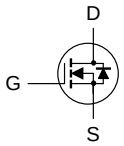
10. Letter Symbols and Graphical Symbols

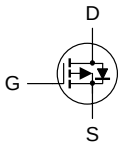
10.1 Power MOSFET Characteristics

Letter Symbol

Symbol	Explanation	Symbol	Explanation
C_{iss}	Input capacitance	$t_{d\ (on)}$	Turn-ON delay time
C_{oss}	Output capacitance	t_r	Rise time
C_{rss}	Reverse transfer capacitance	t_{on}	Turn-ON time
I_D	Drain current	$t_{d\ (off)}$	Turn-OFF delay time
I_{DP}	Drain current (pulse)	t_f	Fall time
I_{DR}	Drain reverse current	t_{off}	Turn-OFF time
I_{DRP}	Drain reverse current (pulse)	V_{DGR}	Drain-gate voltage
I_{DSS}	Drain cutoff current	$V_{DS\ (ON)}$	Drain-source ON voltage
I_{GSS}	Gate leakage current	V_{DS}	Drain-source voltage
P_D	Drain power dissipation	V_{DSX}	Drain-source voltage
Q_g	Total gate charge	V_{DSF}	Drain-source forward voltage (diode)
Q_{gd}	Gate-drain (“Miller”) charge	V_{DSS}	Drain-source voltage
Q_{gs}	Gate-source charge	V_{GS}	Gate-source voltage
$R_{DS\ (ON)}$	Drain-source ON resistance	V_{GSS}	Gate-source voltage
$R_{th\ (ch-a)}$	Channel-ambient thermal resistance	$V_{\ (BR)\ DSS}$	Drain-source breakdown voltage
$R_{th\ (ch-c)}$	Channel-case thermal resistance	V_{th}	Gate threshold voltage
SOA	Safe operating area	$\|Y_{fs}\|$	Forward transfer admittance
T_{ch}	Channel temperature	t_{rr}	Reverse recovery time
T_{stg}	Storage temperature	Q_{rr}	Reverse recovery charge

Graphic Symbols

Device	Graphic Symbol
N-channel MOS enhancement-type field effect transistor	

Device	Graphic Symbol
P-channel MOS enhancement-type field effect transistor	

- The characters and numerals included in the graphic symbols are for explanation purposes and are not part of the symbols. The characters are defined as follows.
  D: Drain
  G: Gate
  S: Source

- The following package symbols are omitted when confusion might not result, and when a device is not connected to an external package.