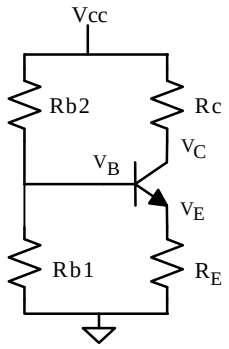
DC Biasing of BJT Amplifiers

A traditional "4-resistor bias circuit" is shown below.



Bias circuit analysis

Assume the transistor is operating in the active region, and that h_{FE} is "large". Then, I_b will be approximately zero (relative to the current in R_{b1}, R_{b2}), and we can use the simple voltage divider formula at the base to get,

$$V_B = V_{cc}\frac{Rb1}{Rb1+Rb2}$$

If the transistor is in the active region, the BE junction is forward biased and $V_{BE} \approx 0.6V$. Hence,

$$V_E \approx V_B - 0.6$$

The emitter current is then,

$$I_E = \frac{V_E}{R_E}$$

and the collector current is,

$$I_C \approx I_E$$

Finally, the collector voltage can be found from the IR drop in Rc as,

$$V_C = V_{CC} - I_C R_C$$

Note that these equations are independent of the exact transistor gain h_{FE} , provided the assumption that the current in R_{b1}, R_{b2} is >> the base current is valid. Hence, the bias voltages and currents should not change significantly with changes in h_{FE} if R_{b1} and R_{b2} are selected to satisfy this assumption.

Note also that the bias current and bias voltages will be relatively insensitive to small variations in V_{BE} caused by temperature or manufacturing, provided that V_E is greater than about 0.5 to 1 volt.

Bias Circuit Design

The following procedure is based on the simplified analysis on the previous page.

Pick $V_E > 0.5$ V to swamp V_{BE} variations due to manufacturing and temperature changes. (But not so high that it significantly degrades the output signal swing you can achieve.)

Pick R_E to give the desired I_E. (or the desired I_C since the two are approximately equal).

Find V_B from $V_B \approx V_E + 0.6$.

Find I_{Bmax} from I_C and the minimum transistor h_{FE} value in the data sheet.

Find R_{b1} and R_{b2} to produce the value of V_B above, subject to the constraint that the current in R_{b1}, R_{b2} is much greater than I_{Bmax}. (Typically 5 to 10 times I_{Bmax} is used.)

Fine-tune R_{b1} and R_{b2} if desired to account for the (small) lowering of V_B due to the non-zero base current expected (use typical h_{FE} here to provide good "design-centering").

Find R_c to produce a desired V_C or to satisfy other design constraints such as the amplifier gain.

Check to be sure the transistor is operating in the active region !!