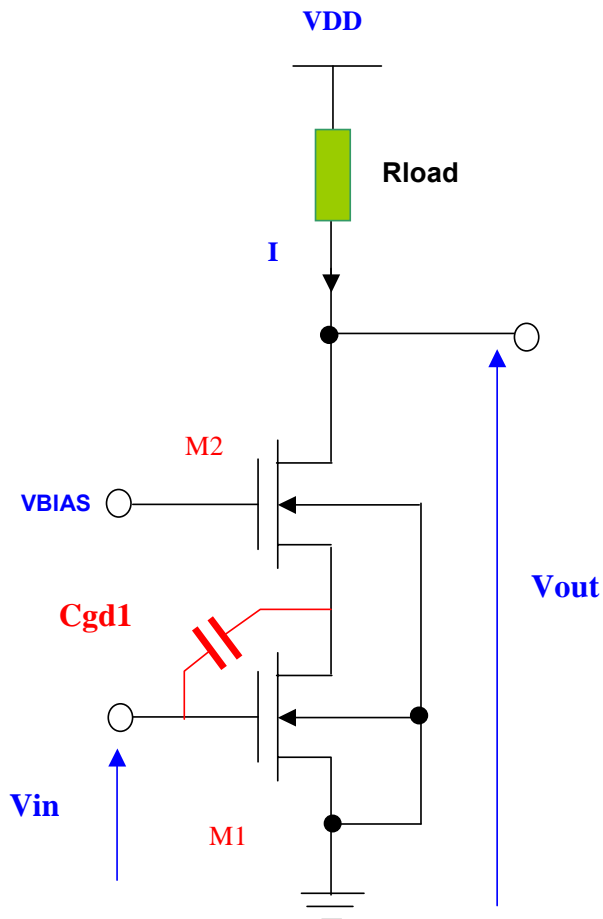


**Cascode CMOS Circuit**

The cascode is a combination of a common-source device with a common-gate load. This has the effect of increasing the output impedance but minimises the Miller effect making it an ideal configuration for use at high frequencies. The circuit of the cascode amplifier is shown in Figure 1.



**Figure 1 Basic Cascode Amplifier**

Lets assume that FET M2 has a short between the drain and source terminals, the remaining circuit will be a common-source amplifier with a gain of:

$$Av = gm_1 \cdot R_{LOAD} \text{ or } \frac{gm_1}{g_{load}} \text{ strictly speaking } Av = \frac{gm_1}{g_{load} + g_{o1}}$$



Now miller effect occurs when there is a large impedance applied to the drain of the common-source M1 in this case it's  $R_{LOAD}$  but it could also be an active load with an even higher resistance. This has the effect of applying a gate shunt capacitance which, has a value of the M1 gate-drain capacitance multiplied by the voltage gain of the amplifier:-

$$C_{gate-shunt} = C_{gd1}(1 + (gm_1 \cdot R_{LOAD}))$$

Thus with a particular source impedance connected to the input of the amplifier the 3-dB break point will be:-

$$f_{3dB} = \frac{1}{2\pi \cdot R_s [C_{gs} + C_{gd1}(1 + (gm_1 \cdot R_{LOAD}))]}$$

If there is a load capacitor attached to the load then a second higher frequency pole will be introduced:

$$f_{3dB} = \frac{G_{o\_LOAD}}{2\pi \cdot C_{LOAD}} \quad \text{If } G_{o\_LOAD} \text{ is active then}$$

$$f_{3dB} = \frac{I_D (\lambda_{M1} + \lambda_{M2})}{2\pi \cdot C_{LOAD}} \equiv \frac{1}{R_{LOAD} \cdot 2\pi \cdot C_{LOAD}}$$

The M1 device is a voltage controlled source and the small gate voltage ( $V_{gs}$ ) creates a large current ( $I_{ds}$ ) through the  $R_{LOAD}$  creating an output voltage ( $V_o$ ) much greater than the input ( $V_{gs}$ ) ie it has voltage gain. So if you could place a low impedance current buffer between M1 and the  $R_{LOAD}$  you could greatly reduce the Miller effect – and this is exactly what M2 biased into saturation does. The resistance looking into a source is pretty low:-

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{gs}}{g_{M1} V_{gs}} = \frac{1}{g_{M1}} = I_D \lambda_{M2}$$

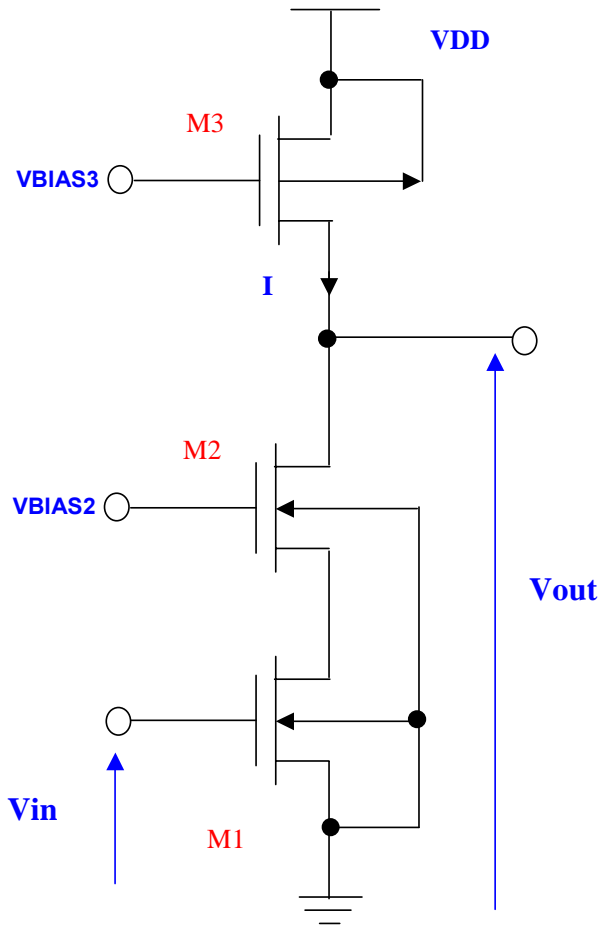
For a typical device @ 100uA,  $\lambda = 0.01$   $R_{IN} = 1E - 6\Omega$

A practical cascode amplifier is shown in Figure 2.

The device M2 acts as a low impedance current buffer, isolating the amplifying M1 with the load M3. Therefore, the gain of the cascode amplifier is approximately:-

$$A_v = \frac{gm_1}{go_3} \quad \text{strictly speaking } A_v = \frac{gm_1}{go_3 + go_1}$$

$$A_v = - \sqrt{\frac{2 \cdot K_{N1} \cdot W_1}{L_1 \cdot I_D \cdot \lambda_3}}$$



**Figure 2 Cascode amplifier with active load**

$$R_{OUT} \cong rds_3 = \frac{1}{I_D \lambda_3}$$

To be able to fully characterise the amplifier we need expressions in order to calculate output voltage swing and frequency response.

$$V_{OUTMAX} = VDD - VDS_{3SAT}$$

$$V_{OUTMIN} = \frac{\beta_{M3}}{2 \cdot \beta_{M2}} \left( VDD - VBIAS3 - |VT3| \right)^2 \left( \frac{1}{VBIAS2 - VT2} + \frac{1}{VDD - VT1} \right)$$

$$\text{Where } \beta = \frac{K \cdot W}{L}$$



### Example

Determine the gain, output resistance, gate bias voltages,  $V_{max}$  and  $V_{min}$  of the cascode amplifier of Figure 2. Assume  $W=L=1\mu m$ ,  $K_N=110\mu A/V^2$ ,  $K_P=50\mu A/V^2$ ,  $\lambda = 0.05$ ;  $V_T = 0.7V$ ,  $I_D=100\mu A$ .

The first step is to calculate the required bias voltages for each device.

First set the correct current to  $100\mu A$ , so we need to determine the correct  $v_{gs}$  to apply to the N-type FET.

$$V_{gs} = V_T + \sqrt{\frac{I_{REF}}{K_N}} = 0.7 + \sqrt{\frac{100E^{-6}}{110E^{-6}}} = 1.65V$$

$$V_{SAT} = V_{GS} - V_T = 1.65 - 0.7 = 0.95V$$

So we set the amplifying device M1 to  $v_{gs} = 1.65V$  and the second device to  $V_{gs} + V_{SAT} = 2.6V$ .

And set the correct  $V_{gs}$  to apply to the P-type FET active source.

$$V_{gs} = V_T + \sqrt{\frac{I_{REF}}{K_P}} = 0.7 + \sqrt{\frac{100E^{-6}}{50E^{-6}}} = 0.72V \text{ (apply } 5 - 0.7 = 4.3V \text{ to gate terminal)}$$

So we set the bias to M3 at  $4.3V$ .

### Calculation of gain

$$A_v = \frac{g_{m1}}{g_{o3}} \text{ strictly speaking } A_v = \frac{g_{m1}}{g_{o3} + g_{o1}}$$

$$A_v = -\sqrt{\frac{2 \cdot K_{N1} \cdot W_1}{L_1 \cdot I_D \cdot \lambda_3}} = -\sqrt{\frac{2 \cdot 110E^{-6} \cdot 1E^{-6}}{1E^{-6} \cdot 100E^{-6} \cdot 0.05}} = 6.63 = 16.5dB$$

### Output Resistance

$$R_{OUT} \cong r_{ds3} = \frac{1}{I_D \lambda_3} = \frac{1}{100E^{-6} \cdot 0.05} = 200K\Omega$$



**Output Voltage Swing**

$$V_{OUTMAX} = VDD - VDS_{3SAT}$$

$$VDS_{3SAT} = V_{GS3} - V_{T3} = 0.72 - 0.7 = 0.02V$$

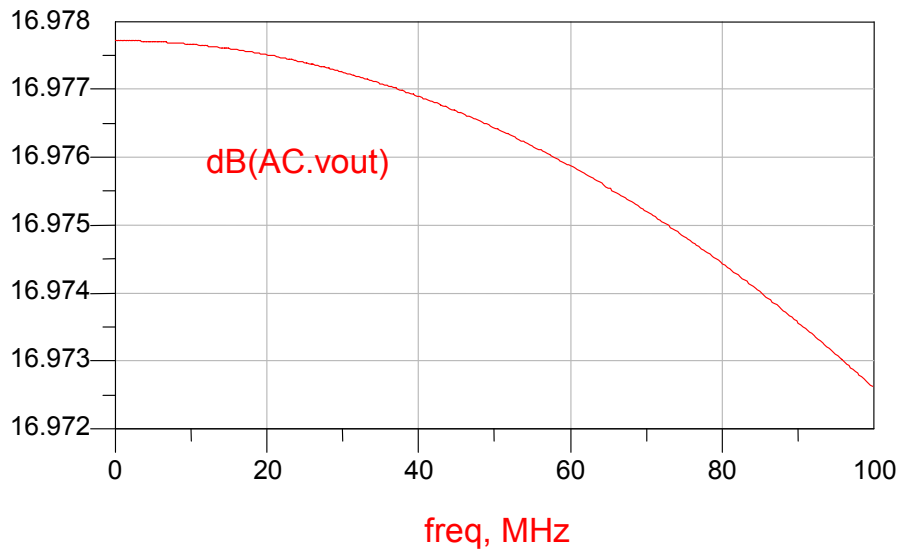
$$V_{OUTMAX} = 5 - 0.02 \cong 5V$$

$$V_{OUTMIN} = \frac{\beta_{M3}}{2 \cdot \beta_{M2}} (VDD - VBIAS3 - |VT3|)^2 \left( \frac{1}{VBIAS2 - VT2} + \frac{1}{VDD - VT1} \right)$$

Where  $\beta = \frac{K \cdot W}{L}$

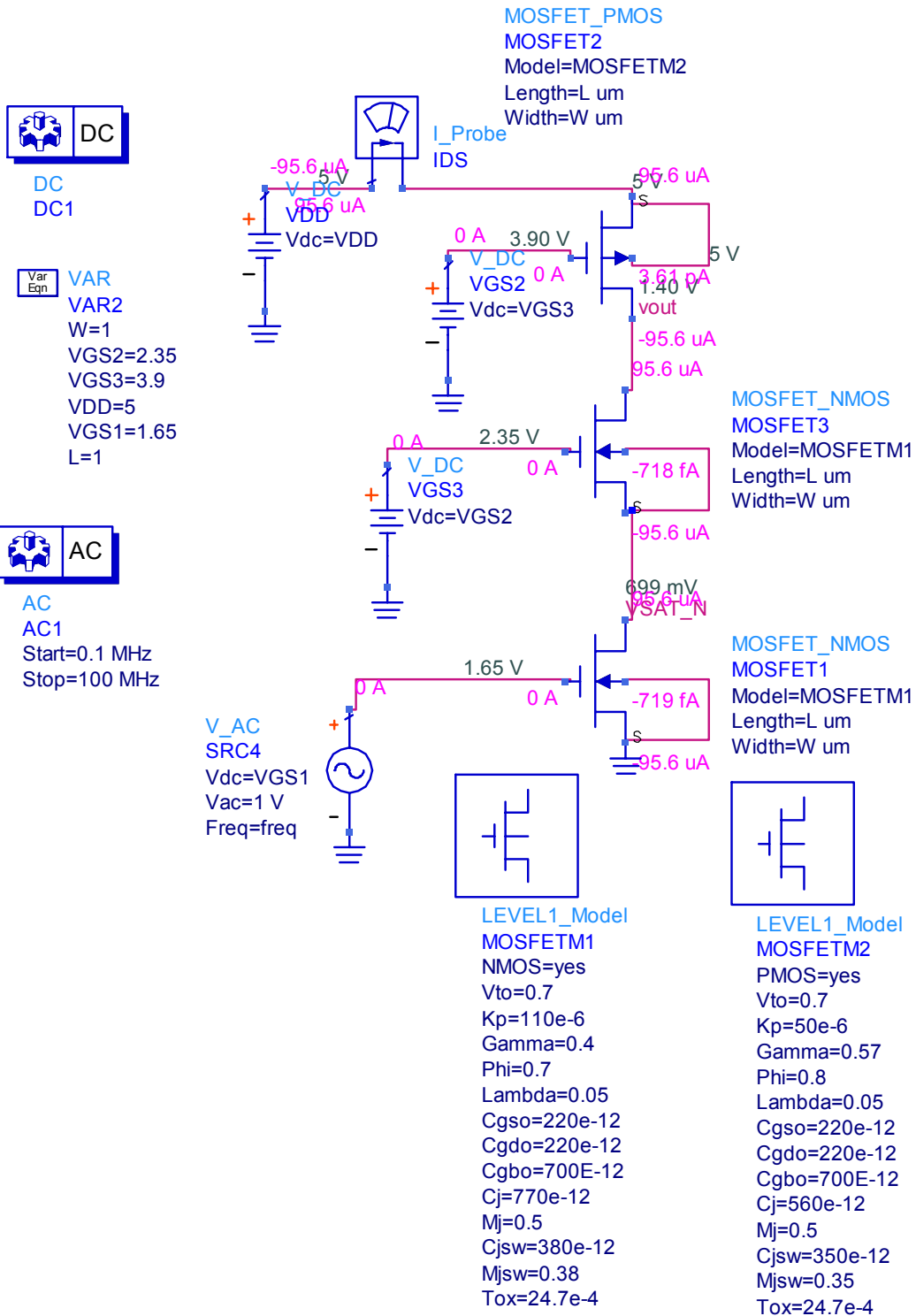
$$V_{OUTMIN} = \frac{\frac{50E^{-6} \cdot 1}{1}}{2 \cdot \frac{110E^{-6} \cdot 1}{1}} (5 - 3.9 - |0.7|)^2 \left( \frac{1}{2.35 - 0.7} + \frac{1}{5 - 0.7} \right) = 0.227 \cdot (0.61) \cdot (0.838) = 0.116V$$

The ADS simulation of the example cascode is shown in Figure 4. The gain plot as a result of the simulation is shown in Figure 3.



| DC.IDS.i | DC.VSAT_N | DC.vout |
|----------|-----------|---------|
| 95.59uA  | 699.3mV   | 1.397 V |

**Figure 3 Resulting Gain plot from the ADS simulation of the example Cascode Amplifier**



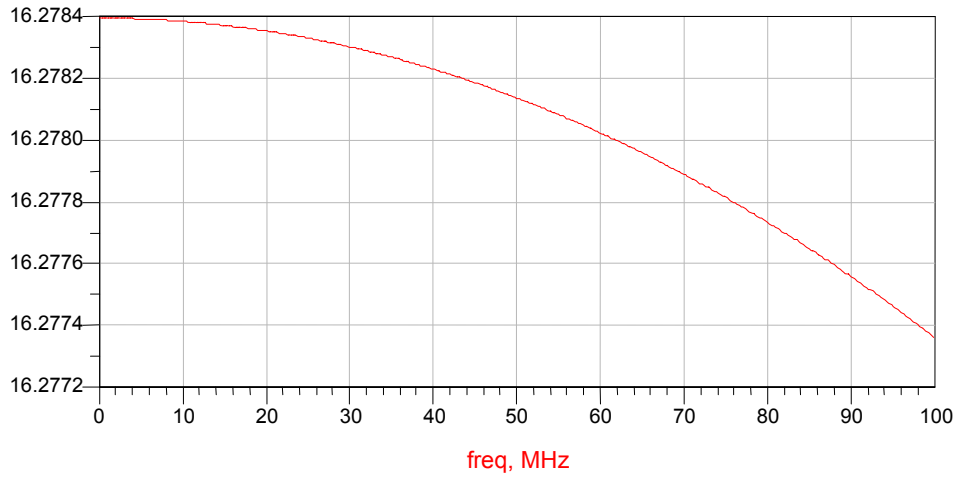
**Figure 4 ADS simulation setup for the example Cascode Amplifier**

A more practical circuit is shown in Figure 5. This circuit now includes the correct bias current mirrors and associated bias setting resistor. The left hand bias arm includes FETs configured as diodes such that the voltage across each source-drain is  $V_{SAT}+V_T$ . One advantage of doing





dB(AC.Vout)



| DC.IDS.i | DC.Vbias1 | DC.Vbias2 | DC.Vbias3 | DC.Vout | DC.VT_VSAT |
|----------|-----------|-----------|-----------|---------|------------|
| 99.97uA  | 1.624 V   | 3.518 V   | 3.631 V   | 3.631 V | 1.625 V    |

**Figure 6** Resulting plot from the simulation of the circuit shown in Figure 5. Note that VT+VSAT = 1.625V and closely agrees with the 1.65V calculated earlier.

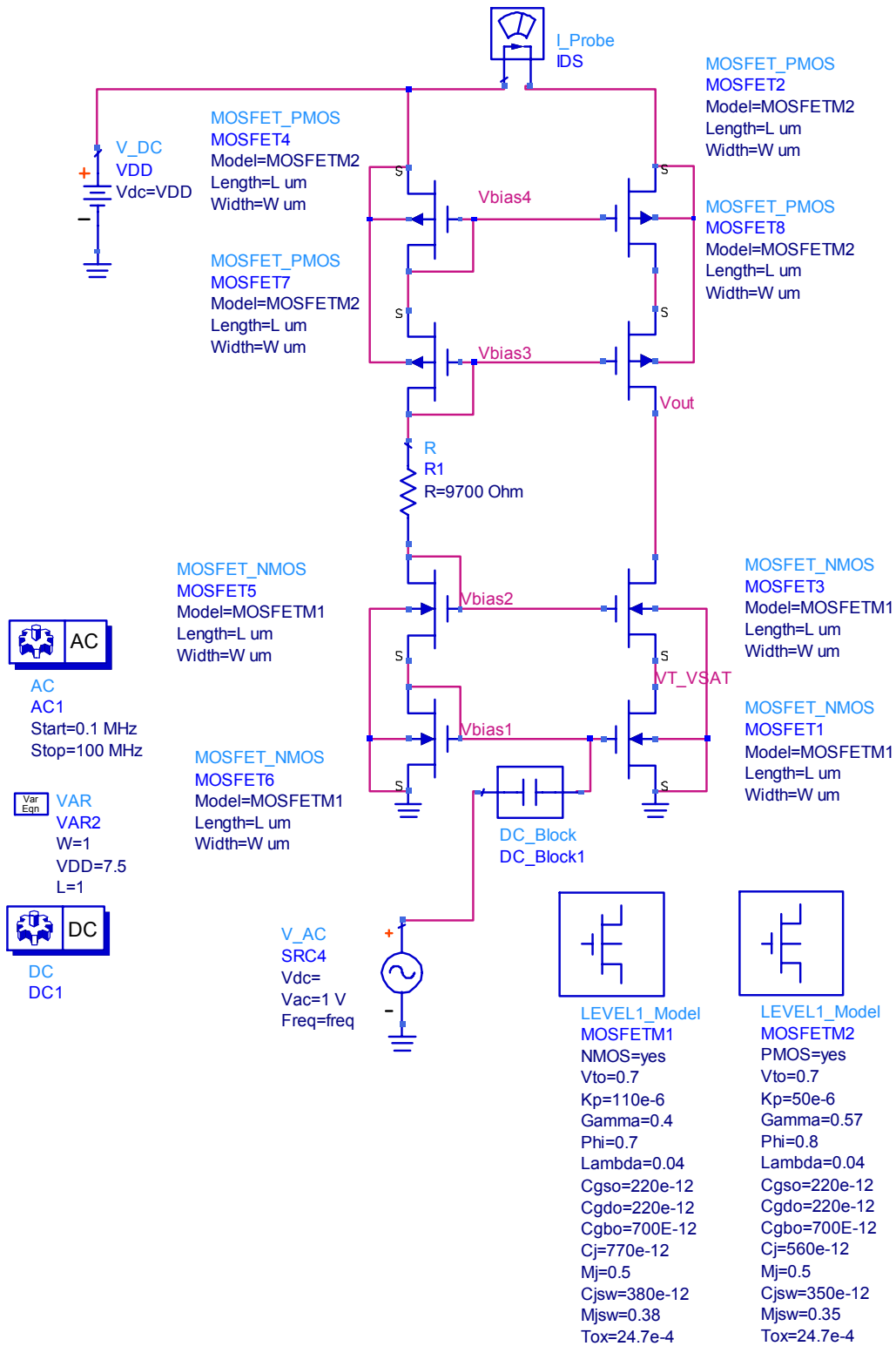
We can obtain more gain from the cascode by adding a further active load as shown in Figure 7. The gain of the stage will now be:-

$$A_v = \frac{g_{m1}}{g_{o3}} \text{ strictly speaking } A_v = \frac{g_{m1}}{g_{o3} + g_{o1}} \text{ If we cascode the load then}$$

$$A_v \approx \left( \frac{g_{m1}}{g_{o3}} \right)^2 \text{ As } A_v = - \sqrt{\frac{2 \cdot K_{N1} \cdot W_1}{L_1 \cdot I_D \cdot \lambda_3}} \text{ Then the new gain} = - \left( \frac{2 \cdot K_{N1} \cdot W_1}{L_1 \cdot I_D \cdot \lambda_3} \right)$$

$$A_v \approx - \frac{2 \cdot K_{N1} \cdot W_1}{L_1 \cdot I_D \cdot \lambda_3} = - \frac{2.110E^{-6} \cdot 1E^{-6}}{1E^{-6} \cdot 100E^{-6} \cdot 0.05} = 44 = 32\text{dB}$$

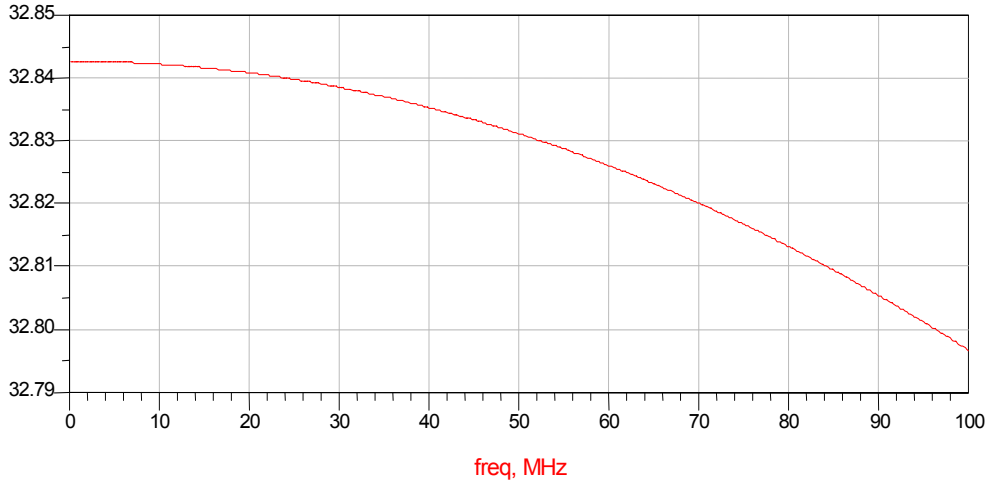




**Figure 7** Addition of another active load to increase the gain of the cascode amplifier. Note however that the additional  $V_T+V_{SAT}$  has meant that to include the bias resistor the supply has been increased to 7.5V.



dB(AC.Vout)



| DC.IDS.i | DC.Vbias1 | DC.Vbias2 | DC.Vbias3 | DC.Vout | DC.VT_VSAT |
|----------|-----------|-----------|-----------|---------|------------|
| 101.1uA  | 1.628 V   | 3.528 V   | 4.508 V   | 4.498 V | 1.642 V    |

**Figure 8 Increased gain cascode of Figure 7, the gain of 32dB agrees with the calculation performed earlier ie  $AV \sim (gm.Ro)^2$ .**

Note one of the problems using cascode stages in that for each device we use the voltage drop across each device will be  $V_T + V_{SAT}$ . This equates to approximately 1.65V per device and with 4 devices this will cause a total voltage drop of 6.6V so we can't use our 5V rail !!! In the example the voltage supply has been increased to 7.5V to allow for the additional device.

This problem of increased voltage rail can be improved by using the folded cascode configuration, where the cascode is split between the active amp and active load and linked by another current load.

**Also we can greatly reduce  $V_{SAT}$  by increasing the W/L ratio.**

The folded cascode is very popular in the design of low voltage Op-Amps and is subject to another tutorial.