5

Discrete Linear Power Amplifier

Introduction

In Chapter 4 you saw power integrated circuits that could deliver up to 56 W to a load. Protection of the load and the IC were provided automatically.

To deliver more power you have to build the amplifier from a collection of resistors, capacitors, diodes, transistors, and op amps. Though more involved, this allows you to better match the circuit to its requirements. You can build amplifiers capable of driving several hundred watts of power, provide current limiting and thermal protection, and match performance to a resistive or a reactive load.

During this chapter you will use the central elements of each of the previous chapters. Op amps will be combined with transistors and a suspended supply amplifier in a composite configuration. All of the power calculations you used with power ICs are directly applicable to the power transistors in this chapter. Heat sinking is as important to these discrete transistors as it is to power ICs. Therefore, you have already mastered many of the details. In this chapter you will learn to apply these procedures to arrays of discrete transistors and their supporting electronics.

Objectives

By the end of this chapter, you will be able to:

- Describe the performance of an enhancement mode MOSFET and interpret its data sheet to determine key parameters.
- Explain the problems of a class A MOSFET power amplifier.
- Analyze and design a class B MOSFET power amplifier with an op amp driver and a suspended supply amplifier intermediate stage. In an analysis, determine all currents, voltages, and power. For a design, select all component values, all power ratings, and heat sinks.
- Properly parallel MOSFETs operated in their linear region.
- Analyze and design required current limiting and a transistor case temperature sensing circuit.
- Determine the effect on the amplifier of a load with both resistive and reactive elements.

5.1 The Enhancement Mode MOSFET

N-Channel

A simplified physical layout of an *n*-channel enhancement mode metal oxide semiconductor field effect transistor (MOSFET) is shown in Figure 5-1. There are three connections. The **source**, at the bottom, is made of ***n*-type** material and has an abundance of free electrons. The **drain**, at the top, is also made of *n* material, with lots of free electrons. But between these two islands is a **channel** made of ***p*** material. This area has no free electrons. In fact, there are many **holes** in the crystal structure. Each hole is a missing electron bond. So any electron that might stray into the channel from the source or drain falls into a hole, and becomes fixed in the crystal structure. It disappears from the horde of electrons free to respond to external voltages and produce conduction. All of this is to remind you that the *p* material forms an open between the *n*-type source and drain. Even with an external voltage between the drain and the source, there is no current flow.

Figure 5-1 Basic MOSFET structure

The third terminal is the **gate**. It is separated from the rest of the transistor by a layer of silicon dioxide. This is an insulator, preventing current flow into or out of the gate.

With zero volts applied between the gate and the source terminals, there is still a barrier of *p*-type material between the *n* material of the source and the *n* material of the drain. So there are no free electrons in this channel and no current can flow between the source and the drain. The transistor is off.

Applying a positive voltage to the gate with respect to the source attracts electrons into the channel near the gate. As the gate-to-source voltage is made more positive, more electrons are attracted into the channel, and the holes of the *p* material are filled. Eventually, there are enough free electrons near the gate to form a complete channel of *n* type material between the source and the drain. Conduction can now take place in response to the voltage supply connected between the drain and the source terminals. This is shown in Figure 5-2.

The gate-to-source voltage needed to **enhance** the channel enough to allow 250 μA of drain (and source) current is called the **threshold voltage**.

$$V_{\text{th}} = V_{\text{GS}}\Big|_{I_{\text{D}}=250\mu\text{A}}$$

Figure 5-2 MOSFET biased on

This parameter is a specification of the transistor. Before the transistor can begin to respond to the input (gate-to-source) voltage, you must apply this much dc voltage, just to turn the transistor on. Figure 5-3 is a part of the data sheet for the IRF630.

IRF530N

International
IOR Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.11	Ω	V_{GS} = 10V, I_D = 9.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	6.4	—	—	S	V_{DS} = 50V, I_D = 9.0A

Figure 5-3 Threshold voltage specification for the IRF630 (*courtesy of International Rectifier*)

The manufacturer indicates that no IRF630 begins to conduct with less than 2 V applied between the gate and the source. At some level between 2 V and 4 V the threshold is reached and drain current flows. The precise threshold varies from one IRF630 to another. But you can be assured that every IRF630 conducts at least 250 μA when V_{GS} = 4 V. You will see how to handle this wide variation when building an amplifier later.

As the gate-to-source voltage is increased beyond the threshold, the *n*-type channel grows both deeper and wider. This increases the cross-sectional *area* of the channel. As a consequence, once the threshold voltage has been reached, the drain (and source) current is proportional to the *square* of the gate-to-source voltage. It takes very little increase in gate-to-source voltage to have a significant effect on the drain current.

Example 5-1

Use simulation software to determine the relationship of I_D to V_{GS} for an IRF530 (very similar to the IRF630) with V_{DS} = 56 V_{dc}. Plot the resulting data.

Solution

The Multisim schematic at V_{GS} = 4.0 V is shown in Figure 5-4, along with the plot of I_D versus V_{GS}. V_{th} = 3.6 V. A few tenths of a volt change beyond 3.6 V causes a major increase in I_D.

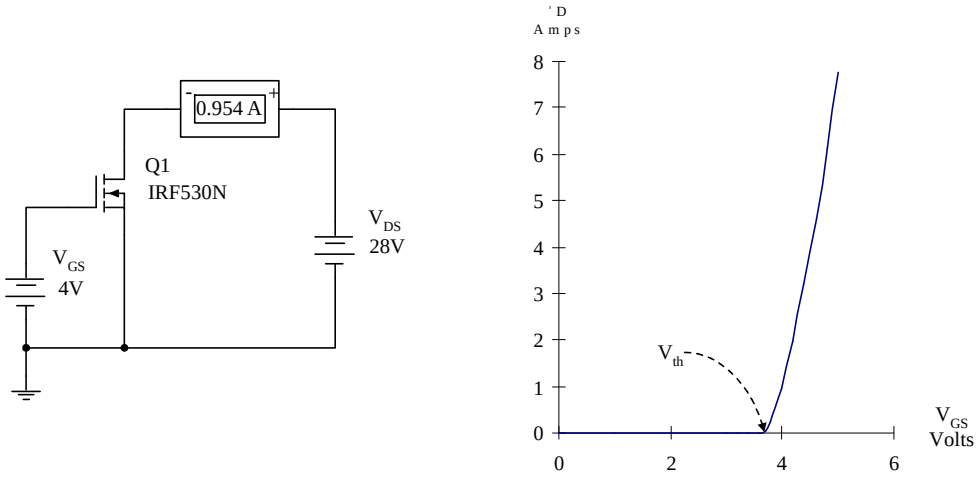

Figure 5-4 Simulation of the IRF530 gate control of drain current

Practice: What effect does changing the drain voltage have?

Answer: It has practically no effect. Once V_{DS} is over 4 V, drain current is relatively independent of drain-to-source voltage.

The manufacture's plot of V_{GS} versus I_D for the IRF630 is given in Figure 5-5. There are several points to notice. First, the shape does not seem to match the shape of the graph from the simulation, shown in Figure 5-4. However, the vertical axis for the specifications in Figure 5-5 is logarithmic, while Figure 5-4 was produced with a linear scale. Secondly, the manufacturer assumes a threshold voltage of 4 V. But you already have seen that this may be as low as 2 V. So, you must offset the horizontal axis, shifting it right or left, to make it apply to your particular MOSFET.

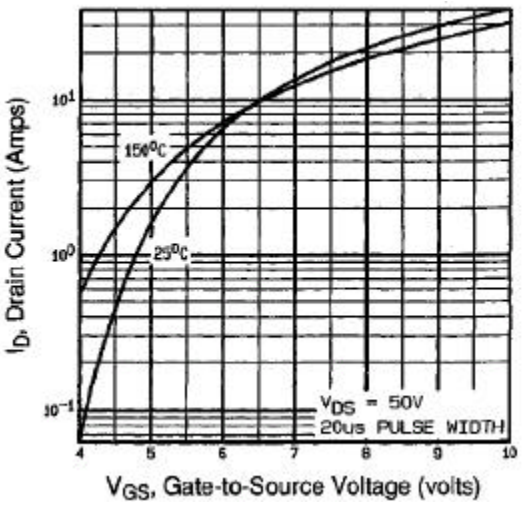

Figure 5-5 Gate control plot of an IRF630 (*courtesy of International Rectifier*)

Example 5-2

Determine the drain current for an IRF630 with V_{GS} = 5.0 V at 25°C.

Solution

$10^0 = 1$. The V_{GS} = 5.0 V vertical grid intersects the 25°C curve at about I_D = 1.7 A, assuming that V_{th} = 4 V. For a transistor with a lower threshold, the drain current is much larger.

Practice: What happens to the drain current when the temperature rises to 150°C?

Answer: The drain current *increases* to 3 A, as the temperature rises.

From Example 5-2, as temperature rises, the drain current increases, dissipating more power, heating up the transistor more, producing more current, heating up the transistor more, and so on, and so on. In *linear* applications, MOSFET transistors can thermally run away, and burn themselves up. So it is critical that you properly manage the power dissipation, temperatures and heat sinks when building linear amplifiers using MOSFETs.

The transistor discussed so far is an *n-channel enhancement mode* MOSFET. The source and drain are made from *n*-type material. With no gate bias voltage, there is no channel. To establish drain current, the gate bias voltage must be made positive enough to *enhance* the channel. So, on the schematic symbol, the channel is shown as a broken line. The arrow points toward the channel, since semiconductor arrows point toward the *n*-type material.

Once the channel is established, n type current carriers (electrons) move from the source to the drain in response to an external positive V_{DS}. Since the electrons are negatively charged, moving from source to drain, *conventional* current moves from the positive terminal of V_{DS}, into the drain of the MOSFET, to the source of the MOSFET, and then to analog common, and back to the negative terminal of the V_{DS} supply. There is a layer of insulating glass between the gate terminal and the channel, so there is no gate current. This is shown in Figure 5-6.

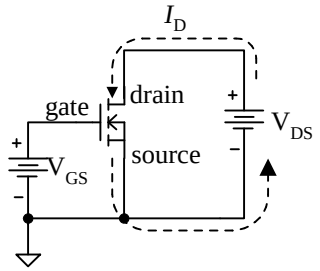

Figure 5-6 Basic *n*-channel enhancement mode schematic

P-Channel

A *p*-channel enhancement mode MOSFET is shown in Figure 5-7. The substrate is *n*-type material, and the source and drain are made from *p* material. The current carriers are the holes in the crystal structure (vacancies that *should* contain an electron). Since holes are the absence of an electron, they act as if they were positive particles. The channel is established (enhanced) by making V_{GS} *negative* enough to repel the free electrons of the *n*-type substrate, and force electrons from their bonds within the crystal structure, leaving holes behind. This changes the region near the gate into *p* material. Once there is a channel from source

Figure 5-7 *P*-channel MOSFET

to drain, holes can flow from the source to the drain in response to the negative V_{DS}.

Holes act as if they are positive charges. They move in the same direction as conventional current. The schematic for a *p*-channel enhancement mode MOSFET with circuit current is shown in Figure 5-8.

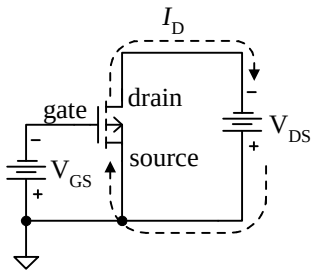

Figure 5-8 Basic *p*-channel enhancement mode schematic

The *p*-channel and the *n*-channel enhancement mode MOSFETs are complementary. Table 5-1 compares their characteristics. In linear applications, *n*-channel MOSFETs are used to handle the positive part of a signal, and *p*-channel devices process the negative voltages.

Table 5-1 *N* and *p*-type MOSFET comparison

characteristic	*n*-channel	*p*-channel
carriers	electrons	holes
bias voltage	positive	negative
I_D	into drain	out of drain

Example 5-3

The IRF9630 is the *p*-channel complement to the IRF630. From its specifications find V_{th} and I_D at $V_{GS} = -5V$.

Solution

$V_{th} = -2$ V to -4 V $\qquad I_{D \text{ at VGS} = -5V} = 2.3$ A

5.2 Class A Common Drain Amplifier

A **class A amplifier** conducts during the entire cycle of the input signal. This amplifier most faithfully reproduces the input signal at the output. It produces the lowest distortion. Figure 5-9 is a class A amplifier built with an *n*-channel enhancement mode MOSFET. It is called a common drain amplifier because the drain is connected to the dc supply voltage. But a dc supply is a short to ac signals. So the drain is connected to ac common.

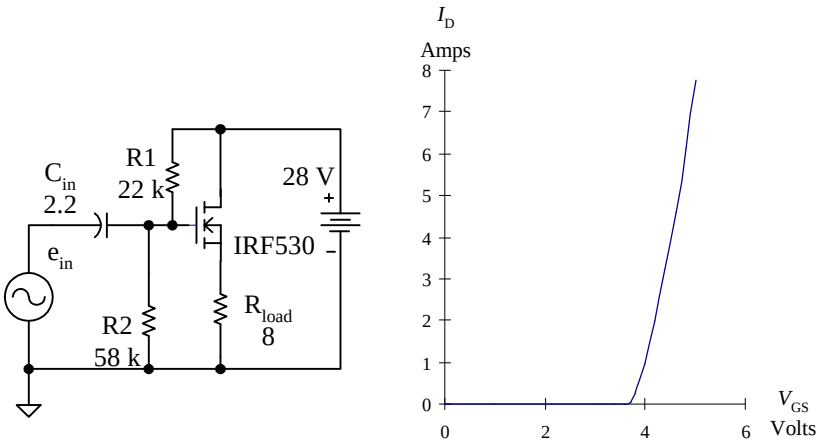

Figure 5-9 Class A common drain amplifier

Bias

The 8 Ω load is connected between the source and circuit common, since power loads are normally tied to common. Resistors R1 and R2 form a voltage divider to set the dc voltage on the gate. They assure that the amplifier is biased well beyond V_{th}, so that the transistor conducts during the entire cycle of the input signal, e_{in}. That is how class A is defined. Capacitor C_{in} blocks the dc bias voltage at the gate from the signal generator, but is sized to pass the lowest signal the amplifier must process.

With a 56 V supply, it is reasonable to set the dc voltage at the source to about 28 V_{dc}. This allows the ac signal to drive the voltage up

toward 56 V and down toward common, giving a wide signal swing. An 8 Ω load dropping 28 V_{dc} must pass 3.5 A_{dc}. According to the transistor's V_{GS} versus I_D graph, 3.5 A_{dc} is produced by $V_{GS} \cong 4.4\ V_{dc}$. With 28 V_{dc} on the source and 4.4 V_{dc} between the gate and the source,

$$V_G = V_S + V_{GS} = 3.5\,A_{dc} \times 8\,\Omega + 4.4\,V_{dc}$$

$$V_G = 32\,V_{dc}$$

The voltage divider, R1 and R2 set V_G to

$$V_G = \frac{30\,k\Omega}{22\,k\Omega + 30\,k\Omega} 56\,V_{dc} = 32.3\,V_{dc}$$

So the amplifier in Figure 5-9 is biased in the middle of its supply range, with 3.5 A_{dc} of bias current constantly running through it. This is necessary to assure class A operation.

AC Operation

The ac performance of this amplifier requires a model and a little math. The ac signal causes the gate-to-source voltage to *change*. This change in gate-to-source voltage causes the drain current to *change*. The key ac parameter tells how much the drain current changes in response to changes in gate-to-source voltage. It is called the amplifier's **forward transconductance**.

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS}\ \text{constant}}$$

It is actually the slope of the I_D versus V_{GS} graph, at the bias point (3.5 A_{dc} in Figure 5-9). The manufacturer specifies that for the IRF530,

$$g_{fs\ IRF530} > 6.4\frac{A}{V}$$

So, the ac signal does not need to change the gate-to-source voltage very much to have a major effect on the current through the transistor, and through the load.

The ac model for the class A amplifier is shown in Figure 5-10. The capacitor and the dc voltage supply have been replaced with shorts. Resistors R1 and R2 are in parallel for the ac signal, so they have been replaced with a single resistor. The MOSFET is modeled as a voltage controlled current source. The gate is open. Between the drain and the

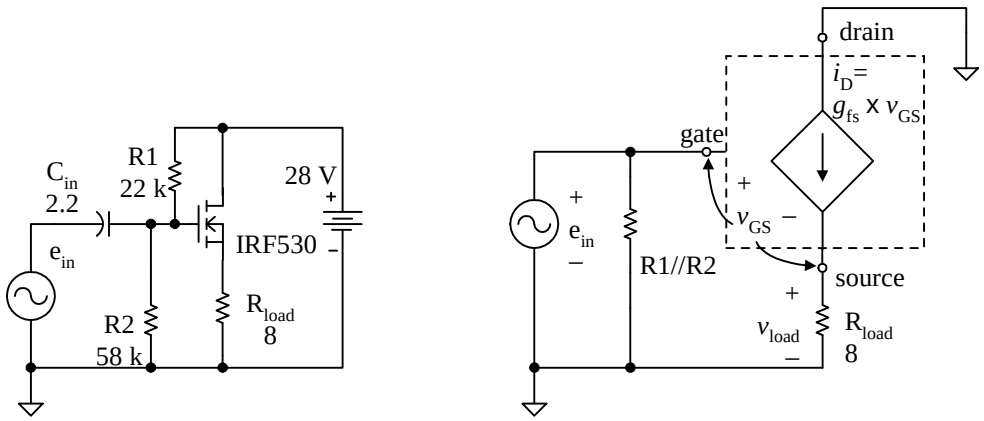

Figure 5-10 AC model of the class A MOSFET amplifier

source is a dependent current source. Its value is determined by the gate-to-source voltage and the transistor's forward transconductance.

To determine the load's ac voltage, apply Kirchoff's voltage law, by summing the loop from e_{in}, v_{GS}, and v_{load}.

$$e_{in} - v_{GS} - v_{load} = 0$$

$$e_{in} - v_{GS} - i_D R_{load} = 0$$

But, i_D is set by v_{GS}. $$e_{in} - v_{GS} - (g_{fs} v_{GS}) R_{load} = 0$$

Collecting terms and rearranging gives

$$e_{in} = v_{GS}(1 + g_{fs} R_{load})$$

Or $$v_{GS} = \frac{e_{in}}{1 + g_{fs} R_{load}}$$

Amplifier output voltage

The load voltage is $$v_{load} = i_D R_{load} = g_{fs} v_{GS} R_{load}$$

Substitute for v_{GS}. $$v_{load} = \frac{g_{fs} R_{load}}{1 + g_{fs} R_{load}} e_{in}$$

$A_v < 1$

Since the denominator is always 1 more than the numerator, the load voltage is always a little less than the input signal. For this amplifier, $A_v = 0.98$, but it can output several amps of current to the 8 Ω load.

Example 5-4

Verify the dc and the ac performance of the class A, common drain amplifier of Figure 5-9 with e_{in} = 20 V_p.

Solution

The Multisim simulation is shown in Figure 5-11.

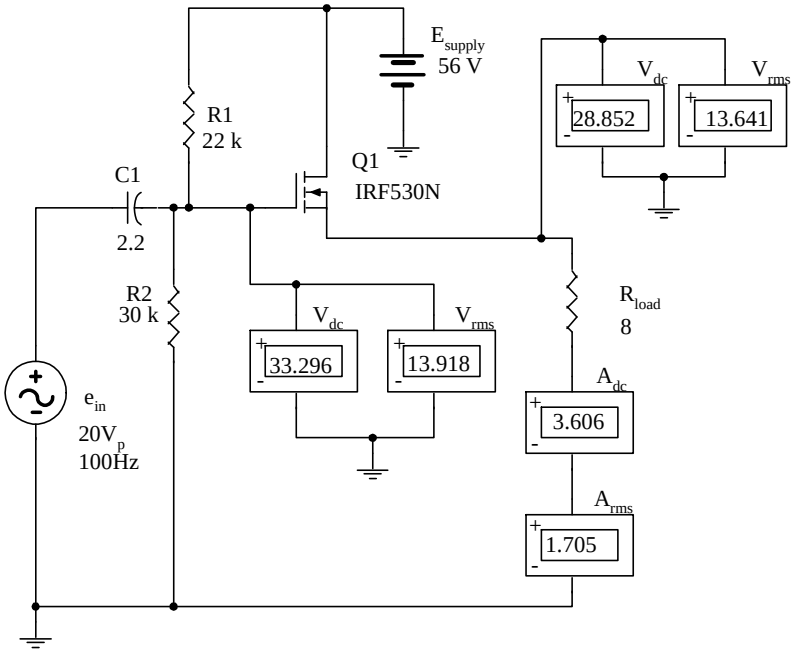

Figure 5-11 Simulation results for Example 5-4

Practice: Using the oscilloscope function, determine how large the output can be before it begins to distort. Explain the distortion.

Answer: The output may go to 28 V_p before it distorts. The distortion is caused by the output running into analog common.

Class A amplifiers may produce very little distortion, when properly biased and not overdriven. However, there are several major problems. In the schematics you have seen so far, the load is connected directly to

the source terminal of the transistor. The *bias* current of 3.5 A_{dc} flows continuously through the load, even when no signal is applied. It is necessary to put that much bias current through the transistor and the load to be sure that when the input signal goes negative, the transistor continues to output a smaller signal. It does *not* cut off, outputting zero. Just because of this bias

$$P_{supply} = 56\ V_{dc} \times 3.5\ A_{dc} = 196\ W$$

The load must dissipate

$$P_{load} = (3.5\ A_{dc})^2 \times 8\,\Omega = 98\,W$$

If the load is an 8 Ω loudspeaker, this dc current causes the cone to deflect once. It does *not* vibrate back and forth as it does with an ac signal. The coil is *not* cooled, and the loudspeaker burns out, without ever making a sound. Even if the load is not a loudspeaker, it still must dissipate the 98 W even before an ac signal is applied.

The transistor must dissipate the power provided by the supply but not dissipated by the load.

$$P_Q = 196\,W - 98\,W = 98\,W$$

This power is wasted. It is not produced by the signal. It is there because the transistor must be biased into the middle of its conduction region.

Class A power amplification is extremely wasteful. It is rarely used. But only a few modifications produce the much more efficient class B amplifier.

5.3 Class B Push-Pull Amplifier

In a **class B** amplifier the transistor is biased *off*, but just on the edge of conduction. That means

$$V_{GS} = V_{th}$$

When the input is 0 V, the transistor is off, and that 98 W wasted by the class A amplifier in the examples of the previous section is not used at all.

The Push Amplifier

The class B amplifier is laid out just a little differently from the class A of the previous section. Look at Figure 5-12. There is no input capacitor. The input signal generator drives the lower end of resistor R2. The value of R2 must be changed to shift the bias from the middle of the linear region down to the threshold voltage.

Example 5-5

For the circuit in Figure 5-12:

1. Calculate R2's value to establish class B operation.
2. Verify that the transistor is biased at $I_D = 0\ A_{dc}$.
3. Determine v_{load}*'s* shape and amplitude with $e_{in} = 40\ V_p$.
4. Determine P_{load}, P_{supply}, and P_Q for $e_{in} = 40\ V_p$.

Figure 5-12 The push side of a class B push pull amplifier

Solution

1. Assuming that the transistor has the same characteristics as seen in the previous sections, with e_{in} replaced with a dc common,

$$V_{GS} = V_{th} = 3.6\,V_{dc}$$

This means that the voltage across R1 is

$$V_{R1} = 56\,V_{dc} - 3.6\,V_{dc} = 52.4\,V_{dc}$$

So, the current through R1 and R2 is

$$I_{R1\&R2} = \frac{52.4\,V_{dc}}{22\,k\Omega} = 2.38\,mA_{dc}$$

For this current to produce 3.6 V_{dc} when flowing through R2,

$$R2 = \frac{3.6\,V_{dc}}{2.38\,mA_{dc}} = 1.5\,k\Omega$$

2. The bias simulation is shown in Figure 5-13. It indicates 3.57 V_{dc} at the gate. This causes 56 μA_{dc} of drain current. With no input signal, the transistor is off, dissipating no power.

3. The two resistors form a voltage divider, dropping the voltage as it travels from the generator to the gate.

$$v_G = \frac{22\,k\Omega}{22\,k\Omega + 1.5\,k\Omega}40\,V_p = 37.5\,V_p$$

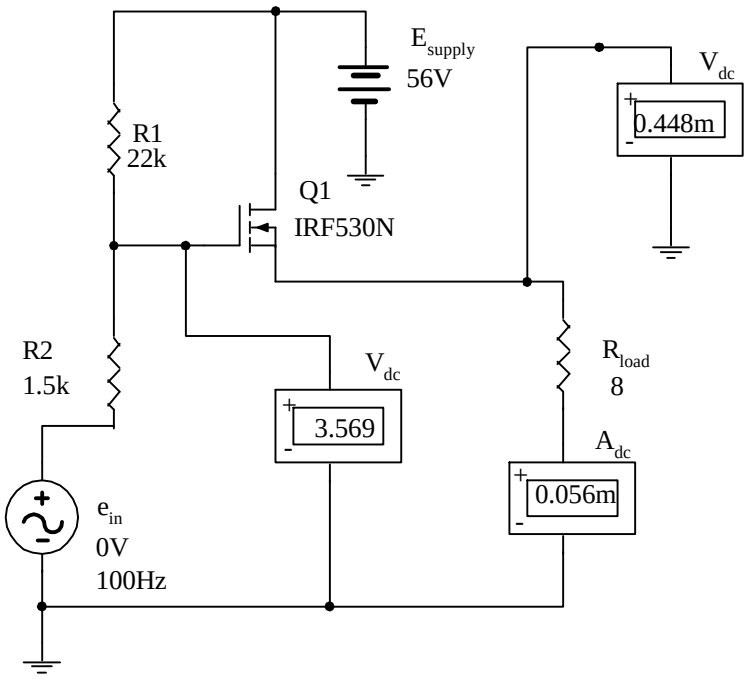

Figure 5-13 Multisim bias simulation results for Example 5-5

You have just seen that the gain for this amplifier is 0.98.

$$v_{load} = 0.98 \times 37.5\,V_p = 36.7\,V_p$$

The probe result from an OrCAD simulation is shown in Figure 5-14. The positive half of the input passes to the load at 36.5 V_p.

4. The voltage wave shape across the load is a half-sine. Through the resistance of the load, this produces a half-sine current.

$$I_{load} = \frac{36.5\,V_p}{8\Omega} = 4.6\,A_p$$

From Table 3-2, the power dissipated by a half-sine voltage and half-sine current is

$$P_{load} = \frac{V_p I_p}{4}$$

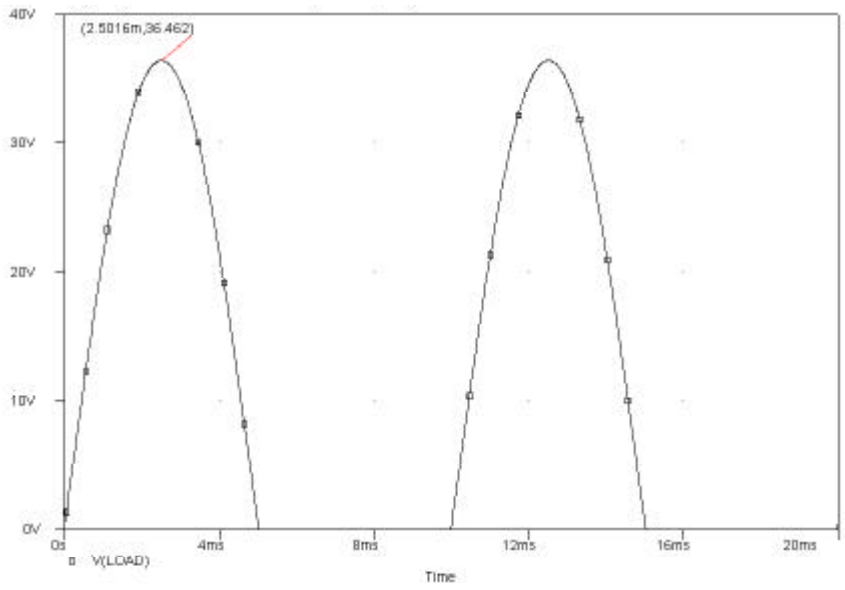

Figure 5-14 OrCAD probe voltage results for Example 5-5

$$P_{\text{load}} = \frac{36.5\,\text{V}_\text{p} \times 4.6\,\text{A}_\text{p}}{4} = 41.6\,\text{W}$$

The power supply provides a constant 56 V_{dc}, but the current is the half-sine delivered to the load. Again, from Table 3-2

$$P_{\text{supply}} = V_{\text{dc}} \frac{I_\text{p}}{\text{p}}$$

$$P_{\text{supply}} = 56\,\text{V}_{\text{dc}} \frac{4.6\,\text{A}_\text{p}}{\pi} = 82\,\text{W}$$

The transistor must dissipate the power that is provided by the power supply, but not delivered to the load.

$$P_\text{Q} = P_{\text{supply}} - P_{\text{load}}$$

$$P_Q = 82\,\text{W} - 41.6\,\text{W} = 40.4\,\text{W}$$

Using OrCAD's probe, each of these powers can be calculated.

P_Q = AVG((VD(M1)-VS(M1))*ID(M1))

P_{supply} = AVG(V(Esupply:+)*I(Esupply))

P_{load} = AVG(-V(load)*I(Rload))

The results of the OrCAD simulation and probe calculations are shown in Figure 5-15.

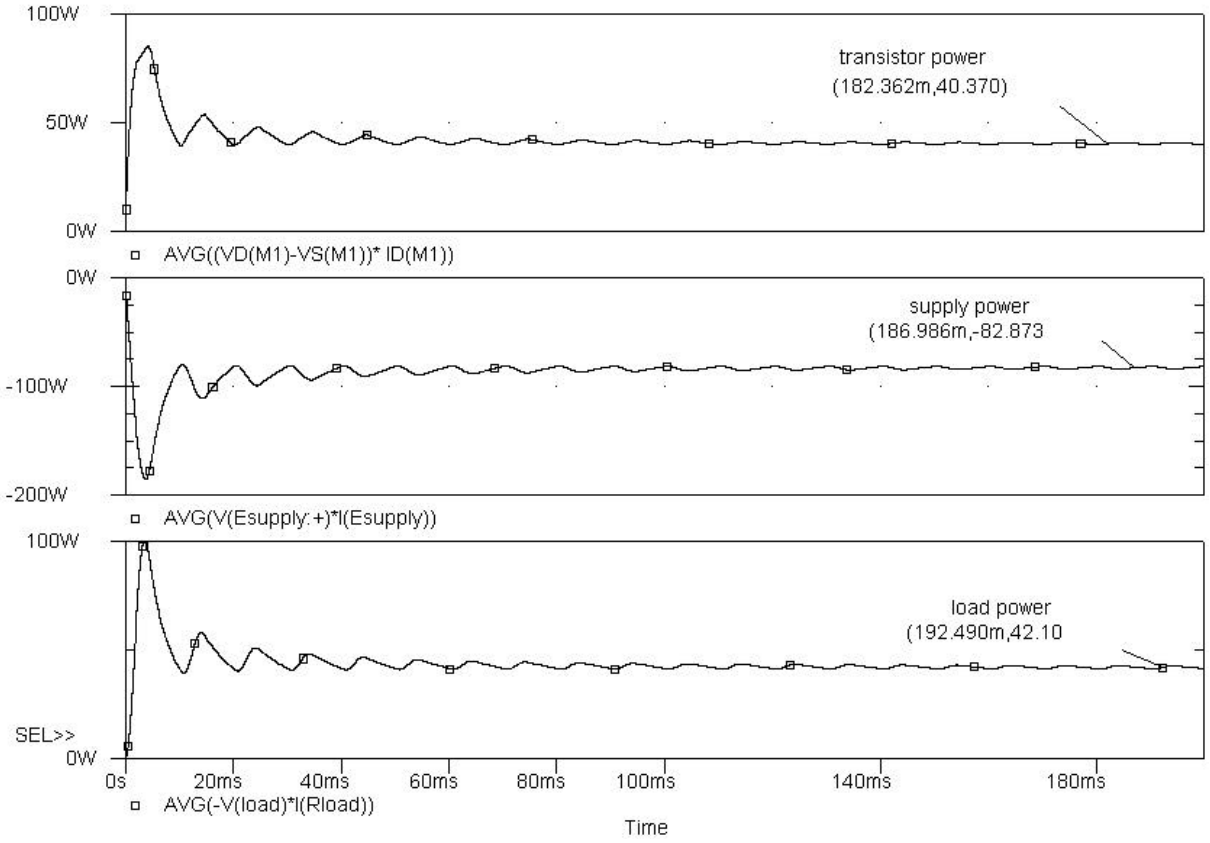

Figure 5-15 OrCAD probe power displays for Example 5-5

The Pull Amplifier

With the *n*-channel, push side of the class B amplifier, you are able to deliver the positive side of the signal to the load with only a small drop in voltage and at close to 4 A. No power has been wasted on biasing the transistor. For the class A amplifier, half of the power was squandered just setting the amplifier up. Manual calculations of bias and power for the positive side (**push**) of the class B amplifier agree well with those from simulation.

But the entire negative half of the signal is missing, because as soon as the input goes negative, the gate voltage falls below the transistor's threshold voltage. The *n*-channel transistor turns off.

A separate (**pull**) stage is needed to process the negative side of the input. The *n*-channel MOSFET is biased on with a positive signal and off when the signal goes negative. The *p*-channel enhancement mode MOSFET handles the negative side, turning on for negative signals, and off when the input goes positive. The *p*-channel pull side of the amplifier and its output wave form are shown in Figure 5-16.

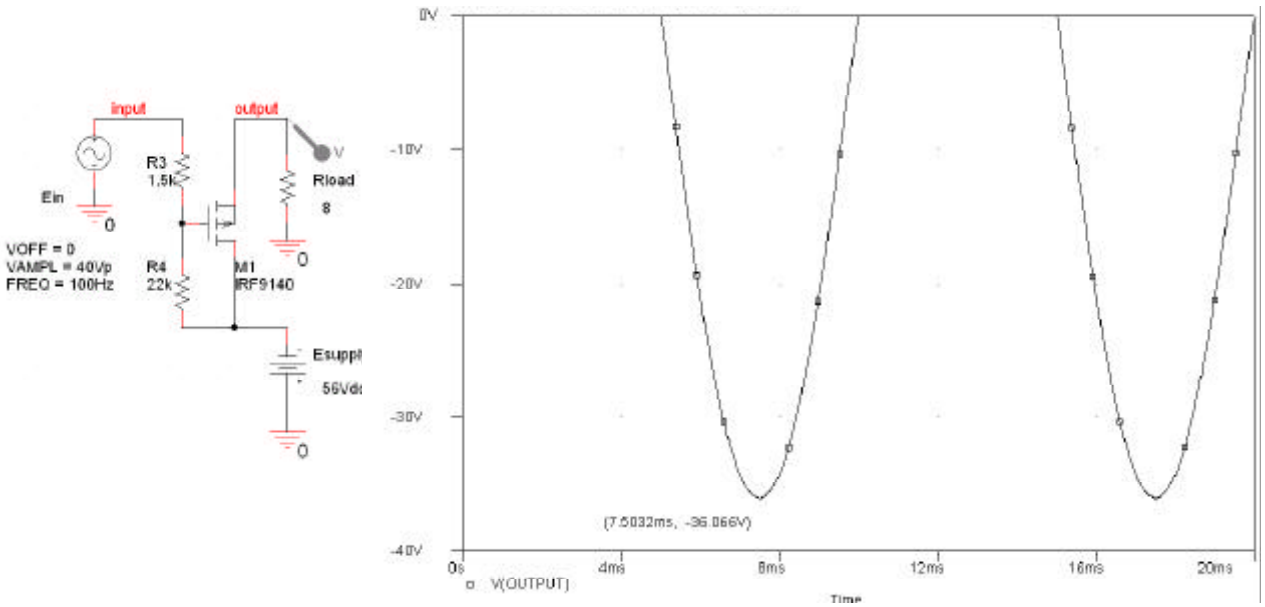

Figure 5-16 *P*-channel pull amplifier and OrCAD probe output wave form

The Push-Pull Amplifier

The combined push-pull (*n*-channel and *p*-channel) amplifier is shown in Figure 5-17. The performance and all of the calculations are just as you saw in Example 5-5. Each transistor is biased to the *edge* of conduction. But neither is on, so no dc current flows through the load, and it does not have to dissipate power just for the transistors to be properly biased.

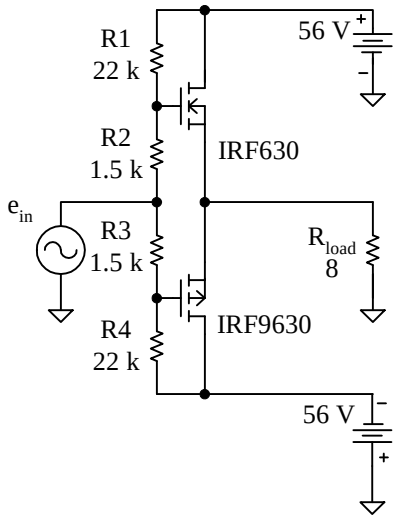

Figure 5-17 Class B push-pull amplifier schematic

From Example 5-5 you saw that when the input goes to positive 40 V_p, the *n*-channel transistor turns *on*, delivering 42 W to the load, and requiring that the transistor dissipate 40 W. The positive power supply must provide 82 W. During that time, the *p*-channel transistor is off, cooling. The negative power supply provides no significant power during this part of the cycle. It too can cool down.

During the negative cycle, the input goes to −40 V_p. As soon as the input drops below common, the *n*-channel transistor's gate is pulled below +3.6 V. That transistor goes off. The negative input now drives the *p*-channel transistor on, outputting as much as −36.5 V_p. This half-cycle

also delivers 42 W to the 8 Ω load. The negative supply provides 82 W and the *p*-channel transistor must also dissipate 40 W.

The two half signals combine at the load, producing a full sine wave, at 36.5 V_p, 73 V_{pp}, 25.8 V_{rms}, and 84 W. Each supply delivers 82 W, for a total power from the power supplies of 164 W. *Each* transistor must dissipate 40 W. You have seen all of these calculations in Example 5-5.

The *n*-channel transistor has been changed from the IRF530 to the IRF630. In the push-pull amplifier of Figure 5-17, the *p*-channel may drive the load (and therefore the source of the *n*-channel transistor) to almost –56 V. With +56 V on its drain, the *n*-channel transistor must have a rated maximum V_{DS} of over 112 V. The IRF630 (*n*-channel) /IRF9630 (*p*-channel) transistors each have a maximum drain voltage of 200 V.

The class A amplifier is so inefficient that it is impractical for use in delivering more than a few watts to a load. The class B amplifier solves this problem, allowing you to build a linear amplifier capable of providing hundreds of watts to the load. Even so, the simple class B amplifier of Figure 5-17 has several problems.

The input signal is divided by R1 and R2 or R3 and R4 before it is passed to the transistors. The voltage gain of the common drain amplifier is less than 1.

Changes in drain current (the ac drain current) depend on the *square* of the change in gate-to-source voltage. The load voltage is created by this change in drain current flowing through the load resistance. There is a *nonlinear* relationship between the input (gate) voltage and the load voltage. The output is distorted. The larger the signal, the worse the distortion.

An even bigger contributor to output distortion is the uncertainty in the transistors' threshold voltages. The manufacturer specifies that *none* of the IRF630s produced turn on at a voltage below 2 V. But, *all* turn *on* at some point below 4 V. That is a 100% variation! In the previous examples, it was possible to precisely set the bias to the edge of conduction because the threshold was measured in Example 5-1. The transistor model *always* turns on at 3.6 V. But when you build a push-pull amplifier with real transistors, some may turn on at 2.1 V and others may not go *on* with 3.9 V between the gate and the source. You *could* measure every transistor you put in every amplifier that you build or repair, and then hope that time, temperature, humidity, or the phase of the moon do not cause the transistor to change its characteristics.

You may ask is a volt or two such a big thing? Look back at the curve in Figure 5-4. A change of 1 V sends the current from 1 A to 8 A.

Even a small error or shift in behavior could have a *huge* effect. The only safe solution is to change the bias so that V_{GS} = 2 V. This assures that every transistor is *off*. The positive part of the input signal then pushes the *n*-channel's gate up until eventually it is positive enough to turn *on* and drive current to the load. Similarly, some part of the input negative signal is needed to augment the *p*-channel's negative gate voltage and eventually turn it *on*, creating the negative part of the output.

Example 5-6

1. Calculate new values for R2 and R3 in Figure 5-17 to set the gate voltages at ±2 V, at the bottom of the rated threshold voltage.
2. Simulate the amplifier with the new biasing resistors. Plot the output voltage in response to a 10 V_p input.

Solutions

1. To place 2 V_{dc} across R2 (and R3), resistor R1 (and R4) must drop the rest of the supply voltage. The current through that resistor is

$$I_{R1} = \frac{56\,V_{dc} - 2\,V_{dc}}{22\,k\Omega} = 2.45\,mA_{dc}$$

This current flows through R2, dropping 2 V_{dc}.

$$R2 = \frac{2\,V_{dc}}{2.45\,mA_{dc}} = 816\,\Omega$$

Pick R1 = R4 = 22 kΩ, R2 = R3 = 820 Ω.

2. The composite waveform is shown in Figure 5-18. When the input falls below a few volts, the voltage on the *n*-channel MOSFET's gate drops below V_{th} and the transistor turns off. That's too early. The *p*-channel MOSFET does not turn on until the input is a volt or two negative. That's too late. The result is a flat spot on the output as the input crosses 0 V. This is the result of the 2 V to 4 V threshold variation. Biasing at ±2 V assures that all versions of the transistor are off. But that conservative practice may then require some of the input signal to bring the transistors into full conduction.

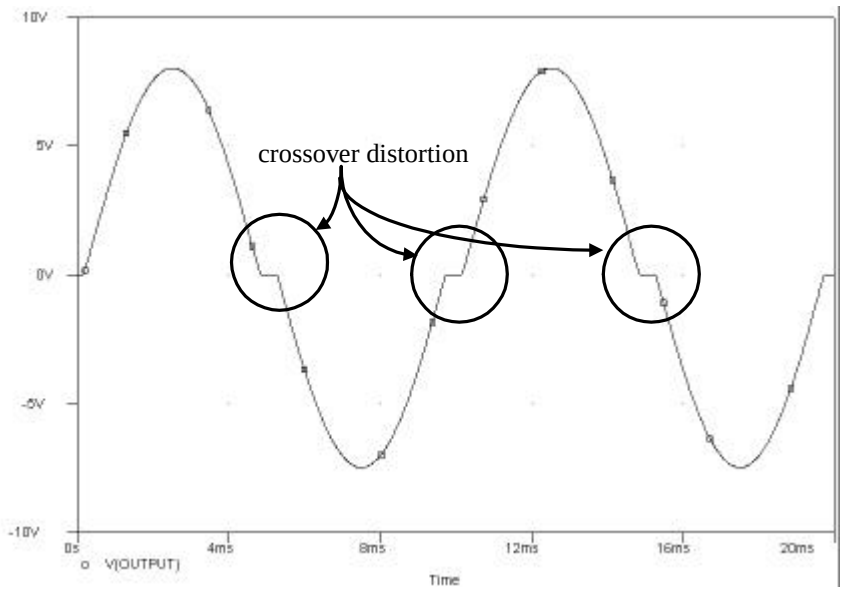

Figure 5-18 Properly biased class B amplifier shows crossover distortion

5.4 Class B Amp with Op Amp Driver

All of the problems with the simple class B push-pull amplifier can be solved by adding an op amp to create a composite amplifier. This was presented in Section 1.3. Look back over that information before you continue. Enclosing the push-pull MOSFET amplifier *within* the negative feedback loop of an op amp based amplifier allows the open loop gain of the op amp to compensate for any nonlinearities, or lack of adequate biasing.

Noninverting Amplifier

The schematic of a noninverting push-pull composite amplifier is given in Figure 5-19.

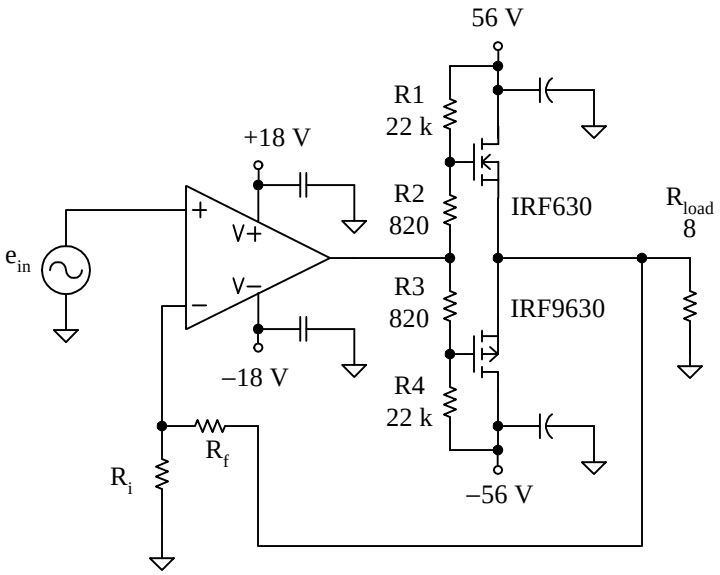

Figure 5-19 Noninverting push-pull composite amplifier

The key feature is that the feedback voltage divider, R_f and R_i, is connected to the *load*. It is *not* connected to the output of the op amp IC. Connecting the feedback directly to the load sends any imperfections at the load (such as nonlinearity or crossover distortion) back to the inverting input of the op amp. Any difference in voltage between that fed back signal and the input on the noninverting pin is amplified by the open loop gain of the op amp (often 100,000 or more).

The output of the op amp jumps significantly, driving the voltage at the load into proper shape. This then assures that the divided version of the load voltage fed back to the op amp's input pin matches the input signal.

Example 5-7

Simulate the performance of the circuit in Figure 5-19 with

e_{in} = 350 mV_{rms}, 100 Hz (typical consumer line output level)
R_f= 10 kΩ, R_i = 520 Ω

Plot the waveform at the load, and the op amp's output.

Solution

The OrCAD probe waveforms are shown in Figure 5-20. There are several items to notice.

1. The output voltage should be

$$V_{\text{p load}} = \left(1 + \frac{10\,\text{k}\Omega}{520\,\Omega}\right) 350\,\text{mV}_{\text{rms}} \times \sqrt{2} = 10.0\,\text{V}_{\text{p}}$$

This is precisely the load voltage. The loss across the bias network and across the transistor have been compensated for by the op amp. The op amp's output is 12 V_p. Overall gain has been realized and set by R_f and R_i.

2. The crossover distortion is gone. Look carefully at the output of the op amp. During the crossover time, when both transistors try to turn off, the output of the op amp makes a jump of several volts to bias the opposite transistor on. So the flat spot in the output has been removed by the step in the op amp's output voltage.

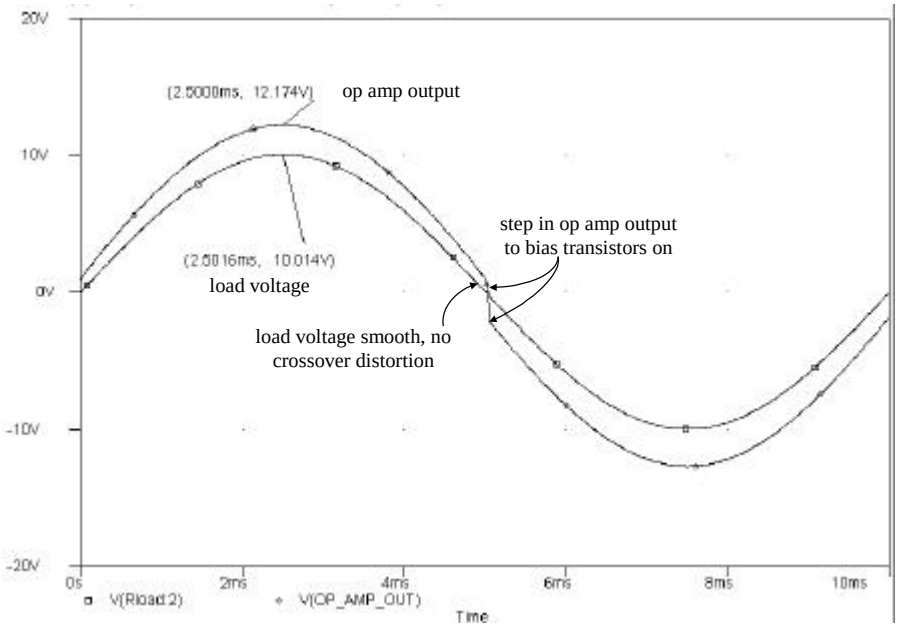

Figure 5-20 Composite amplifier's waveforms for Example 5-7

Practice: How large can the load voltage be driven? What causes this limitation?

Answers: Less than 16 V_p. The op amp's power supply limits its output, and therefore limits the MOSFETs' input and output.

The Suspended Supply Amplifier

To produce a large voltage to the load, the op amp must provide a slightly larger voltage at its output, to drive the MOSFETs' gates. But a conventional op amp's output is limited by its supply voltages, usually ±18 V or less. Delivering a 100 W sinusoidal signal to an 8 Ω load means that the op amp must be able to output over 40 V_p. This cannot happen from an op amp with ±18 V supplies.

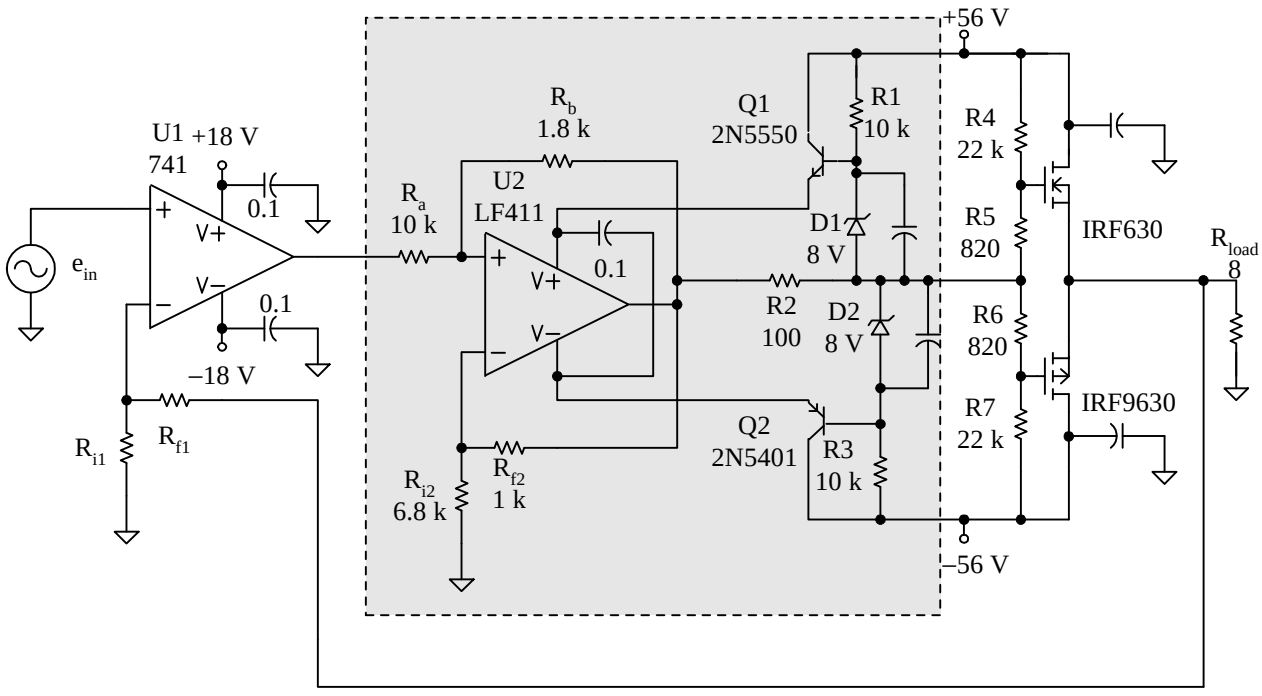

Figure 5-21 Three-stage push-pull composite amplifier

But the suspended supply amplifier presented in Section 1.4 can be powered from the same ±56 V supplies used for the MOSFETs, and can output 45 V_p. Look back over that material before continuing. The suspended supply amplifier is slipped between the output of the op amp and the input to the MOSFET push-pull amplifier, as shown in Figure 5-21.

Layout Concerns

With all of these high voltages and high currents running around in your circuit, *how* you connect the parts is critical. The principles of good high voltage, high current layout are covered in Chapter 2. You should review these before you begin building an amplifier. Incorrectly positioning a single high current wire can drive the entire amplifier into oscillations, or reduce the gain by 30%.

Run separate power lines to the op amps and the power transistors, but keep each as short as possible. This reduces the possibility that the major variation in current from the power transistor is coupled back into the op amp along a shared power bus. With separate power wires, the massive capacitance of the power supply sits between the transistor power pins and the op amp power pins.

The same is done with the common return lines. The op amp needs the cleanest common line you can provide. So do not contaminate it with current from the power output stage. Any noise appearing on the op amp's common line may be interpreted as part of the signal and amplified. Certainly keep the common return from the power transistors and the load separate from the small signal amplifier common, until they get back to the single point common at the power supply connector.

Figure 5-22 is a repeat of Figure 2-15. It shows the interconnection of an amplifier and test instruments. Look carefully at how the supply leads are kept short and separate, as are the two common returns. The signal enters from the left. The suspended supply amplifier stage has been omitted, but there is plenty of space for it in the center of the protoboard. The load is connected at the extreme right. Finally, current from the load returns *directly* to the supply common in its own lead. This assures that any signal created by the large load return current cannot get back into the input small signal amplifier.

Inverting Amplifier

All of the previous examples are for *noninverting* amplifiers. However, you can just as easily use a push-pull power configuration to build an inverting amplifier, an inverting summer, a difference amplifier, an inte-

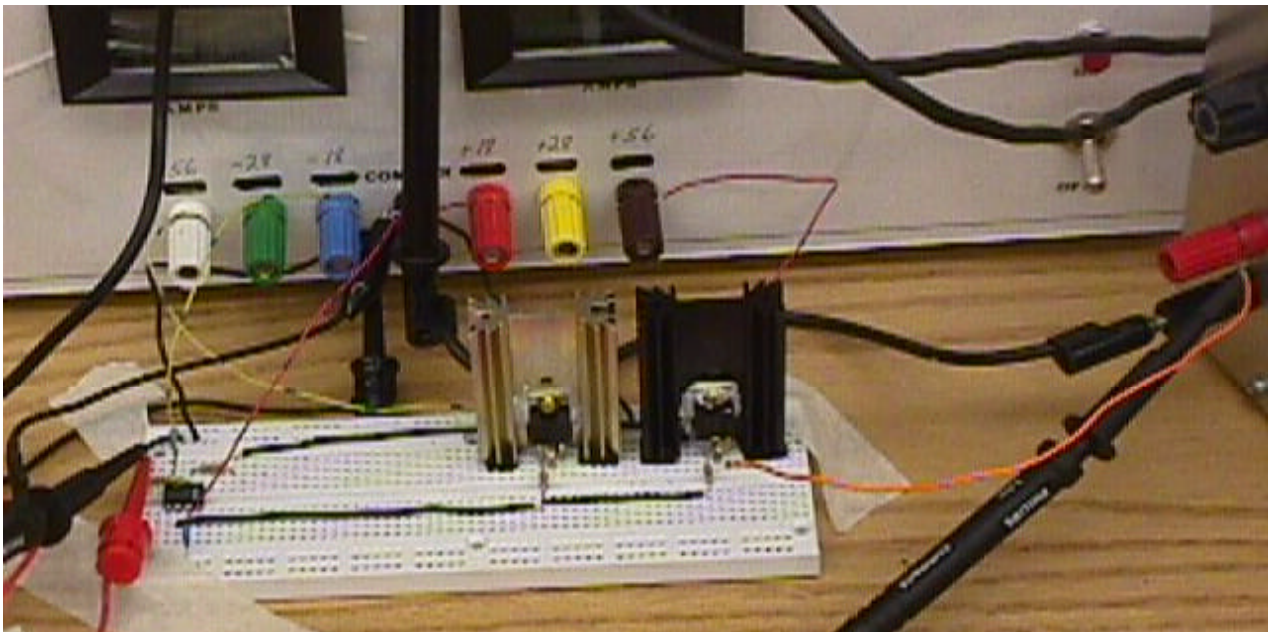

Figure 5-22 Proper amplifier and load connection
(*photo by John Zimmerman*)

grator, an oscillator, or any other configuration in which the simple op amp is used. It is as easy as building the op amp circuit, then inserting the suspended supply second stage and push-pull output stage between the output of the op amp and the load. The negative feedback must stay at the load, *not* at the op amp IC's output. It's as simple as that.

Example 5-8

Design an inverting amplifier to meet the following requirements:

e_{in} = +4 dBu at audio frequencies	input impedance 4.7 kΩ
50 W to a 4 Ω load	T_A = 40°C, $T_{J\,max}$ = 140°C

power supplies: ±18 V_{dc}, ± 28 V_{dc}, ± 56 V_{dc} each at 6 A_{dc}

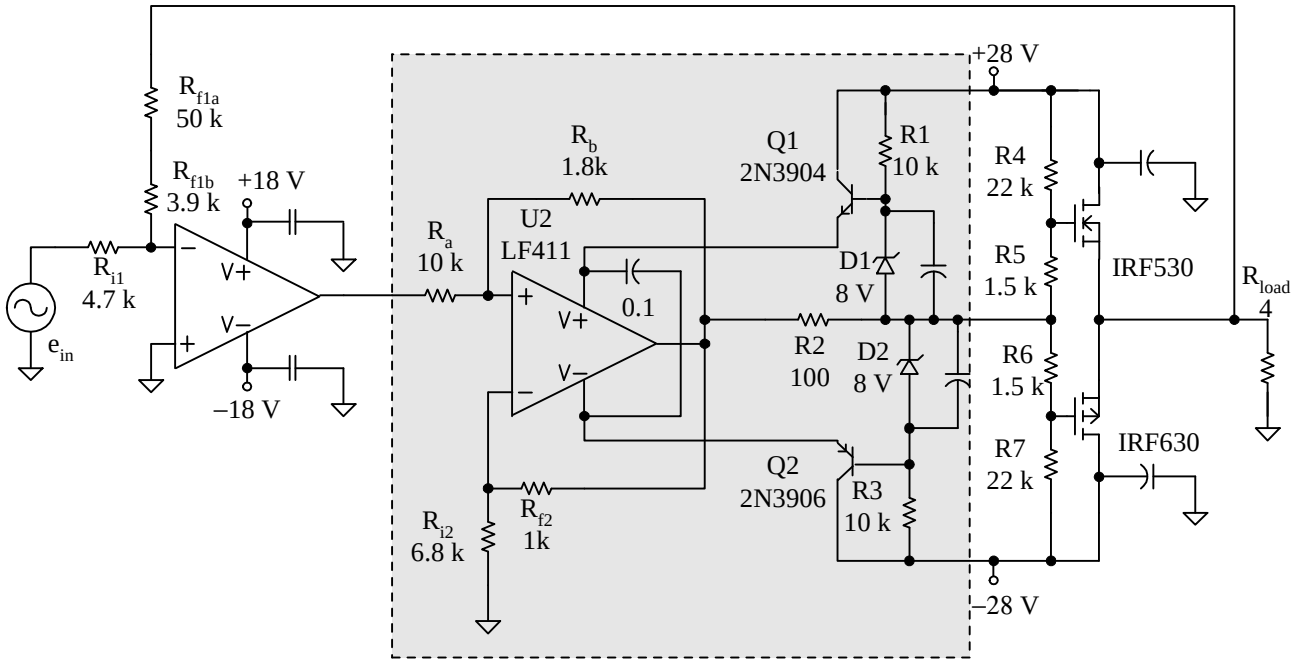

Figure 5-23 Inverting power amplifier

Solution

The power delivered to the load is sinusoidal.

$$P_{\text{load}} = \frac{v_{\text{rms load}}^{\ 2}}{R_{\text{load}}}$$

Solve this for $v_{\text{rms load}}$

$$v_{\text{rms load}} = \sqrt{P_{\text{load}} \times R_{\text{load}}}$$

$$v_{\text{rms load}} = \sqrt{50\,\text{W} \times 4\,\Omega} = 14.1\,\text{V}_{\text{rms}} = 20.0\,\text{V}_{\text{p}}$$

The op amp can have no more than ±18 V_{dc} supplies. But it needs at least 3 V of head room. So the op amp alone cannot output a 20 V_p signal. A suspended supply second stage is needed. It requires about 6 V of head room. For a 20 V_p output the suspended supply stage needs about ±28 V_{dc} supplies. The ±28 V_{dc} supplies are adequate. The ±56 V_{dc} supplies would just

cause the transistors to have to dissipate more power, running hotter and requiring more heat sinking. Choose the ±28 V_{dc} supplies.

The input impedance of an inverting op amp amplifier is set by R_i..

$$R_i = Z_{in} = 4.7\,\text{k}\Omega$$

From Section 4.5 the line level of professional sound equipment is typically +4 dBu = 1.23 V_{rms}. This is the input.

$$A_v = -\frac{v_{load}}{e_{in}}$$

$$A_v = -\frac{14.1\,V_{rms}}{1.23\,V_{rms}} = -11.5$$

The gain of an inverting op amp amplifier is

$$A_v = -\frac{R_f}{R_i}$$

Solving this for R_f

$$R_f = -A_v R_i$$

$$R_f = -(-11.5) \times 4.7\,\text{k}\Omega = 53.9\,\text{k}\Omega$$

You can build R_f with a 50 kΩ resistor in series with a 3.9 kΩ resistor.

The component values in the suspended supply second stage are fine. You can replace the high voltage bipolar transistors with the more common 2N3904 and 2N3906. They work well with ±28 V_{dc} supplies.

Resistors R5 and R6 in the push-pull amplifier must be calculated to set the gate voltages at ±2 V_{dc}. The current through the divider string is

$$I = \frac{28\,V_{dc} - 2\,V_{dc}}{22\,\text{k}\Omega} = 1.18\,\text{mA}_{dc}$$

This current must drop no more than 2 V across R5 and R6.

$$R \le \frac{2\,V_{dc}}{1.18\,\text{mA}_{dc}} = 1.69\,\text{k}\Omega$$

A smaller resistor drops a smaller voltage, assuring that the transistors are off. Pick

$$\mathrm{R5} = \mathrm{R6} = 1.5\ \mathrm{k}\Omega$$

All of the components have been calculated. It's now time to look at the worst case power dissipation, and select the transistors' heat sinks. In Section 4.2 and Figure 4-11, you saw that the worst case power dissipation happens when

$$v_{\mathrm{p\ load@worstcase}} = 0.63 \times E_{\mathrm{supply}}$$

$$v_{\mathrm{p\ load@worstcase}} = 0.63 \times 28\,\mathrm{V} = 17.6\,\mathrm{V_p}$$

$$i_{\mathrm{p\ load@worstcase}} = \frac{17.6\,\mathrm{V_p}}{4\,\Omega} = 4.4\,\mathrm{A_p}$$

This current flows from either supply, through the transistor that is conducting and through the load. For the supplies and the transistors the current is a half-sine of 4.4 $\mathrm{A_p}$. The currents from each transistor combine in the load to create a full sine wave for the load voltage and current waveform.

Each supply provides a steady voltage and a half-sine current. From Table 3-2, the power each delivers is

$$P_{\mathrm{supply@worstcase}} = E_{\mathrm{supply}} \frac{I_{\mathrm{supply}\,p}}{\mathrm{p}}$$

$$P_{\mathrm{supply@worstcase}} = 28\,\mathrm{V_{dc}} \frac{4.4\,\mathrm{A_p}}{\mathrm{p}} = 39\,\mathrm{W}$$

The load carries a full sine wave.

$$P_{\mathrm{load@worstcase}} = \left(I_{\mathrm{rms\ load@worstcase}}\right)^2 \times R_{\mathrm{load}}$$

$$P_{\mathrm{load@worstcase}} = \left(\frac{4.4\,\mathrm{A_p}}{\sqrt{2}}\right)^2 \times 4\,\Omega = 39\,\mathrm{W}$$

Half of this power comes through each of the transistors. The transistors must dissipate the power that the supplies provide but is not delivered to the load.

$$P_{\text{Q@worstcase}} = P_{\text{supply@worstcase}} - \frac{P_{\text{load@worstcase}}}{2}$$

$$P_{\text{Q@worstcase}} = 39\,\text{W} - \frac{39\,\text{W}}{2} = 19.5\,\text{W}$$

In Section 4.3 you saw the thermal characteristics of the transistor and its heat sink.

$$T_{\text{J}} = T_{\text{A}} + P\left(\Theta_{\text{JC}} + \Theta_{\text{CS}} + \Theta_{\text{SA}}\right)$$

Solve this for the thermal resistance of the heat sink.

$$\Theta_{\text{SA max}} = \frac{T_{\text{J max}} - T_{\text{A}}}{P} - \Theta_{\text{JC}} - \Theta_{\text{CS}}$$

For the IRF530, $\Theta_{\text{JC}} < 1.9°\text{C/W}$. Properly installing the heat sink *without* a mica wafer insulator sets $\Theta_{\text{CS}} = 0.2°\text{C/W}$.

$$\Theta_{\text{SA max}} = \frac{140°\text{C} - 40°\text{C}}{19.5\,\text{W}} - 1.9\frac{°\text{C}}{\text{W}} - 0.2\frac{°\text{C}}{\text{W}} = 3.0\frac{°\text{C}}{\text{W}}$$

So, you must provide a heat sink that fits a TO220 package (the IRF530 and IRF9530 package) with a thermal resistance of less than 3°C/W when passing 19.5 W. This is a very low thermal resistance. It may be difficult to find that heat sink. You may have to consider forced air cooling (see Figure 4-13.)

Practice: What effect would changing the power supply to ±56 V_{dc} have?

Answers: Use the 2N5555 and 2N5551 in the suspended supply second stage, IRF630 and IRF9630 in the push-pull stage. Set R5 = R6 = 820 Ω. $v_{\text{load @ worst case}} = 35.3\ V_{\text{p}}$, $P_{\text{load @ worst case}} = 156$ W, $P_{\text{supply @ worst case}} = 156$ W, $P_{\text{Q @ worst case}} = 78$ W. There is *no* heat sink able to keep the transistors from overheating.

Op Amp Selection

Up to this point the op amps have been ignored. At the low frequencies and relatively low gains of the examples, the 741 is an inexpensive, commonly available, through-hole part that works adequately for the first-stage amplifier. But it is this IC's characteristics that set the performance of the entire amplifier. For applications that require higher speed, lower dc offsets, surface mount, or very low cost, you may need to pick a different op amp.

The first-stage op amp's input offset voltage ($\boldsymbol{V_{ios}}$) is multiplied by the overall gain of the amplifier, and shows up across the load as dc.

$$V_{\text{out nonideal}} = A_{\text{amp}} \times V_{\text{ios}}$$

Even though you have been told that *no* current flows into the input of an op amp, in reality there is a small current that *must* flow into the IC in order to bias its input transistors. Without this current, these transistors turn off, and the op amp's output goes into saturation. In the worst case this current flows through R_f, producing a voltage drop.

$$V_{\text{out nonideal}} = A_{\text{amp}} V_{\text{ios}} + I_{\text{bias}} R_{\text{f}}$$

An output dc voltage across the load of only a few hundred millivolts *may* produce enough dc current through the load to disrupt its ac performance. This is particularly true of electromagnetic loads such as loudspeakers and transformers.

If the nonideal dc load current rises to this level, first lower R_f (and R_i to keep the gain correct). If this does not lower the output dc voltage and current enough, then you have to select an op amp with smaller input offset voltage and bias current. Be sure to use the manufacturer's worse case specifications for V_{ios} and I_{bias}, and use the values that accounts for variation with temperature.

Example 5-9

For the circuit of Example 5-8, look up the specifications of the 741C op amp and calculate the worst case dc load current. Is this acceptable for a loud speaker?

Solution

The worst case specifications for the 741C across the entire temperature range are:

$$V_{\text{ios}} = 7.5\,\text{mV}_{\text{dc}}$$

$$I_{\text{bias}} = 800\,\text{nA}_{\text{dc}}$$

Combining these with the values from Example 5-8 gives

$$V_{\text{out nonideal}} = 11.5 \times 7.5\,\text{mV}_{\text{dc}} + 800\,\text{nA}_{\text{dc}} \times 53.9\,\text{k}\Omega = 129\,\text{mV}_{\text{dc}}$$

This voltage produces

$$I_{\text{dc load}} = \frac{129\,\text{mV}_{\text{dc}}}{4\,\Omega} = 32\,\text{mA}_{\text{dc}}$$

Although this does not seem like very much current, it may affect the magnetic characteristics of the loudspeaker. At this point you should refer to the manufacturer of the loudspeaker to verify that 32 mA_{dc} does not adversely affect it.

Practice: If the loudspeaker can only tolerate 20 mA_{dc}, how much V_{ios} can the op amp have, if it has only I_{bias} = 300 pA_{dc}?

Answer: 7 mV_{dc}

There are two specifications that relate to the speed of the op amp. The gain bandwidth product is of concern if the input or output is below 1 V_{p}.

$$GBW = A_{\text{O}} \times f_{\text{H}}$$

where A_{O} = the amplifier's closed loop gain.
f_{H} = the amplifier's high frequency cutoff, the frequency at which the gain has dropped to 0.707 A_{O}.

For larger signals you must be concerned about the slew rate. This specification tells how rapidly the output of the op amp can change. *If* the op amp's output is a pure sine wave, then the required slew rate is

$$SR = 2\pi f_{\text{max}} V_{\text{p opamp out}}$$

Be careful of the powers of ten. Slew rate is specified in V/μs. But the calculation produces V/s.

A difficulty arises because the output of the op amp *steps* several volts as the sine wave passes through common, in order to turn one transistor off and turn the other on. Look back at Figure 5-20. Typically a 741C op amp's dc characteristics are low enough and its gain bandwidth is high enough to be used as the input stage in an audio power amplifier. But as the frequency increases from the 100 Hz in Figure 5-20 into the voice band, the 741C's slew rate is too slow for the jump needed to pre

vent crossover. As the frequency increases, you see a flat spot develop as the load waveform crosses common. An op amp with a faster slew rate is needed. The 741C has a slew rate of 0.5 V/μs. Op amps designed for audio applications often have slew rates of 10 V/μs, even though their gain bandwidth is no faster than the 741C's GBW.

The dc characteristics of the op amp in the suspended supply stage are not particularly important. They must not be so bad that they force that stage into saturation. But any dc added to the signal by the suspended supply only adds (and subtracts) slightly to the bias of the MOSFETs. Any shift in the output this causes is sent to the input op amp as *negative* feedback. That op amp then changes its output to compensate.

However, it is critical that the op amp used in the inner, suspended supply stage, be several times faster (GBW and SR) than the input, first stage op amp. Otherwise, the suspended supply op amp's output responds more slowly than its input, producing a phase lag. At some frequency this lag causes the negative feedback to the input op amp to actually be in-phase (positive), rather than negative, (out of phase) feedback. The amplifier oscillates. In the examples, a LF411 is used for the suspended supply stage. This allows the suspended supply stage to output 50 V_p signals at over 200 kHz. A less expensive, high speed op amp certainly would also work.

5.5 Parallel MOSFETs in a Linear Amp

In Example 5-8, delivering 50 W to a 4 Ω load requires a heat sink with a thermal resistance so low that forced air cooling is needed. More power to the load means a larger supply voltage, which forces the transistor to dissipate so much power that you may not be able to cool it enough to make the amplifier work. A single pair of MOSFETs just cannot deliver much more than about 30 W without inappropriately extreme measures to keep them cool.

To provide more power place several *n*-channel MOSFETs in parallel, instead of the single *n*-channel MOSFET. Of course the *p*-channel MOSFETs should be paralleled too. This certainly seems simple enough. Paralleling three transistors on each side now means that the 5 A_p that must be sent to the load is shared by the three transistors, each carrying only 1.7 A_p. Just solder the three drains together, the gates together, and the sources together. Bolt each transistor to a heat sink and away you go. Right?

When you power up this concoction, one of two things happens. If you are lucky, massive oscillations appear at the output, completely

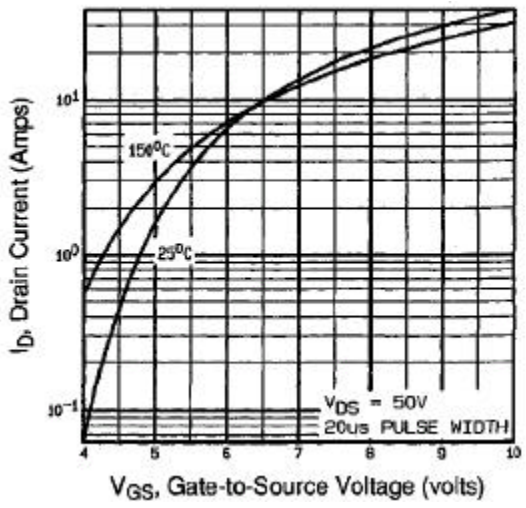

Figure 5-24 Thermal impact on MOSFET performance (*courtesy of International Rectifier*)

overwhelming the signal that is supposed to be there. In the worse case, the transistors rapidly burn out, one at a time, though it probably happens so fast that you think they committed mass suicide.

Paralleling the transistors certainly *seemed*-like a good idea. What did we miss? Look at Figure 5-24. It is a repeat of Figure 5-5, the gate-to-source voltage to drain current characteristic curve.

There are *two* curves on the graph, one at 25°C, the other at 150°C. As the transistor heats up, for the same gate-to-source voltage, the drain current goes *up*. At V_{GS} = 4.5 V_{dc}, 25°C, the transistor passes 0.4 A_{dc}. As it heats up, the current increases, until at 150°C (just before it burns up) it is passing 1.5 A_{dc}. That is a 375% increase in current, just because of a rise in temperature.

It is impractical to electrically and thermally match the transistors you wire in parallel well enough to force them to track each other as temperature rises. Instead, one of the trio will be more sensitive to temperature variations than the other two. As soon as the temperature begins to increase, the most sensitive transistor increases its current much more quickly than the others. Since the op amp is trying to drive a constant voltage (and current) to the load, when the sensitive transistor starts hogging the current, this current is stolen from the other transistors. The hog heats up more ($P = I^2R$), and the others cool. This drives more cur-

rent through the hog and less to the others. The hog heats up more and steals more current. The other two transistors soon have no current while the most sensitive part is trying to carry all of the current you intended be evenly shared. It burns out. Now the same dance is performed by the remaining two transistors, until one of them burns up, leaving only one, which also quick burns up.

The solution is a little negative feedback right at the transistors. Look at Figure 5-25.

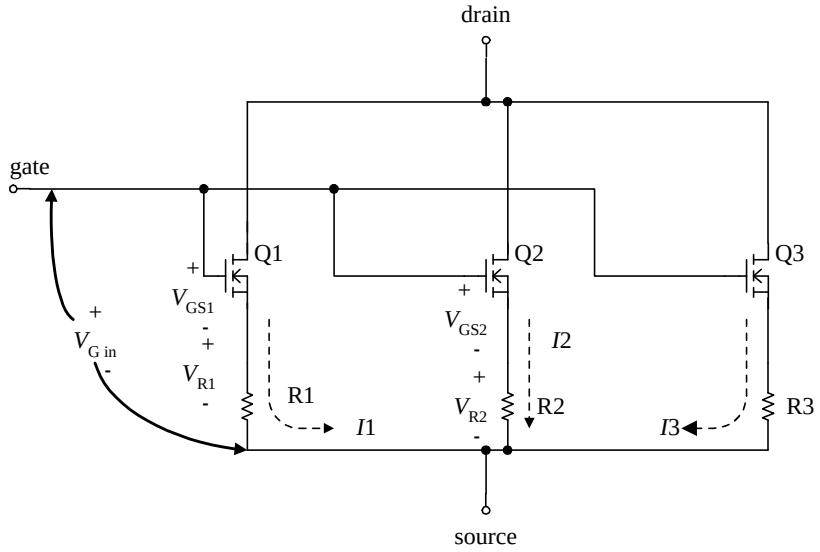

Figure 5-25 Paralleling three MOSFETs in a linear amplifier

The external circuit produces $V_{G\,in}$. In response, each transistor conducts ($I1$, $I2$, and $I3$). Each transistor's current flows through its source resistor, producing a voltage drop (V_{R1}, V_{R2}, and V_{R3}). But it is the transistor's own gate-to-source voltage (V_{GS1}, V_{GS2}, and V_{Gs3}) that actually controls that transistor's current. Summing the loop for Q1 gives

$$V_{G\,in} = V_{GS1} + I1 \times \mathrm{R1}$$

Solve for V_{GS1}.

$$V_{GS1} = V_{G\,in} - I1 \times \mathrm{R1}$$

Remember, $V_{G\ in}$ is the fixed external voltage that is driving the amplifier, $I1$ is what we are trying to assure is not too large, and V_{GS1} is the voltage that directly sets $I1$ (from Figure 5-24).

Assume that Q1 begins to steal current, raising $I1$, and lowering $I2$, and $I3$. When $I1$ increases, the voltage dropped across R1 goes up. This leaves less of the fixed $V_{G\ in}$ for V_{GS1}. But when V_{GS1} goes down, $I1$ also decreases. The initial problem is that $I1$ had increased. This mismatch has been compensated for.

When Q1 steals current from the other transistors, $I2$ and $I3$ drop. This drop lowers V_{R2} and V_{R3}. With less voltage lost across these resistors, more of $V_{G\ in}$ is left between Q2 and Q3's gate and source. This increase in V_{GS2} and V_{GS3} sends their currents up, fighting the theft that Q1 is attempting. Properly sized, R1, R2, and R3 force poorly matched transistors to share the current.

A reasonable value for R1, R2, and R3 is

$$\mathrm{R1} = \mathrm{R2} = \mathrm{R3} > \frac{1}{g_{fs}}$$

where g_{fs} is the transistor's forward transconductance. This specification was introduced in the AC Operation part of Section 5.2. For the transistors used in the examples

$$g_{fs\ IR530} > 6.2\frac{\mathrm{A}}{\mathrm{V}} \qquad g_{fs\ IRF630} > 3.8\frac{\mathrm{A}}{\mathrm{V}}$$

For all power MOSFETs R1, R2, and R3 fall in the 0.1 Ω to 1.0 Ω range. The larger these resistors, the more closely the transistors are forced to share the current. But remember that the load itself may only be 4 Ω to 8 Ω. So a 1 Ω resistor requires one fourth the power delivered to the load. Three of them dissipate almost as much power as the load. So considerations of efficiency, cost, and size mean you should set R1, R2, and R3 as small as possible.

The actual mismatch that these resistors are to correct is very poorly defined by typical manufacturers' specifications. A reasonable approach is to start with resistors twice the minimum suggested above. Build the amplifier and drive it at its worst case point, $V_{p\ load} = 0.63E_{supply}$ for a sine wave, then cycle the temperature over its full ambient range, and monitor the currents. Repeat this test for a variety of transistor samples. If the amplifier is stable, lower the resistors; if not, increase the resistors and repeat the test.

Example 5-10

Replace the single *n*-channel and single *p*-channel MOSFETs of Example 5-8 each with three transistors in parallel. Calculate:

1. The value and wattage of the required resistors.
2. The heat sink's thermal resistance.

Solution

1. Set the resistors at twice the recommended minimum.

$$R = 2 \times \frac{1}{g_{fs}} = \frac{2}{6.3\frac{A}{V}} = 0.32\Omega$$

Pick R = 0.33 Ω

At maximum load current, each transistor and each source resistor carries a half-sine current.

$$I_{max} = \frac{5\,A_p}{3} = 1.7\,A_p$$

This current, flowing through the source resistors, drops

$$V_{R\,max} = 1.7\,A_p \times 0.33\Omega = 0.56\,V_p$$

This half-wave rectified sine current, and half-wave rectified sine voltage require that the resistor dissipate

$$P_R = \frac{V_p I_p}{4}$$

$$P_R = \frac{0.56\,V_p \times 1.7\,A_p}{4} = 0.24\,W$$

This assumes that the current is evenly shared. To account for variation, use ½ W, 0.33 Ω resistors.

2. In Example 5-8, it was calculated that a single transistor would have to dissipate up to 19.5 W, in the worst case. With three transistors, ideally each would dissipate one third of this power. To account for some mismatch, assume that one of the transistors takes half of the power.

$$P_{Q@worstcase} = \frac{19.5\text{W}}{2} = 9.8\text{W}$$

Each of the transistors now needs a heat sink with a thermal resistance no larger than

$$\Theta_{SA\,max} = \frac{T_{J\,max} - T_A}{P_Q} - \Theta_{JC} - \Theta_{CS}$$

$$\Theta_{SA\,max} = \frac{140°\text{C} - 40°\text{C}}{9.8\text{W}} - 1.7\frac{°\text{C}}{\text{W}} - 0.2\frac{°\text{C}}{\text{W}} = 8.3\frac{°\text{C}}{\text{W}}$$

A 8.3°C/W TO220 heat sink is much more practical than the 3°C/W heat sink originally calculated in Example 5-8.

Practice: With a 56 V supply and six paralleled transistors, calculate the maximum load power and the transistor heat sinks.

Answers: $v_{p\,load} \approx 46\ V_p$, $P_{load\,max} = 264$ W, $\Theta_{SA} = 5.8°\text{C/W}$

5.6 Amplifier Protection

In the preceding sections you have seen how to build a linear amplifier capable of delivering hundreds of watts to the load. The traditional way of connecting a load is to turn the amplifier on, set the volume up, then grab a screwdriver and some wire. The owner fiddles with the metal screwdriver, the output terminals, and the loudspeaker until sound comes blasting out. Of course, during this operation the screwdriver and connecting wires short out the amplifier repeatedly. Once the amplifier has survived this operation, the wires are run under a rug, and books. There the wires are subjected to repeated rubbing, chewing from pests, and overheating. An eventual short circuit somewhere along these wires is not unusual.

But under any of these conditions the amplifier must *not* fail, shock the user, spark, overheat or cause a fire. That, however is precisely what would happen with the amplifier you have seen so far. So protection must be added. It should take two forms; current limiting to protect the amplifier and the user from excessive temporary shorts, and thermal shutdown that takes over if the fault continues. Both forms of protection are built into the OPA548 from Chapter 4. Look back over that section.

Current Limiting

Current limiting is illustrated in Figure 5-26. This is a copy of Figure 4-15. When the current is low, the output current is dictated by the output voltage and the load resistance, as set by Ohm's law. Once I_{LIM} is reached, the output current is fixed. Since Ohm's law still applies, once current limiting is entered, further reductions of the load resistance causes the load *voltage* to drop proportionally.

Select

$$I_{LIM} \approx 120\% \times I_{p\ max\ load}$$

This assures enough current to the load at maximum power, but limits the current under a fault.

Figure 5-26 Current limiting characteristic curve.

Example 5-11

Select an appropriate current limit level for an amplifier that delivers up to 200 W into an 8 Ω load.

Solution

Assuming a sinusoidal wave form,

$$P_{load} = \left(I_{rms\ load}\right)^2 \times R_{load}$$

Solve for the load current at the maximum load power.

$$I_{rms\ load} = \sqrt{\frac{P_{load\ max}}{R_{load}}}$$

$$I_{load} = \sqrt{\frac{200\,\text{W}}{8\,\Omega}} = 5.0\,\text{A}_{rms} = 7.1\,\text{A}_{p}$$

Set I_{LIM} to be

$$I_{LIM} = 1.2 \times 7.1\,\text{A}_{p} = 8.5\,\text{A}$$

Practice: Select an appropriate current limit for $P_{load\ max}$ = 50 W, 4 Ω. (Example 5-8)

Answer: Set I_{LIM} = 6.0 A

Current limiting can be installed in the push-pull amplifier with the addition of three components on each side. These are shown in Figure 5-27. On the positive side, D1, Q2, and R_{sc1} have been added between the gate of Q1 and the load. A similar arrangement is installed on the negative side around the *p*-channel MOSFET, Q4. Carefully notice that Q2 is an *npn* transistor while Q3 is *pnp*. Also the direction of D1 and D2 must be observed. Resistors R_{sc1} and R_{sc2} control the current limit level.

At low current on the positive cycle, the voltage developed by the load current flowing through R_{sc1} is small. Transistor Q2 and diode D1 are off. They have no effect. The amplifier operates as it did without current limiting.

When the current becomes large enough to cause V_{Rsc1} to be greater than about 0.6 V, Q2 turns on. During that part of the cycle, input current flows from the generator, through R2, D1 and Q2. This drops more voltage across R2, lowering the signal at the gate. Transistor Q2 is beginning to short out the MOSFET's gate signal.

When the gate voltage drops, the MOSFET's drain (and source) current drops. This lowers the voltage across R_{sc1}, causing Q2 and D1 to conduct less. With less of the input signal current flowing through Q2, less input signal voltage is dropped across R2, and the gate voltage goes up.

Figure 5-27 Current limiting added to a push pull amplifier

But an increase in gate voltage sends the current to the load back up. This increases the voltage across R_{sc1}, turning Q2 and D1 on harder. This draws a little more current from the generator, dropping more voltage across R2, lowering the gate signal, dropping the load current.

The net result of this iterative process is that the load current is controlled at a constant level, independent of the generator voltage, the load resistance, or any op amps between the generator and R2.

Pick

Short circuit resistor value

$$R_{sc} = \frac{0.6\text{V}}{I_{LIM}}$$

The voltages around the transistors and the currents through them are small enough that any commonly available BJT should work. Typically the 2N3904 (*npn*) and 2N3906 (*pnp*) may be used.

The diodes' purpose may not be obvious. When the output voltage is driven to the negative extreme, a large negative voltage is placed on the base of the *npn* transistor, Q2. The voltage from the generator (or suspended supply second stage) is even more negative, to overcome the

losses in the voltage divider and the MOSFET. Depending on the resistors in the divider and the size of the dc supplies, it is possible that the gate of Q1 may be driven more negative than the output. This has no effect on Q1. But, without D1, driving Q2's collector more negative than its base would forward bias Q2's collector-base junction. On the negative half-cycle the intention is that Q1 and Q2 be off. So, D1 is placed in the circuit. When the gate of Q1 is driven more negative than the output, D1 is reverse biased, keeping Q2 off. This diode should have a reverse voltage breakdown rating greater than the load peak voltage, but turn on in a fraction of the highest frequency's half cycle.

Power dissipation calculations for Q1, Q4, and R_{sc1} and R_{sc2} during current limiting are a little different from those you have done so far. There are two major points. When Q1 and Q4 go into current limiting, the load is no longer dissipating any power. It has been shorted. *All* of the power provided by the supplies must be dissipated by the MOSFETs. Secondly, the current wave shape is no longer a half-sine. The current is being forced to a *constant* value. So the current is at a steady value of I_{LIM} for half of the time.

Example 5-12

For Example 5-8, add current limiting with I_{LIM} = 6.0 A. Calculate

1. R_{sc}
2. P_{Rsc}
3. P_Q with $E_{supply} = \pm 28\ V_{dc}$
4. T_J with $T_A = 40°C$, $\Theta_{SA} = 3°C/W$

Solution

1.
$$R_{sc} = \frac{0.6\text{V}}{6\text{A}} = 0.1\Omega$$

Be careful with resistances this small. You must also take into account the trace resistance in series with the resistor.

2. The current through the resistor is a 50% duty cycle square wave with a peak amplitude of 6 A_p and 0.6 V_p. Look back at Table 3-2.

$$P_{Rsc} = DV_pI_p$$

$$P_{Rsc} = 0.5 \times 0.6\,V_p \times 6.0\,A_p = 1.8\,W$$

This is considerably more than the ¼ W that you might have used out of habit. Pick a 0.1 Ω, 2 W resistor.

3. The same calculation applies for the MOSFETs, except, they each have the entire supply voltage across them.

$$P_{\text{MOSFET}} = DV_{\text{p}}I_{\text{p}}$$

$$P_{\text{MOSFET}} = 0.5 \times 28\,\text{V}_{\text{p}} \times 6\,\text{A}_{\text{p}} = 84\text{W}$$

4. So, what happens to the MOSFETs when current limiting takes over to protect the load?

$$T_{\text{J}} = T_{\text{A}} + P\left(\Theta_{\text{JC}} + \Theta_{\text{CS}} + \Theta_{\text{SA}}\right)$$

$$T_{\text{J}} = 40°\text{C} + 84\,\text{W}\left(1.7\frac{°\text{C}}{\text{W}} + 0.2\frac{°\text{C}}{\text{W}} + 3.0\frac{°\text{C}}{\text{W}}\right) = 452°\text{C}$$

In response to a shorted load, the circuit limits the current, saving the wiring and the load, but causes the power transistors to burn up!

Practice: Work steps 4 and 3 backwards to determine the largest short circuit current that would not cause the transistors to burn up. At that I_{LIM}, what is the maximum sinusoidal load power?

Answers: $P_{\text{Q @140C}} = 20$ W, $I_{\text{LIM @ 20 W}} = 1.5\ \text{A}_{\text{p}}$, $P_{\text{sine @ 1.5Ap}} = 4.5$ W

Thermal Shutdown

The MOSFETs fail because they become too hot. So the most direct way to protect them is to measure their temperature, and turn the power supply off if the transistors get too hot. In Chapter 4 you saw that the OPA548 power op amp has thermal shutdown built into the IC.

You cannot directly measure the junction temperature of discrete transistors. But the temperature of the heat sink, *immediately adjacent* to the transistor, can be sensed. This gives a good indication of the transistor's junction temperature. In the last two chapters you have often seen that the junction temperature is related to the *ambient* temperature.

$$T_{\text{J}} = T_{\text{A}} + P\left(\Theta_{\text{JC}} + \Theta_{\text{CS}} + \Theta_{\text{SA}}\right)$$

In terms of the heat sink's temperature, T_{S}, this becomes

$$T_{\text{J}} = T_{\text{S}} + P\left(\Theta_{\text{JC}} + \Theta_{\text{CS}}\right)$$

Example 5-13

Calculate the maximum safe temperature of the heat sink for the amplifier in Example 5-8, holding the junction temperature (T_J) at 130°C when the transistors are dissipating their worst case power of 19.5 W.

Solution

$$T_J = T_S + P(\Theta_{JC} + \Theta_{CS})$$

or

$$T_S = T_J - P(\Theta_{JC} + \Theta_{CS})$$

$$T_S = 130°C - 19.5\,W\left(1.9\frac{°C}{W} + 0.2\frac{°C}{W}\right) = 89°C$$

Practice: For an ambient temperature of 40°C and a heat sink thermal resistance of 3°C/W, calculate the heat sink temperature and the junction temperature if the transistors are forced to dissipate 21 W.

Answers: T_J = 147°C (on the verge of destruction), T_S = 103°C

When dissipating the rated worse case power, the transistors' heat sinks should be no more than 93°C. As soon as the transistors are required to dissipate a little more power, as the result of a fault, the junction temperature rises to the point of semiconductor meltdown, and the heat sink temperature goes over 103°C.

The simplest thermal protection is an IC temperature switch, bonded directly to the heat sink, and rated at 95°C. When the sink reaches that temperature, the IC changes logic levels on its output. You can then use this logic level change to turn the power supply off.

The MAX6501 is such a family of temperature switches. Look at Figure 5-28. The sense temperature is fixed. You just buy the temperature rating that you need. Standard values are 45°C, 55°C, 65°C, 75°C, 85°C, 95°C, 105°C and 115°C. Below its rated temperature, the IC outputs an open. Connect a 3.3 kΩ pull-up resistor between the switch's output and +5 V to produce a legal TTL or CMOS logic high at the IC output pin. When the temperature exceeds its rating, the output pin is shorted to common. This open drain arrangement allows you to tie the output pin of several switches to the same pull-up resistor. If any of the switches sense an over temperature, the line is pulled low to warn you to remove power.

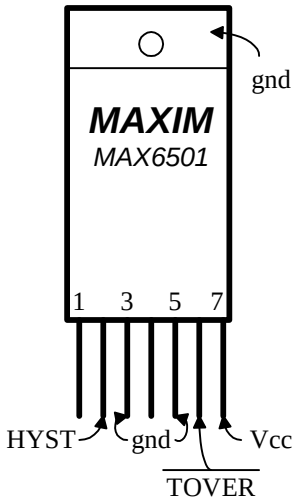

Figure 5-28 MAX6501 TO220 pin diagram

There are two package styles. The surface mount package is designed to monitor the ambient temperature of a printed circuit board. The TO220 package, shown in Figure 5-28, can be connected directly to the same heat sink that contains the MOSFETs. In fact, you could even connect it on the back side of the sink, directly behind the transistor, using the same mounting hardware. However, be sure to use a mica wafer and nylon hardware since the case of the MOSFET is connected to the supply voltage, and the case of the MAX6501 is tied to common.

***Always* provide the proper current limiting and thermal shutdown.**

The MAX6501 also has a hysteresis pin. Connecting this pin to +V provides a 10°C hysteresis. That means that once the IC has output a low in response to a 95°C temperature, the temperature must fall to 85°C before the output returns to an open (that is pulled to +5 V by the pull-up resistor). This allows the system to cool more than just a little before changing the signal that may automatically turn the power supplies back on.

5.7 Driving a Reactive Load

All of your calculations so far, in every section of this book, have assumed that the load is purely resistive. In reality, *every* load has some reactive element. It may be as simple as the inductance contained in the wires that tie the resistor to the amplifier. Or it may be as complicated as a loudspeaker with a crossover network. Loudspeakers alone change their characteristics as frequency varies. At some frequencies, the loudspeaker looks like an 8 Ω resistor; at others it may be purely inductive; and at others purely capacitive; while in between the loudspeaker is a complex reactance. Add the crossover network and the load is definitely complex. Shifting the phase relationship of voltage to current drastically alters the power delivered to the load and the power that the MOSFETs must dissipate. Of course, that alters all of the heat sink and protection calculations.

From your ac circuits course you learned that a complex load shifts the phase relationship of the current through the load with respect to the voltage across it:

$$P_{\text{complex load}} = v_{\text{rms}} i_{\text{rms}} \cos q$$

where q = angle of the current through the load with respect to the voltage across the load.

But for a resistor, or the *resistive part* of the load, current and voltage are in phase. So cos q = 1. That's simple enough.

$$P_{\text{resistive load}} = v_{\text{rms}} i_{\text{rms}} \cos q = v_{\text{rms}} i_{\text{rms}}$$

For the capacitive or inductive *part* of the load, the current leads or lags the voltage across the capacitor or inductor by 90 °. The cos ±90° = 0. So the reactive part of the load dissipates no power. Only the resistive part dissipates power.

With those facts, power calculations around a push-pull power amplifier driving a reactive load are done just as you have done it for a resistive load. You begin by figuring out how much voltage is across the resistive part of the load. After that, you use the same steps and equations as you have done for the OPA548 power op amp or for the discrete MOSFET push-pull amplifier.

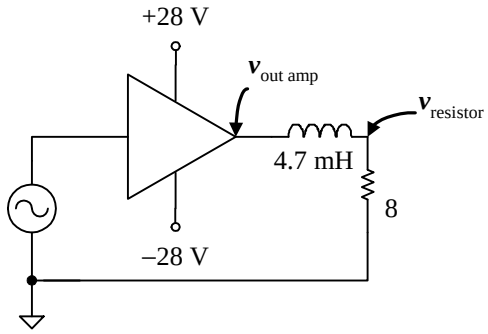

Figure 5-29 Amplifier driving a woofer crossover and loudspeaker

Example 5-14

Calculate the three powers for the circuit in Figure 5-29, given that the output voltage is 15 V_{rms} at 300 Hz.

Solution

First, find the reactance of the inductor.

$$X_L = 2\pi fL$$

$$X_L = 2\pi \times 300\,\text{Hz} \times 4.7\,\text{mH} = 8.9\,\Omega$$

Phasor calculations are needed for the next few steps.

$$\overline{Z_{\text{load}}} = 8\Omega + j8.9\Omega$$

$$\overline{V_{\text{amp out}}} = 15\,\text{V}_{\text{rms}}\angle 0°$$

Calculate the voltage across the resistor.

$$\overline{V_{\text{R}}} = (15\,\text{V}_{\text{rms}}\angle 0°)\frac{8\Omega\angle 0°}{8\Omega + j8.9\Omega} = 10.0\,\text{V}_{\text{rms}}\angle -48°$$

The resistive part of the load dissipates

$$P_{\text{R}} = \frac{(V_{\text{R}})^2}{\text{R}}$$

$$P_{\text{R}} = \frac{(10\,\text{V}_{\text{rms}})^2}{8\Omega} = 12.5\,\text{W}$$

Since the inductive part of the load dissipates no power, the entire load dissipates

$$P_{\text{load}} = P_{\text{R}} = 12.5\,\text{W}$$

The current through the load is the current through the resistance, which is

$$I = \frac{10.0\,\text{V}_{\text{rms}}}{8\Omega} = 1.25\,\text{A}_{\text{rms}} = 1.77\,\text{A}_{\text{p}}$$

This current flows from the 28 V_{dc} supply, a positive half-cycle from the positive supply and a negative half-cycle into the negative supply. *Each* of these dc supplies provides

$$P_{\text{supply}} = V_{\text{dc}}\frac{I_{\text{p}}}{\text{p}}$$

$$P_{\text{supply}} = 28\,\text{V}_{\text{dc}}\frac{1.77\text{A}_{\text{p}}}{\text{p}} = 15.8\,\text{W}$$

Each transistor must dissipate the power provided by its supply that is not passed on to the load.

$$P_{\text{Q}} = P_{\text{supply}} - \frac{P_{\text{load}}}{2}$$

$$P_Q = 15.8\,\text{W} - \frac{12.5\,\text{W}}{2} = 9.6\,\text{W}$$

So, only the first step is different from the power calculations that you have previously done. Use phasor math to calculate the voltage across the resistive part of the load.

Practice: Calculate P_{load}, P_{supply}, and P_Q for a push-pull amplifier powered from ±56 V_{dc}, driving a 10 μF capacitor in series with a 8 Ω resistance. The output from the amplifier is 35 V_{rms} at 3 kHz.

Answers: P_{load} = 106.3 W, P_{supply} = 92.7 W, P_Q = 39.5 W

Summary

Enhancement mode MOSFETs are normally *off*. There are two types, *n*-channel and *p*-channel. The *n*-channel devices are turned on with a positive gate-to-source voltage. *P*-channel MOSFETs bias on with a negative gate-to-source voltage. Once this gate-to-source voltage is above the threshold, drain current increases as the square of gate-to-source voltage. So very little change in input voltage results is a large output current.

The common drain class A amplifier takes advantage of this relatively large transconductance ($\Delta I_D / \Delta V_{GS}$). The transistor is biased well on so that the input voltage can increase and decrease current flow, but cannot turn the transistor off. This produces a low distortion output voltage slightly smaller than the input voltage, but with enough current to drive heavy loads. But the bias current flows through the load requiring it to dissipate a large dc power even when there is no signal. The transistor also must waste a lot of power just idling.

There are two transistors in the class B push-pull amplifier. Each is biased off, but on the edge of conduction. The positive half of the input turns the *n*-channel MOSFET on. The negative half is processed by the *p*-channel. To accommodate the 2 V variation in threshold voltage from part to part, biasing must be set at the lowest specified level. So there must be an increase of several volts at the input before the output begins to conduct. The result is crossover distortion. The signal voltage also is attenuated by the bias network and by the MOSFET itself.

Adding an op amp *around* the push-pull stage solves both of these problems. The negative feedback for this input op amp stage is taken directly from the load. The op amp's output steps at the crossover

and is larger at the peak than the load voltage. This provides a clean signal at the load A suspended supply stage is needed for voltages above 15 V.

Power calculations are done similarly to the power op amp. But each transistor provides only half of the load power. For a sinusoid,

$$P_{\text{load}} = \frac{\left(V_{\text{rms load}}\right)^2}{\text{R}_{\text{load}}} = \left(I_{\text{rms load}}\right)^2 \text{R}_{\text{load}}$$

$$P_{\text{each supply}} = E_{\text{dc supply}} \frac{I_{\text{p supply}}}{\text{p}}$$

$$P_{\text{Q}} = P_{\text{supply}} - \frac{P_{\text{load}}}{2}$$

These calculations should be done at maximum load power to be sure that the supply and the load are adequate, and at the worst case for the transistor ($V_{\text{p load}}$ = 0.63 E_{supply} for a sine wave). Heat sinking calculations are performed at transistor worst case.

MOSFETs can be paralleled to provide load power over 50 W. But to assure that each transistor handles its fair share of current, place a small resistor between the transistor's source and their common connection to the load. These resistors should be a little larger than $1/g_{\text{fs}}$.

Current limiting is implemented by sensing the current leaving the amplifier with a small resistor. When that current develops enough voltage to turn on a bipolar transistor, the gate voltage is reduced, holding the current at a constant level. Under a prolonged short circuit, the power transistors overheat. A temperature switch must be added to the heat sink to turn off the power supply if the sink gets too hot.

Reactive loads force the load current out of phase with the load voltage. The power calculations still work. But you must first use phasor algebra to determine the voltage across the resistive part of the load.

If the objective is to provide more or less power to a load, and you can tolerate distortion levels of a few percent, then the transistors can be operated as switches. Turned on the switch provides full power to the load, and dissipates very little itself. The circuit may be 98% efficient.

During the next chapter you will look at the ideal and nonideal characteristics of MOSFETs used as switches. Paralleling MOSFET switches is easy. The transistors can be used to apply and remove power (high side) or to connect to circuit common (low side). Special gate drive circuits are needed to realize the advantages of high speed power switching

Problems

Enhancement Mode MOSFETs

5-1 Locate data sheets for the IRF530, IRF630, IRF9530, and IRF9630. Construct a table with a column for each of these transistors and a row for each of the following specifications:

V_{DSS}, $I_{D\,max}$, $V_{GS\,max}$, $T_{J\,max}$, $\Theta_{JC\,max}$, V_{th}, g_{fs}

5-2 **a.** For the IRF530 data determine I_D for V_{GS} = 4.5 V and T_J = 25°C.

b. For problem 5-2a, what threshold voltage is assumed? How do you know?

c. If V_{th} = 2.5 V, find I_D for V_{GS} = 4.5 V and T_J = 25°C.

d. Compare your answers to problem 5-2a and problem 5-2c. Discuss the effect of this variation.

5-3 **a.** For the IRF9530 data determine I_D for V_{GS} = –4.5 V and T_J = 25°C.

b. Compare your answers to problem 5-2a and problem 5-3a. Do the two transistors appear to be complements?

Class A Operation

5-4 Design a class A power amplifier using an IRF530. Set E_{supply} = 18 V_{dc}, R_{load} = 2 Ω, $e_{in\,max}$ = 5 V_p

5-5 For your design of Problem 5-4,

a. assuming no input signal, calculate P_{load}, P_{supply}, and P_Q.

b. with e_{in} = 5 V_p calculate $v_{G\,rms}$, $v_{rms\,load}$ and $P_{load\,from\,ac\,signal}$.

c. discuss the efficiency of this amplifier.

Class B Push-Pull Amplifier

5-6 Given that R1 = R4 = 33 kΩ, with ±28 V_{dc} power supplies, calculate the value of R2 and R3 to properly bias a class B amplifier using an IFR530 and IRF9530.

5-7 For the circuit designed in Problem 5-6, with e_{in}= 0 V_{rms}, calculate:

V_{G1}, I_{Q1}, V_{G2}, I_{Q2}, V_{load}, P_{supply}. P_{Q1}, and P_{Q2}

5-8 For the circuit designed in Problem 5-6, with R_{load} = 4 Ω, e_{in}= 10 V_{rms}, calculate:

$v_{G\,rms}$, $v_{rms\,load}$, P_{load}, $P_{supply,}$ and P_Q

Class B Amplifier with Op Amp Driver

5-9 Design a class B amplifier with a noninverting gain of 48, capable of delivering 8 W into an 8 Ω resistive load. Determine the following:

supply voltage (±18 V, ±28 V, or ±56 V)
bias components
R_f and R_i
$P_{Q\ @\ worse\ case}$ (assume a sine wave input)
heat sink thermal resistance (T_A = 50°C)

5-10 Design a class B amplifier with an inverting gain of −100, capable of delivering 60 W into an 8 Ω resistive load. Is a suspended supply second stage necessary? Explain.

5-11 Calculate the gain bandwidth and the slew rate needed for the op amp in Problem 5-9 assuming that the amplifier is to be used across the entire audio range.

5-12 Calculate the gain bandwidth and the slew rate needed for the op amp in Problem 5-10 assuming that the amplifier is to be used up to 3 kHz (the voice band).

Parallel MOSFETs in Linear Applications

5-13 A class B three-stage amplifier has a ±72 V_{dc} supply, an 8 Ω load and a sinusoidal input. If each transistor has a 10°C/W heat sink, and the ambient temperature is 60°C, determine the:

a. number of *n*-channel and *p*-channel transistors.
b. power available to the load.
c. resistance and wattage of the source resistors.

5-14 Four IRF530 transistors are paralleled as the push element in a dc amplifier that outputs 0 V_{dc} to +12 V_{dc} at 5 A_{dc} from an 18 V_{dc} supply. Assuming an ambient temperature of 40°C, calculate:

a. thermal resistance of the transistors' heat sinks.
b. resistance and wattage of the source resistors.

Amplifier Protection

5-15 **a.** Add the components necessary to the amplifier in Problem 5-14 to limit the load current to 5 A_{dc}.
b. Calculate the wattage of the current limit resistor.

5-16 **a.** If the load for Problem 5-15 shorts, calculate the power that each transistor must dissipate.
b. Using the heat sink selected in Problem 5-14, calculate the junction temperature of each transistor if the load shorts.

5-17 An IRF9530 is dissipating 10 W, with a case temperature of 105°C. Calculate the junction temperature.

5-18 An IRF9530 has a case temperature of 85°C. Determine:

a. a *safe* junction temperature.
b. the power the transistor can dissipate at these temperatures.

Reactive Loads

5-19 A class B three-stage amplifier has a ±72 V_{dc} supply, and a complex load made from a 2.2 mH inductor in series with a 12 Ω resistance. For a 1 kHz sine wave, maximum output amplitude, calculate P_{load}, $P_{each\ supply}$, and $P_{each\ transistor}$.

5-20 A class B three-stage amplifier has a ±56 V_{dc} supply, and a complex load made from a 68 μF capacitor in series with a 4 Ω resistance. For a 500 Hz sine wave, maximum output amplitude, calculate P_{load}, $P_{each\ supply}$, and $P_{each\ transistor}$.

Class B Amplifier Lab Exercise

A. *N*-Channel Enhancement Mode MOSFET Characteristics

1. Build the circuit in Figure 5-30.

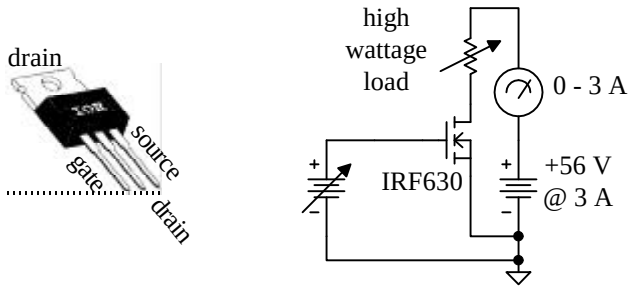

Figure 5-30 V_{GS} versus I_D test circuit

2. Assure that :
- **a.** the TO220 heat sink is properly installed.
- **b.** the load rheostat is set to at least 110 Ω.
- **c.** the +56 V supply is turned *off*.
- **d.** the transistor's source returns to the +56 V_{dc} supply's single point common in its own lead.
- **e.** the low voltage adjustable supply's common returns to the +56 V_{dc} supply's single point common in its own lead.
- **f.** the low voltage adjustable supply is set to 0 V_{dc}.

3. While watching the ammeter in the +56V_{dc} line, turn on the +56 V_{dc} supply. If its current exceeds 100 mA_{dc} turn the supply *off* and determine the error.

4. Measure and record the drain current.

5. Lower the load rheostat to the value indicated below, then increase V_{GS} until the drain current equals the indicated current. Record V_{GS}.. Repeat the procedure for the five points.

110 Ω, 0.1 A_d 70 Ω, 0.5 A_d 40 Ω, 1.0 A_{dc}
25 Ω, 1.5 A_{dc} 20 Ω, 2.0 A_{dc}

6. Complete a plot of V_{GS} (x axis) versus I_D (y axis).

B. Class B Operation

1. Build the circuit in Figure 5-31. Neatness counts. Carefully follow the steps from Chapter 2.

2. Assure that
- **a.** the ±56 V_{dc} power supply is turned *off*.
- **b.** R_{load} is set to its maximum value.
- **c.** the load's return is run *directly* back to the power supply's common (single common point), *not* back to the amplifier's or generator's common.
- **d.** the amplifier's and the generator's common returns to the power supply's common in its own, separate wire.

3. Set the input signal generator to provide an input signal of:

0 V_{dc}, 0 V_{rms}, 100 Hz

4. Connect the generator to the circuit. Do *not* leave the node between R2 and R3 open.

Figure 5-31 Class B push-pull amplifier

5. Monitor the load voltage with the oscilloscope and digital multimeter. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply. If any of these values are more than a few tenths of a volt or amp, stop and determine the problem.
6. Set the input signal generator to provide an input signal of

   $0\ V_{dc}, \quad 20\ V_{pp}, \quad 100\ Hz$

7. Monitor the load voltage with the oscilloscope and digital multimeter. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply.
8. Compare the results with theory. If there are any notable errors, stop and determine the mistake before continuing.
9. Lower the load resistance to 12 Ω.
10. Monitor the load voltage with the oscilloscope and digital multimeter. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply.
11. Compare the results with theory. If there are any notable errors, stop and determine the mistake before continuing.
12. When the results are numerically correct, record and explain the wave shape.
13. Set the signal generator to 0 V_{dc}, 0 V_{rms}. Turn the ±56 V_{dc} supply off.

C. Push-Pull Amplifier with Op Amp Driver

1. Build the circuit in Figure 5-32. Neatness counts. Carefully follow the steps from Chapter 2.
2. Set R_{load} to its maximum resistance.
3. Verify that the signal generator is set to 0 V_{dc} and 0 V_{rms}.
4. Turn on the ±18 V_{dc} and ±56 V_{dc} power supplies.
5. Verify that the load voltage (dc and ac) and the current from the +56 V_{dc} supply are all negligible. Record their actual values.
6. Set the input signal generator to 0 V_{dc}, 100 mV_{rms}, 100 Hz.

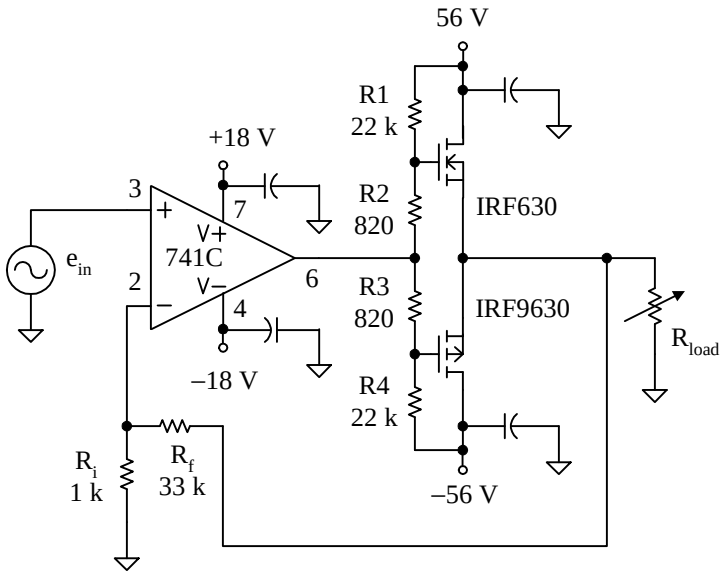

Figure 5-32 Push-pull power amplifier with an op amp driver

7. Monitor the load voltage with the oscilloscope and digital multimeter. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply.
8. Compare the results with theory. If there are any notable errors, stop and determine the mistake before continuing.
9. Gradually lower the load resistance while carefully monitoring the supply current. Be sure that the supply current does not exceed 0.3 A_{dc}. Lower the load resistance to 12 Ω.
10. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply.
11. Compare the results with theory. If there are any notable errors, stop and determine the mistake before continuing.
12. Record the waveform at the load and at the output of the op amp. Explain each.

13. Increase the input amplitude until the load voltage clips. Record this peak load voltage. Explain the reason for the limiting.

14. Set the signal generator to 0 V_{dc}, 0 V_{rms}. Turn the ±56 V_{dc} supply off.

D. Three-Stage Push-Pull Amplifier

1. Build the circuit in Figure 5-33. Neatness counts. Carefully follow the steps from Chapter 2.

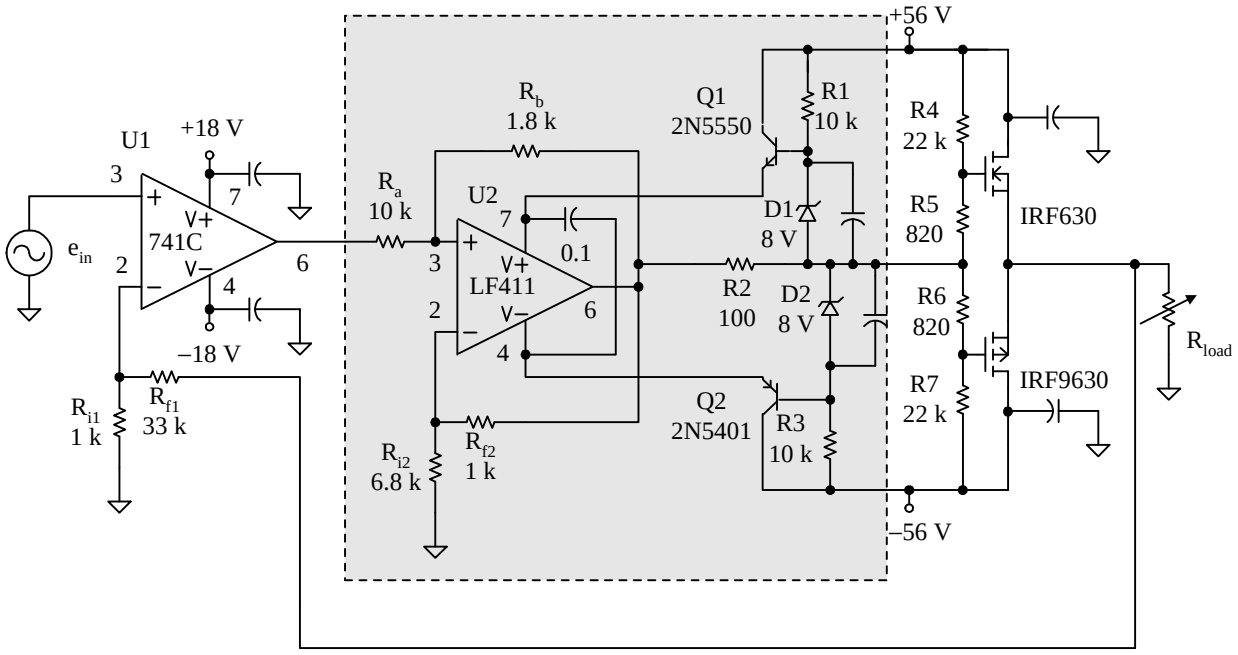

Figure 5-33 Three-stage push-pull amplifier

2. Set R_{load} to its maximum resistance.

3. Verify that the signal generator is set to 0 V_{dc} and 0 V_{rms}.

4. Turn on the ±18 V_{dc} and ±56 V_{dc} power supplies.

5. Verify that the load voltage dc and ac and the current from the +56 V_{dc} supply are all negligible. Record their actual values.

6. Set the input signal generator to 0 V_{dc}, 100 mV_{rms}, 100 Hz.

7. Monitor the load voltage with the oscilloscope and digital multimeter. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply.
8. Compare the results with theory. If there are any notable errors, stop and determine the mistake before continuing.
9. Gradually lower the load resistance while carefully monitoring the supply current. Be sure that the supply current does not exceed 0.5 A_{dc}. Lower the load resistance to 24 Ω.
10. Measure and record the load dc and rms voltages and the current from the +56 V_{dc} supply.
11. Compare the results with theory. If there are any notable errors, stop and determine the mistake before continuing.
12. Increase the input amplitude until the load voltage clips. Record this peak load voltage.
13. Lower the input signal amplitude until the output is as large as possible without clipping either peak.
14. Increase the input frequency until the output amplitude drops or until the output wave shape begins to distort. Explain the cause of the drop in amplitude or the distortion caused by an increase in frequency.
15. Set the signal generator to 0 V_{dc}, 0 V_{rms}. Turn the ±56 V_{dc} supply off.