CpE358/CS381

Switching Theory and Logical Design

Class 4

Today

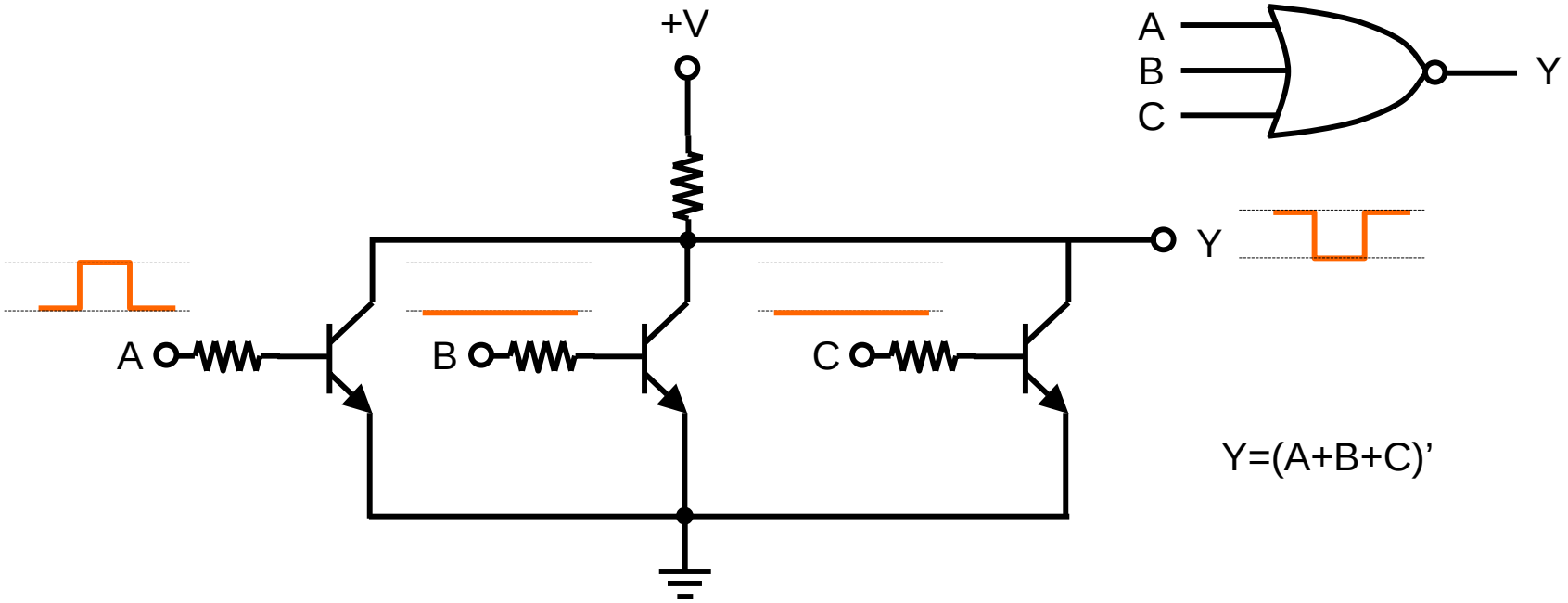
- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Hazards, Races, and time related issues in digital design (Ch 9)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- Synchronous vs. asynchronous design (Ch 9)
- Counters, shift register circuits (Ch 6)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

Logic Families

- RTL – Resistor-Transistor Logic
- DTL – Diode-Transistor Logic
- TTL – Transistor-Transistor Logic
- ECL – Emitter-Coupled Logic
- MOS – Metal-oxide semiconductor
- CMOS – Complementary MOS

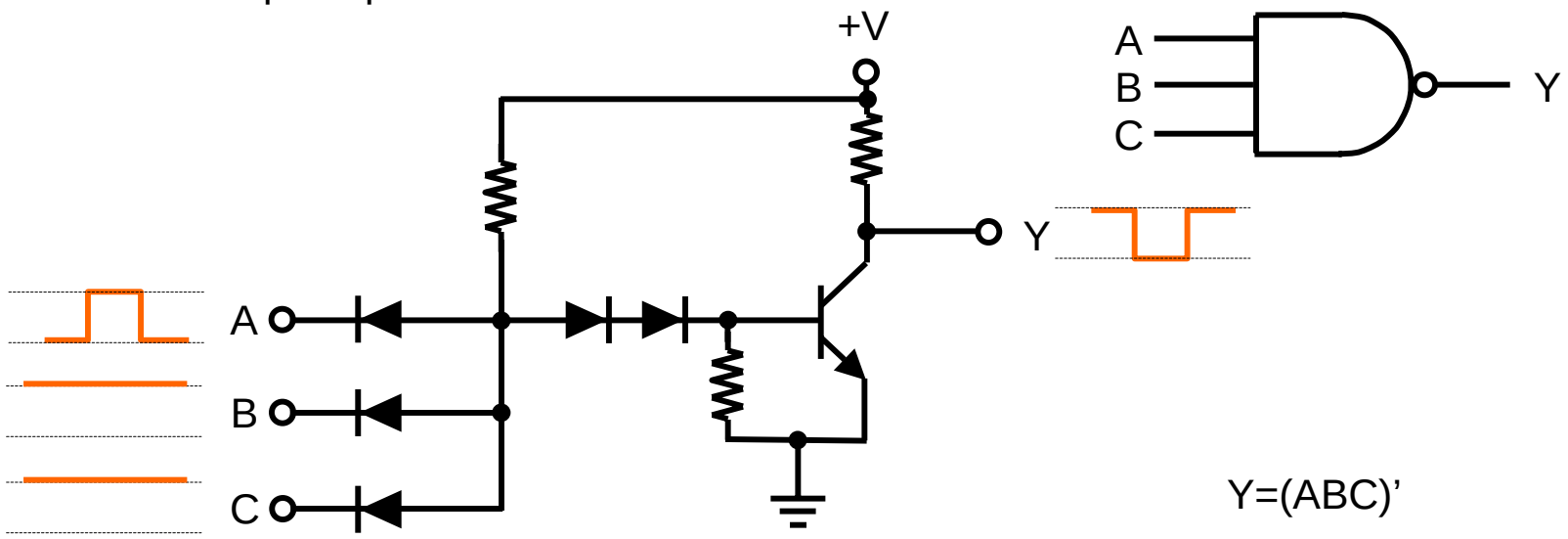
RTL

- RTL Characteristics:
  - Minimum component count
  - Passive “pull-up”



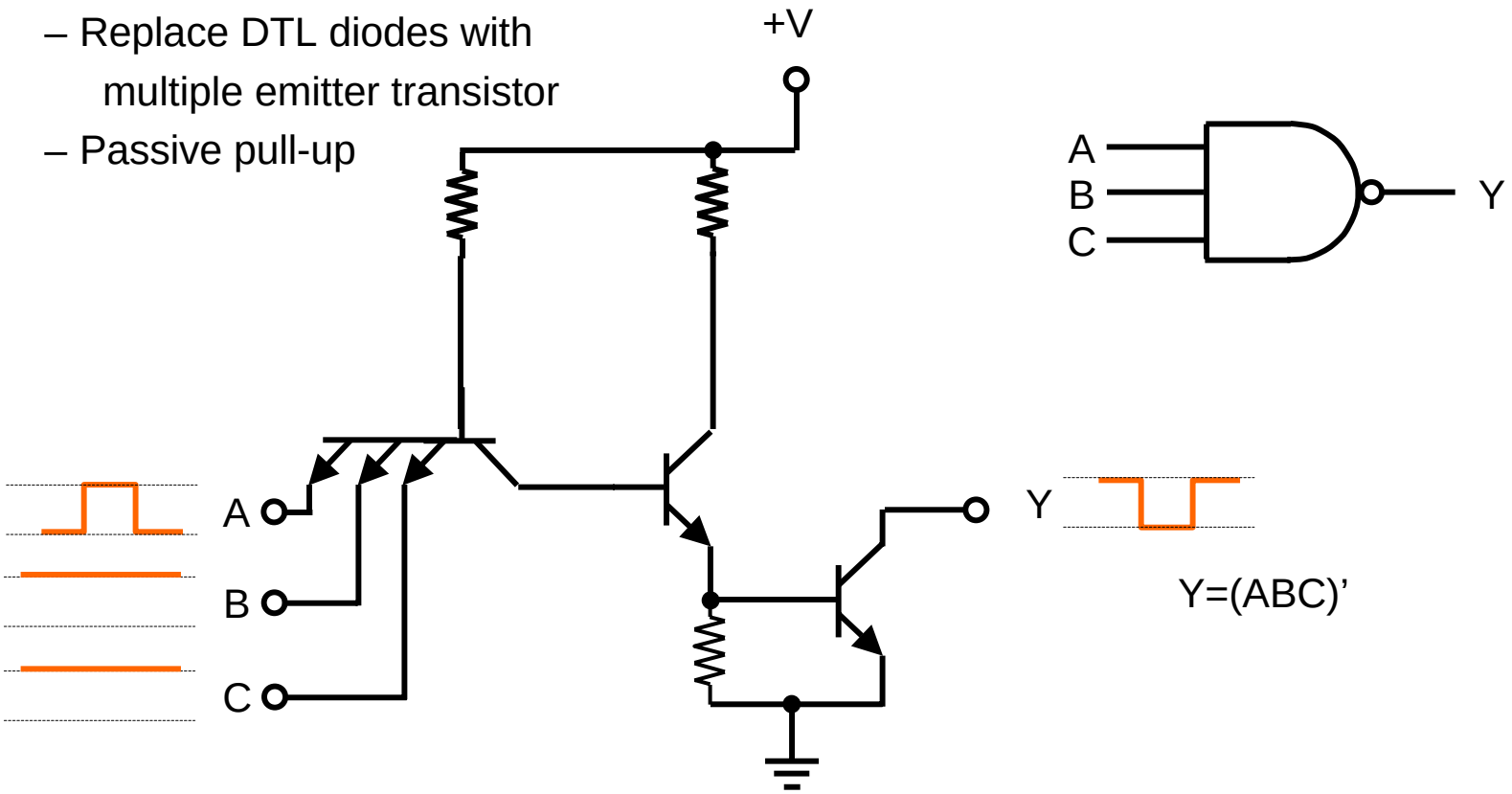
DTL

- DTL characteristics:
  - Diode AND circuit at input
  - Passive pull-up



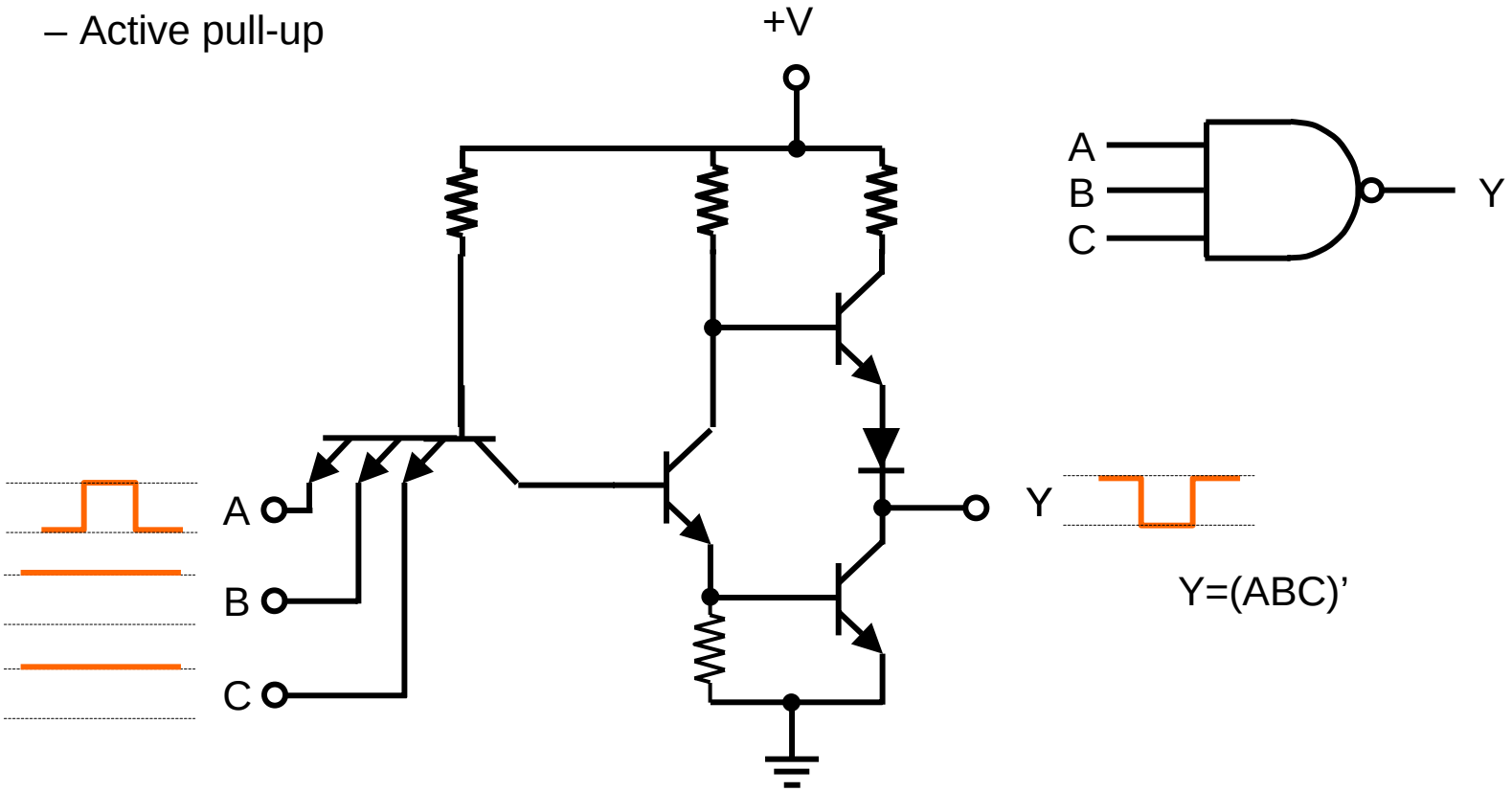
Open Collector TTL

- TTL Characteristics:
  - Replace DTL diodes with multiple emitter transistor
  - Passive pull-up



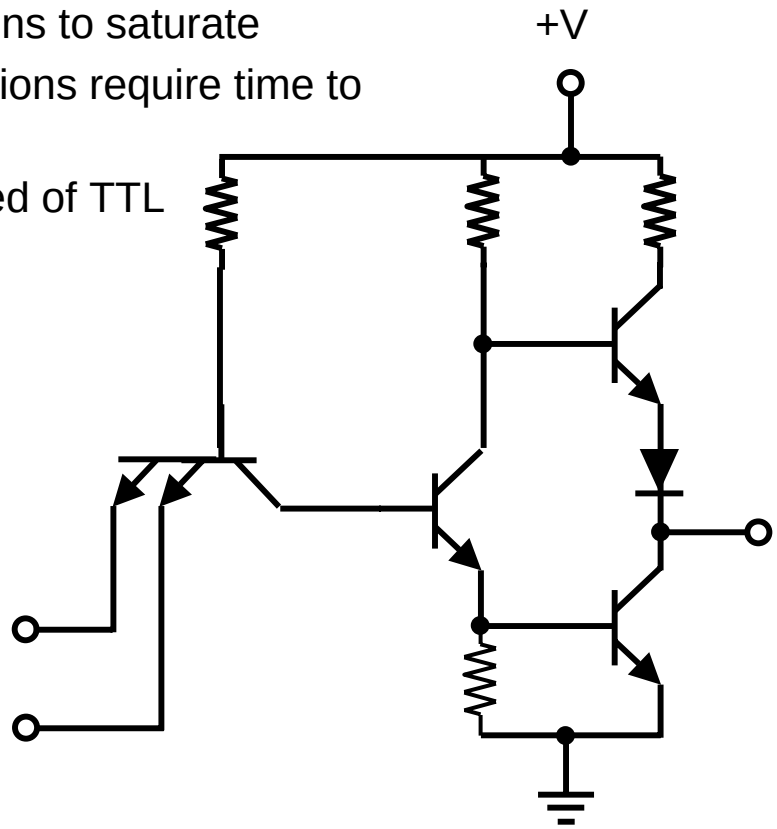
Totem Pole TTL

- Totem-pole TTL Characteristics:
  - Active pull-up



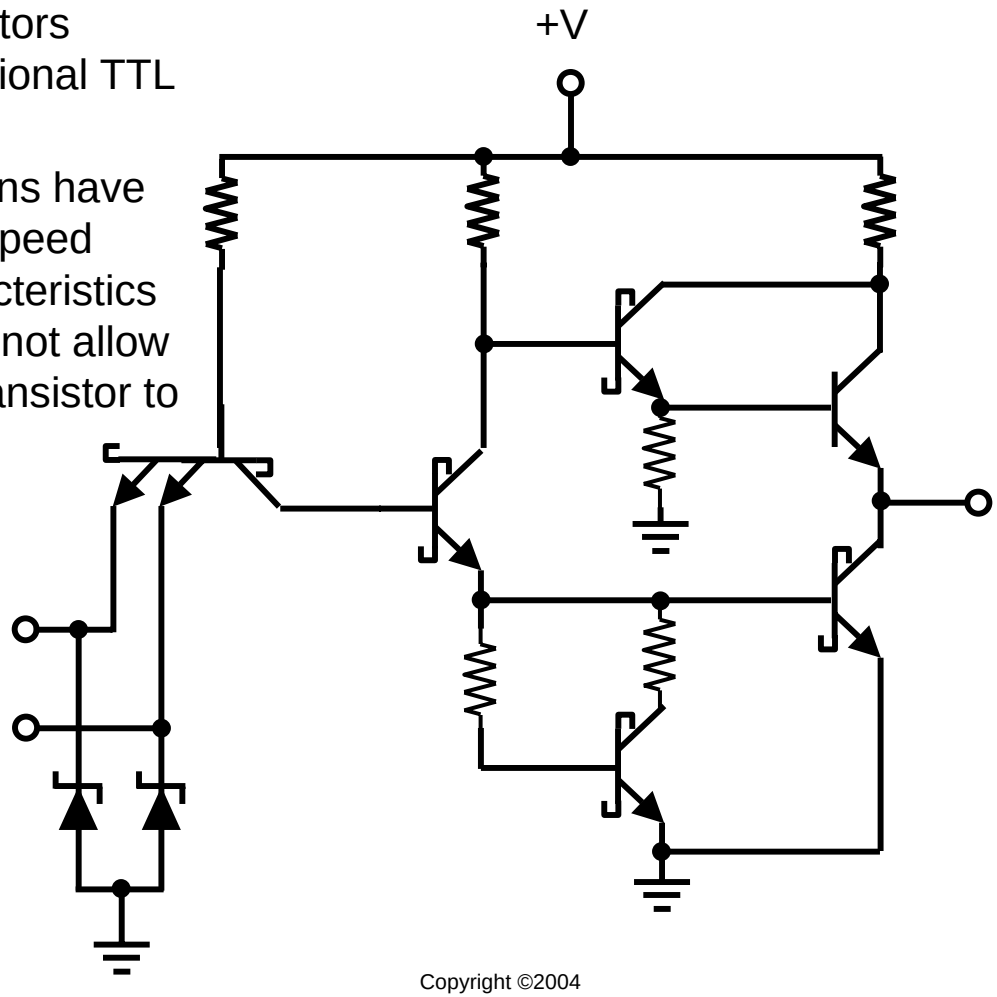
Conventional TTL

- Switching transistors on/off requires junctions to saturate
- Saturated junctions require time to recover
- This limits speed of TTL

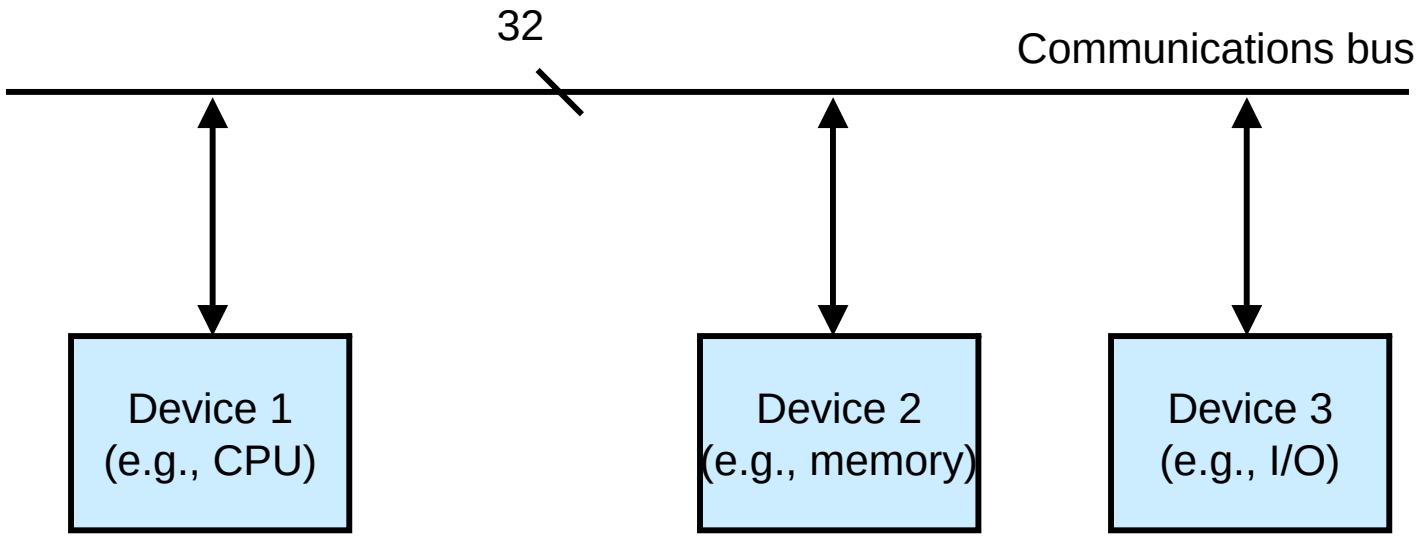


Schottky TTL

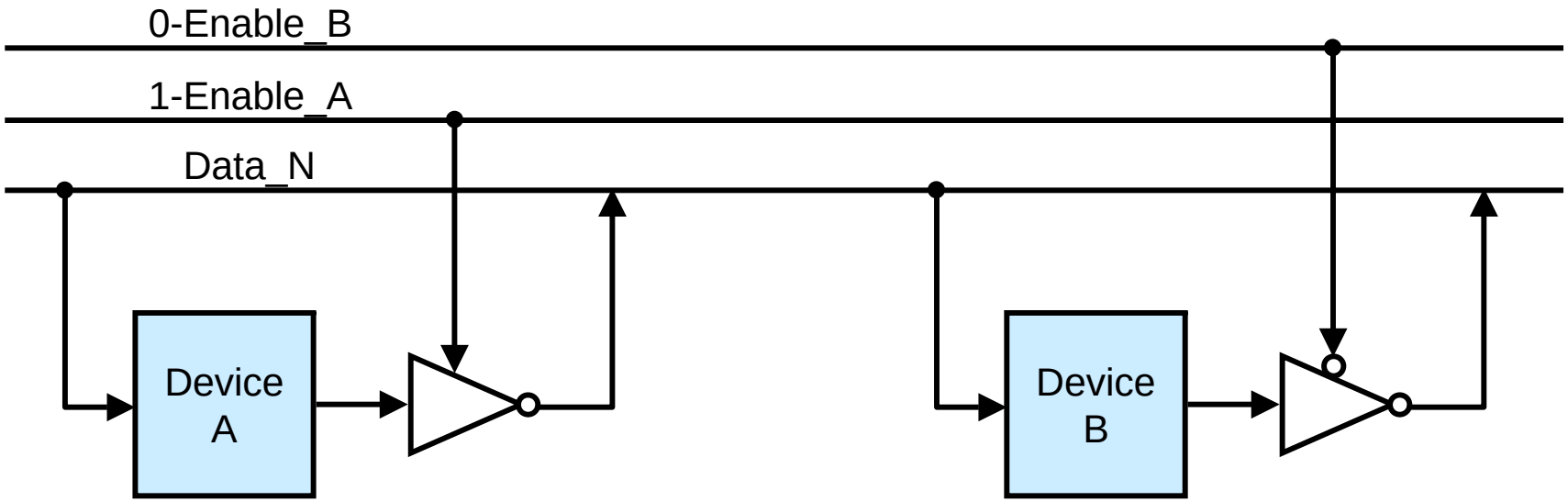
- Schottky diodes and Schottky transistors replace conventional TTL transistors
- Schottky junctions have improved high speed switching characteristics because the do not allow the switching transistor to saturate



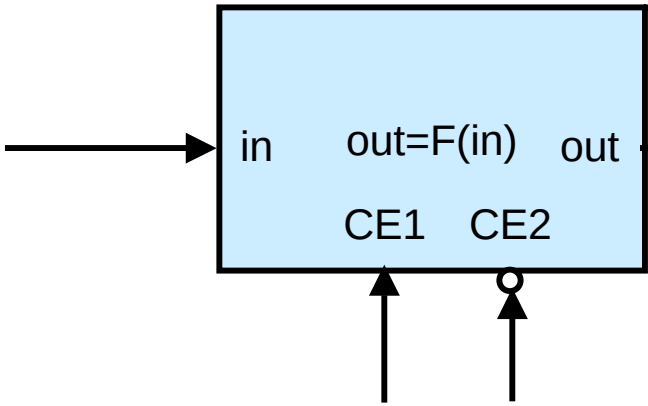
Tri-State Logic



Tri-State Logic



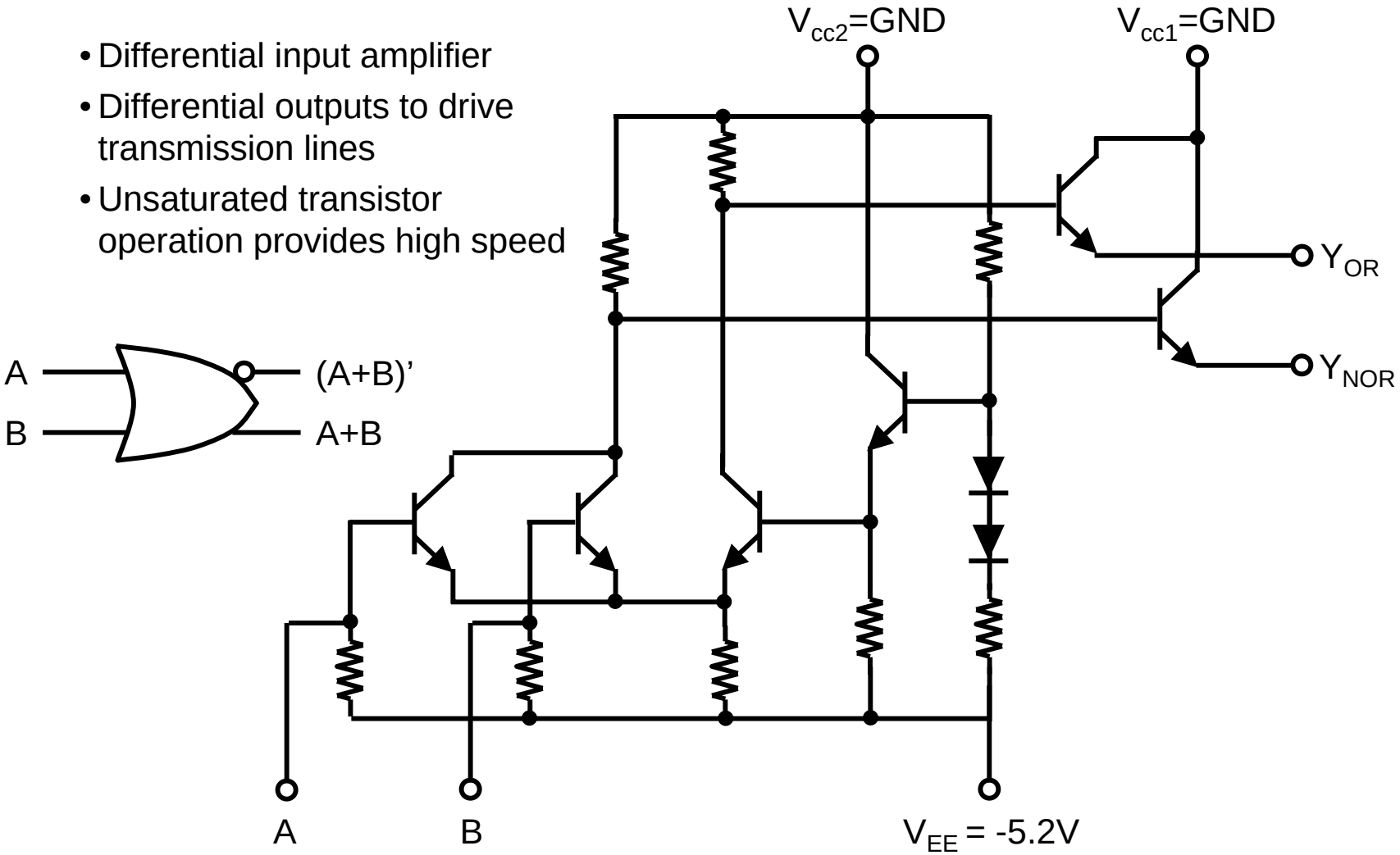
Tri-state Devices



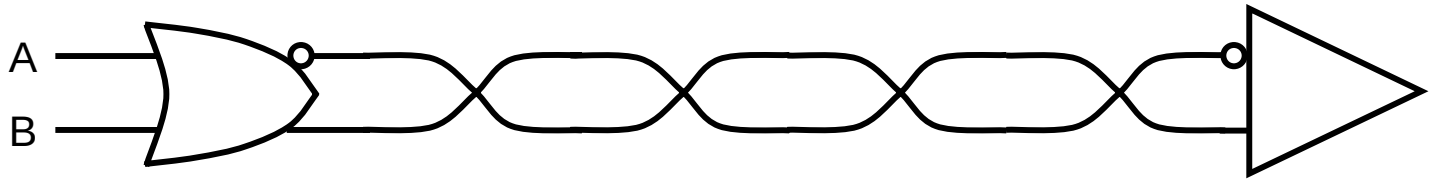

```
if(CE1=1 AND CE2=0)
   {
    out=F(in)
    }
     else
        out=Hi-Z;
```

ECL

- Differential input amplifier
- Differential outputs to drive transmission lines
- Unsaturated transistor operation provides high speed

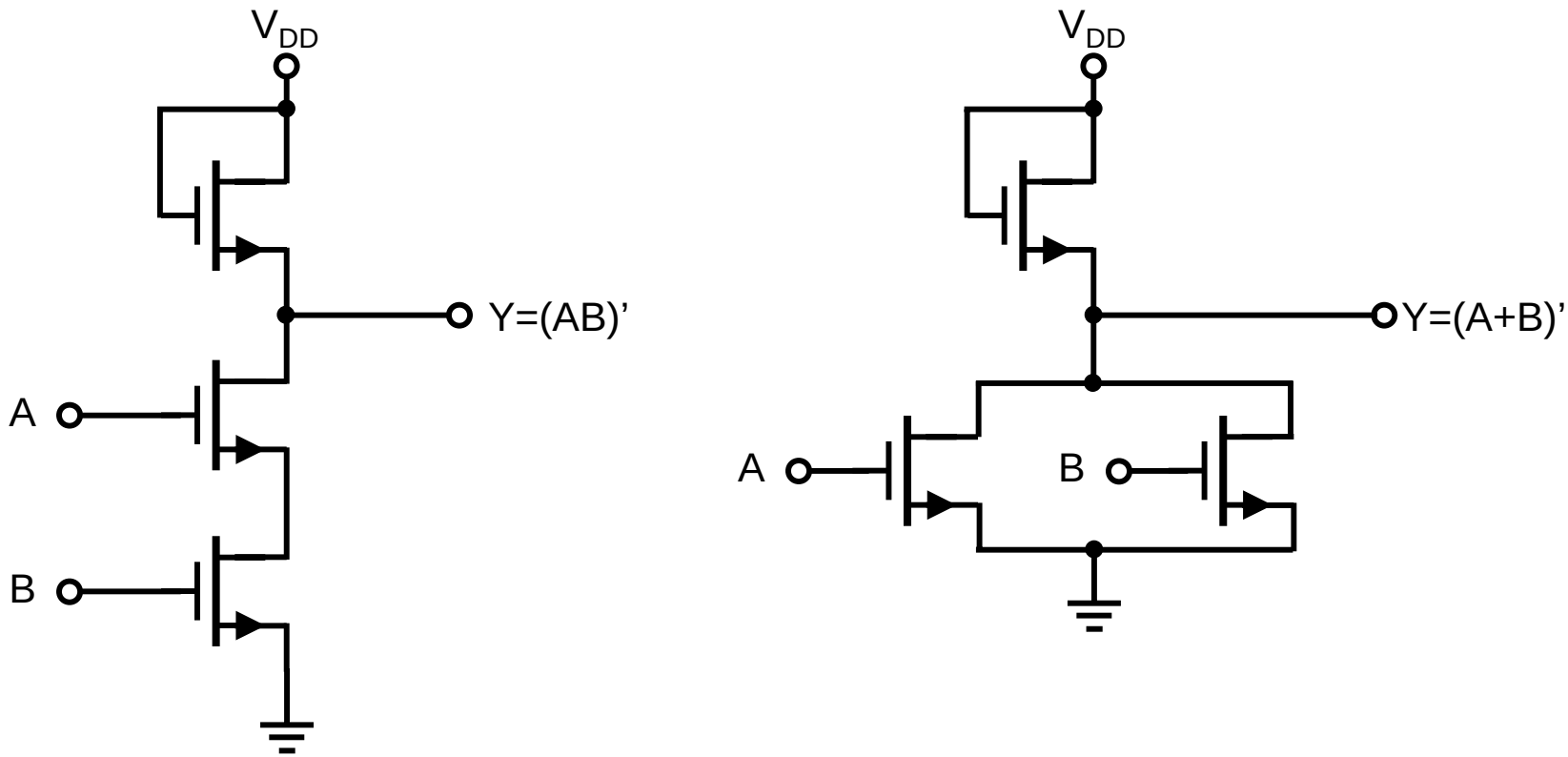


ECL



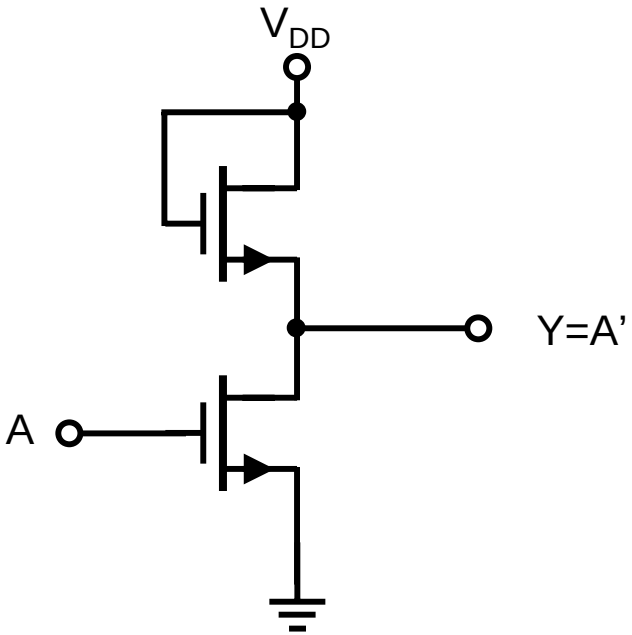
Differential
Input
Receiver

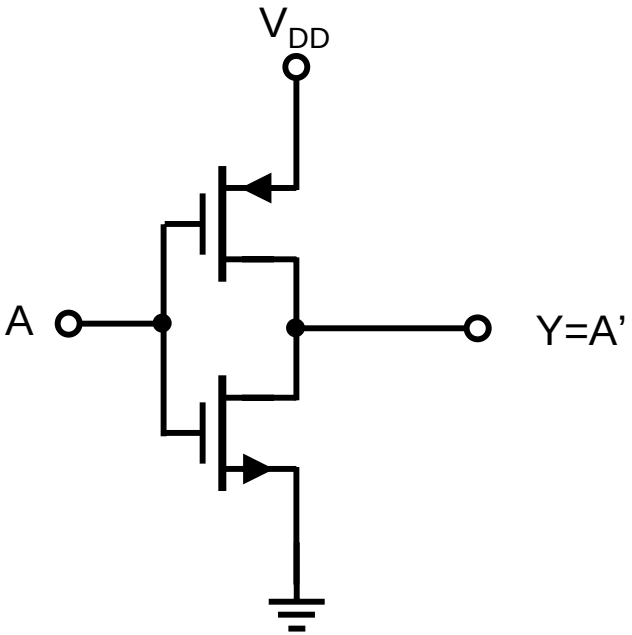
MOS



MOS vs. CMOS

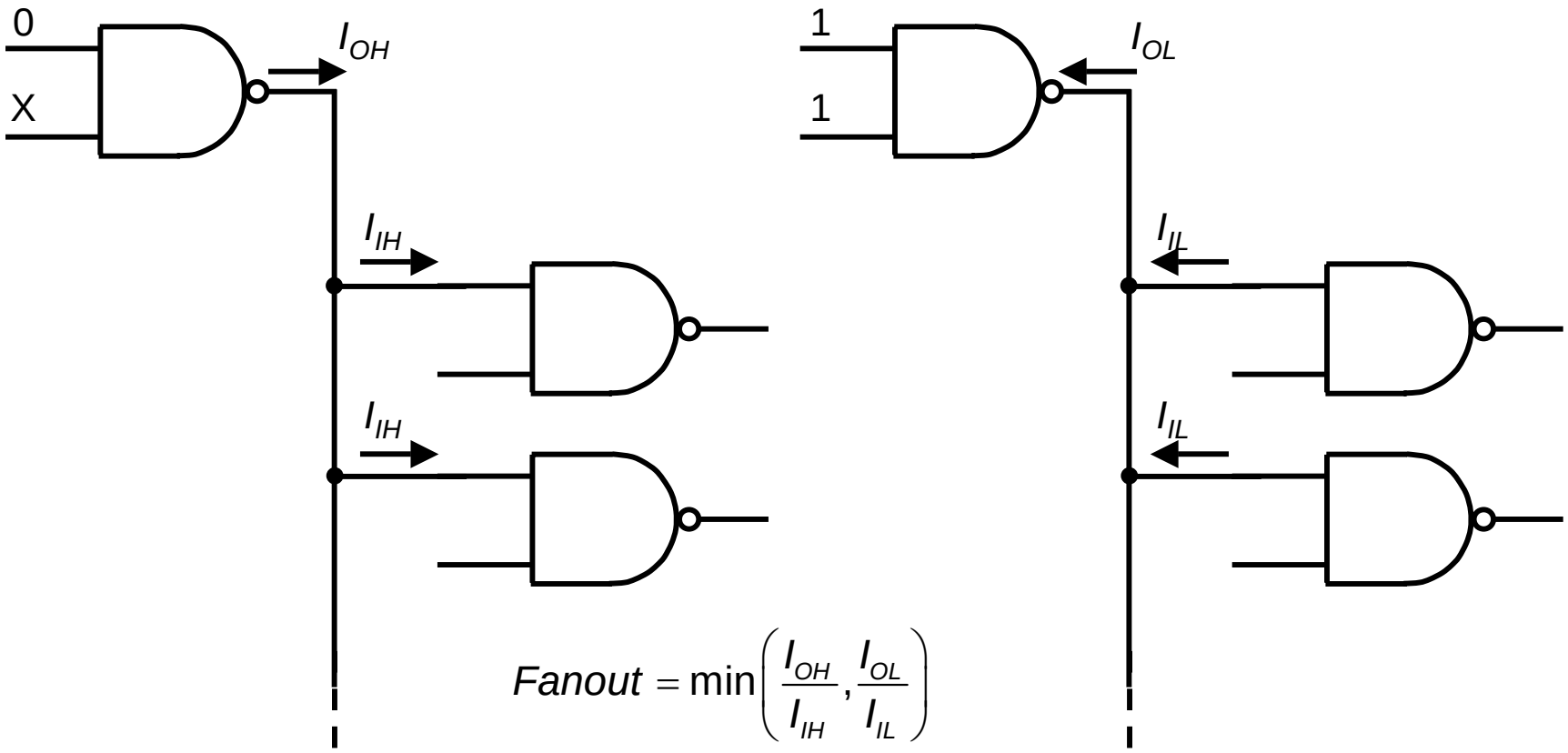
- MOS upper transistor is analogous to RTL logic resistor
- CMOS circuit is analogous to TTL totem pole
- CMOS draws essentially no power in static state
- Power is consumed when switching states $\rightarrow$ power consumption $\propto$ frequency





Fan-out

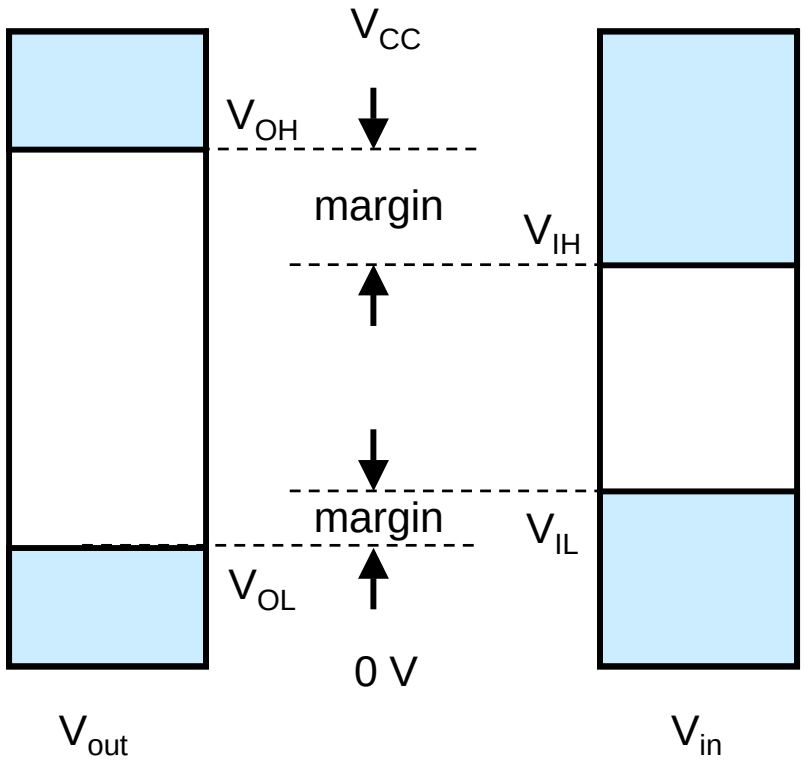
- Exceeding fanout degrades performance or prevents proper operation



$$Fanout = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$

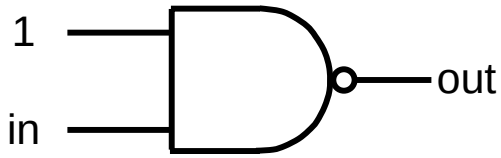
Noise Margin

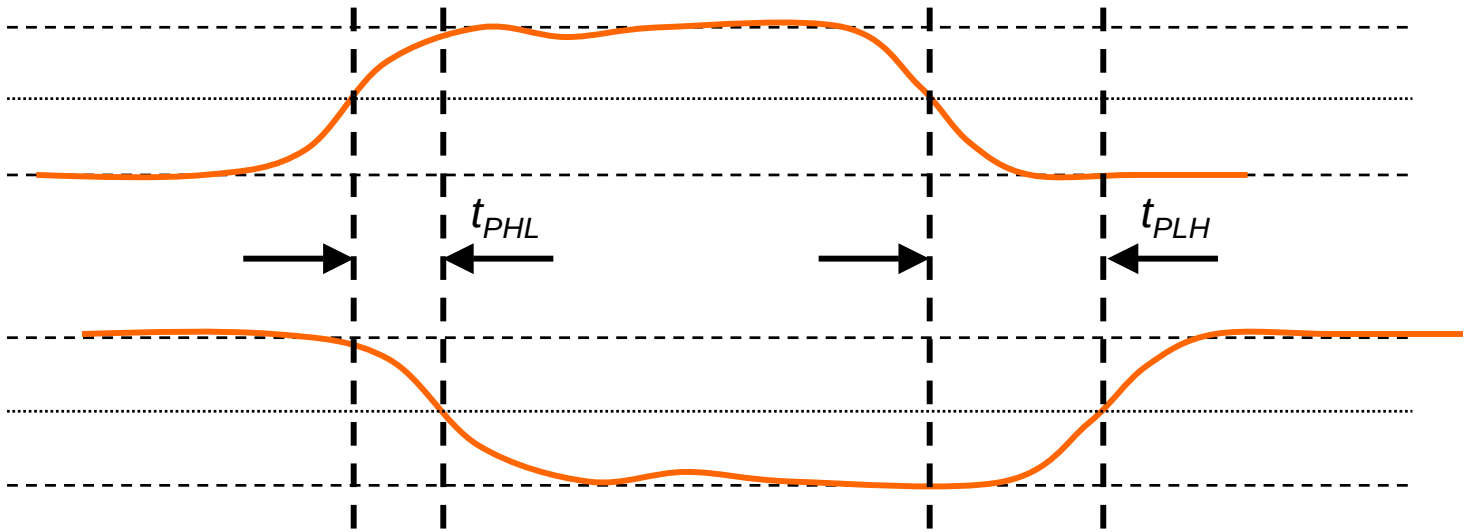
Worst case with
- loading
- power Δ
- temperature



Worst case tolerable input with
- power Δ
- temperature

Propagation delay

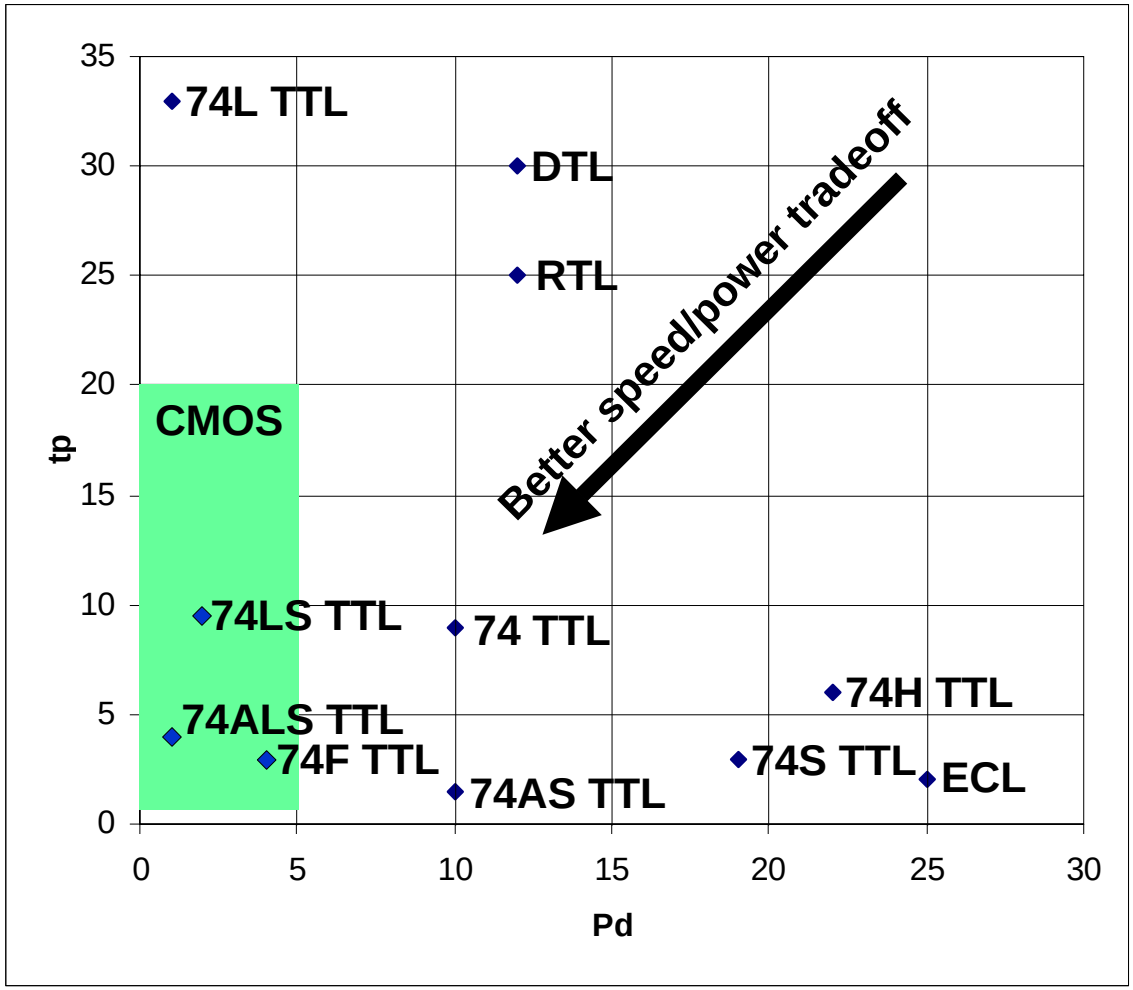




Comparison of Logic Families

Logic Family	Common designation	Fanout	P_d (mW)	t_p (ns)	Noise margin
RTL	-	5	12	25	0.4 V
DTL	-	8	12	30	1.0 V
TTL	74xx/54xx	10 UL	10	9	0.4 V
Low power (LP) TTL	74Lxx	20 UL	1	33	0.4 V
High Speed TTL	74Hxx	10 UL	22	6	0.4 V
Schottky TTL	74Sxx	10 UL	19	3	0.3 V
LP Schottky TTL	74LSxx	20 UL	2	9.5	0.4 V
Advanced Schottky TTL	74ASxx	40 UL	10	1.5	0.4 V
Advanced LP Schottky TTL	74ALSxx	20 UL	1	4	0.4 V
Fast TTL	74Fxx	20 UL	4	3	0.4 V
ECL		high	25	2	0.3 V
Conventional CMOS	4xxx	30@1MHz Less at higher frequency	.01@DC 1@1MHz 5@10MHz	5-20	40% Vdd
TTL pin compatible CMOS	74C				40% Vdd
High-speed TPC CMOS	74HC				40% Vdd
TTL compatible CMOS	74HCT	10 UL			>0.4 V

Logic Family Tradeoffs



Summary

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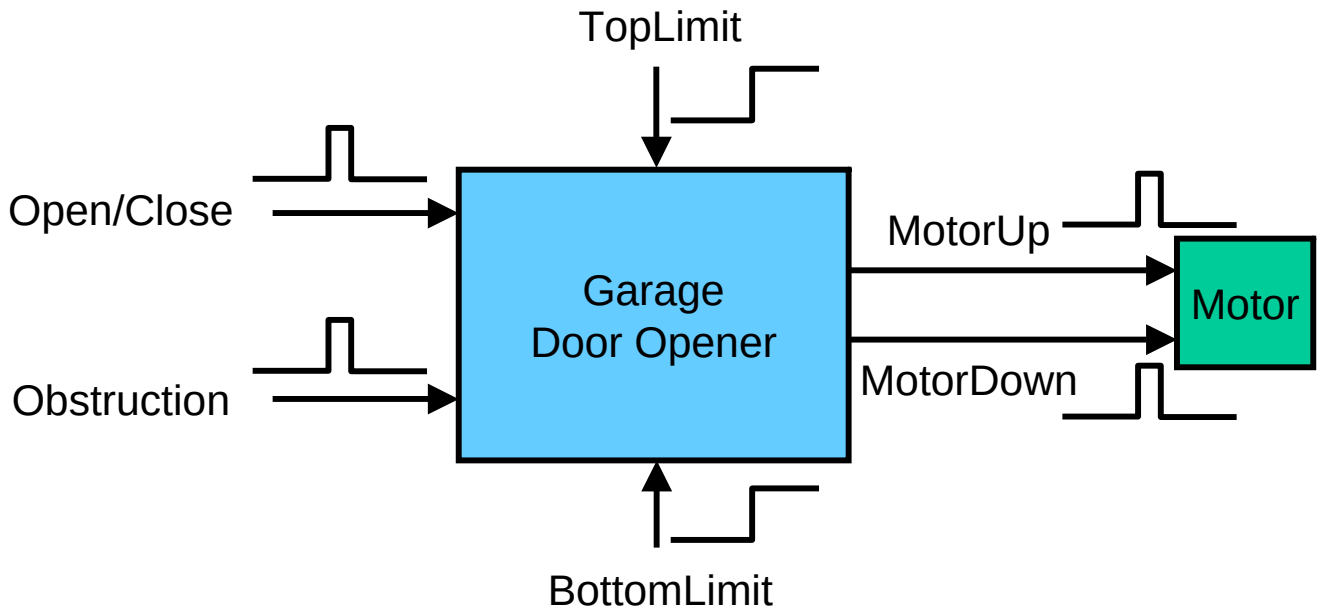
Design Projects

- Design projects are INDIVIDUAL EFFORTS.
- Projects are due during Class 15 (June 24)
- Several choices for projects will be described. Each has associated with it a "Level of Difficulty" Pick any N projects with a level of difficulty totaling at least 10 points. Grade(s) on project(s) will be multiplied by difficulty level and added to determine overall project grade. Any amount of extra credit is permitted.
- Design must include expression of Boolean functions designed and their minimization. Any methods used in the course are permitted. Extra credit will be given for multiple approaches. Show all work. Credit will be deducted for excessively complicated designs (where possible, provide an estimate the minimum required complexity for the design)
- Timing diagrams are required for all sequential designs. Make and state realistic assumptions about gate delays and other timing considerations (e.g., the frequency or period of clocks).

Design Projects

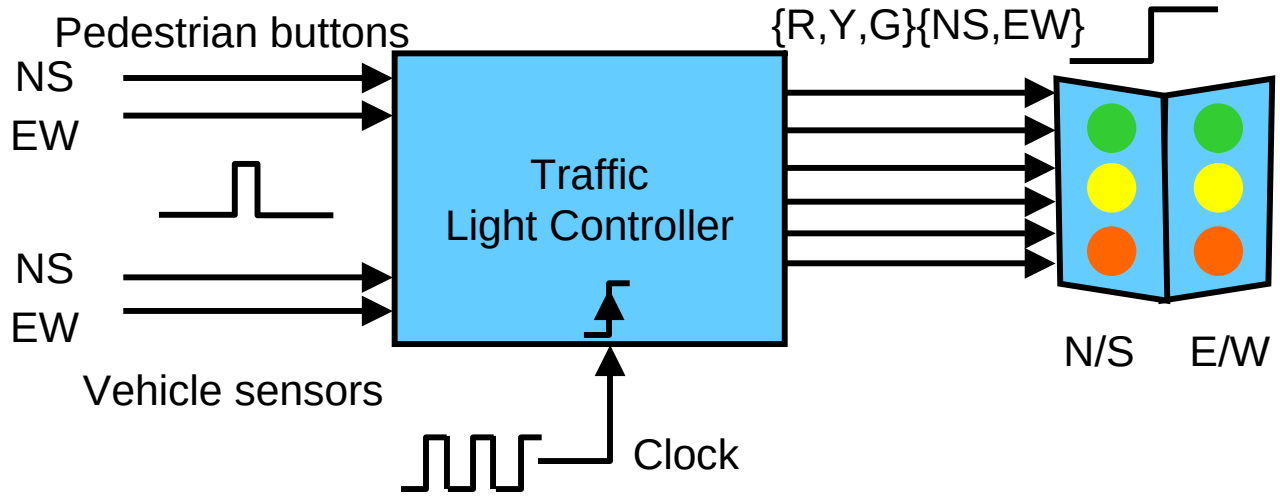
Pick any combination of design projects with Difficulty totaling at least 10:

1. Garage Door Opener (Difficulty = 3):
   - Output functions: Fmotorup(), Fmotordown() both functions of inputs: top_limit_sw, bottom_limit_sw, obstruction_sensor, open_close_button,timer.
   - Press open_close_button momentarily to move door. Door continues moving until either: timer expires, door reaches top limit, door reaches bottom limit, door encounters obstacle while moving down. Obstacle encountered while moving down causes door to open



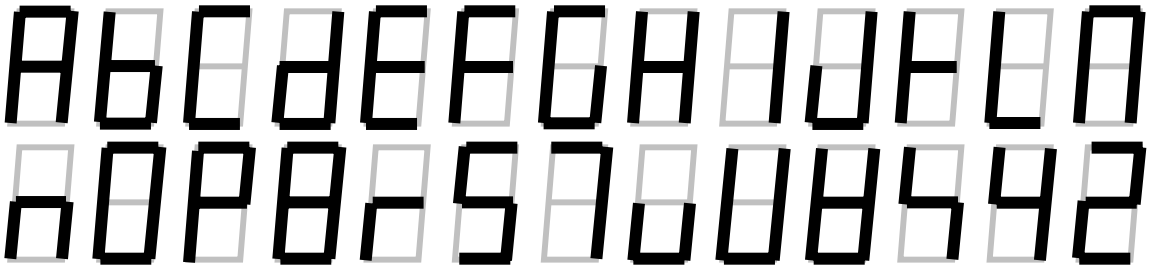
Design Projects

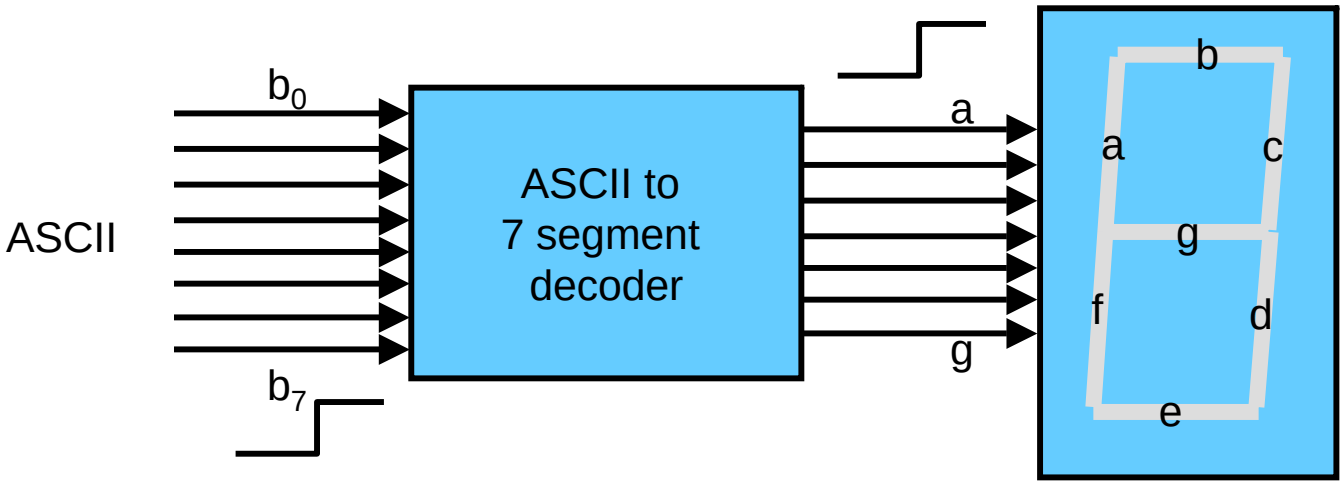
2. Traffic Light Controller (Difficulty = 5):
   - Output functions: Light_NS_Red(), Light_NS_Yellow(), Light_NS_Green(), Light_EW_Red(), Light_EW_Yellow(), Light_EW_Green(). All are functions of inputs EW_ped_button, NS_ped_button, NS_vehicle, EW_vehicle,clock.
   - With no pedestrian or traffic, light cycles Green 55 seconds, Yellow 5 seconds, Red 60 seconds. If EW pedestrian pushes button to cross, NS Green cycle is ends immediately. Ditto for NS pedestrian. If EW vehicle enters stop area during Red light, if there have been no NS vehicles in past 15-20 seconds, NS Green cycle ends immediately. Ditto for NS vehicle.
   - Extra credit (Difficulty = 2): Include green and yellow left turn arrow for NS traffic. Green arrow is 10 seconds at start of "green" interval for N traffic followed by Yellow arrow for 5 seconds. Green arrow is 10 seconds at end of "green" interval for S traffic, followed by 5 second yellow arrow.



Design Projects - Continued

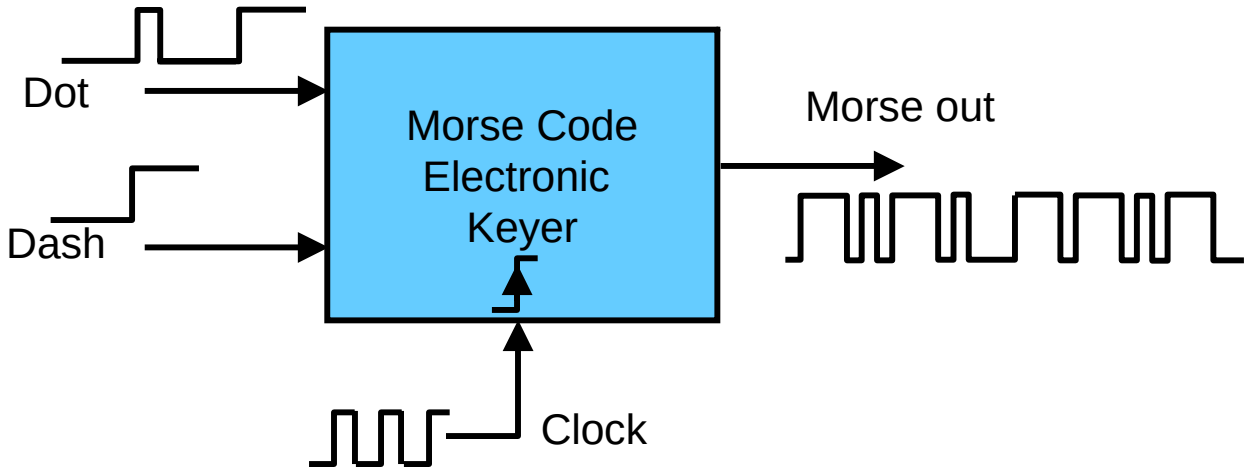
3. Seven Segment Alphabetic decoder (Difficulty=8).
   - Seven segment displays have been used for years to display the numerals from 0 to 9. The 7447 TTL device can decode BCD to a 7 segment.
   - Design a decoding circuit that has as its input ASCII characters and outputs signals to drive a seven segment display to represent the alphabet. Non-alphabetic characters can be ignored (Don't Care). You may design the circuit to respond to upper case only or upper and lower case, or both. The outputs for A-Z should look like:





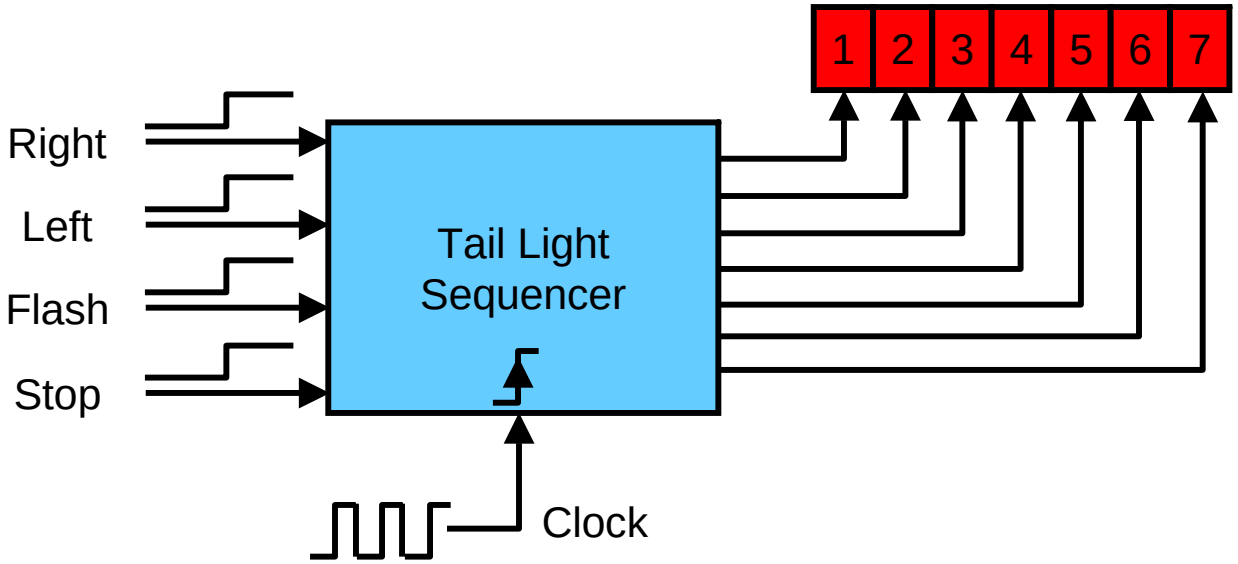
Design Projects - Continued

4. Morse Code Electronic Keyer (Difficulty = 10)
   - Two inputs: dot and dash, one output – normally 0, switches to 1 when output signal is asserted.
   - Morse code consists of two timed code elements: short signals (dots – length T) and long signals (dashes – length 3T). Letters and other code symbols are created by combining sequences of dots and dashes. Within a letter, the spacing between code elements is equal to the length of a dot.
   - An electronic keyer generates dots and dashes of precise length automatically. If the dot input is asserted, a sequence of dots (T on, T off) is output. If the dash input is asserted, a sequence of dashes is output (3T on, T off). If both inputs are asserted, an alternating sequence of dot-dash-dot-dash is sent (T on, T off, 3T on, T off,…). If dash is continually asserted and dot is momentarily asserted, a single dot is sent in the middle of the string of dashes. (The converse facility is extra credit)
   - The speed at which dots and dashes are generated is externally set by the user and may be assumed to be a constant. The initial transmission of dots and dashes may be assumed to occur at fixed times, corresponding to the beginning of a dot interval. Extra credit: the initial transmission may start at a time instant that is a fraction of a dot interval, but the duration of code elements must be retained.



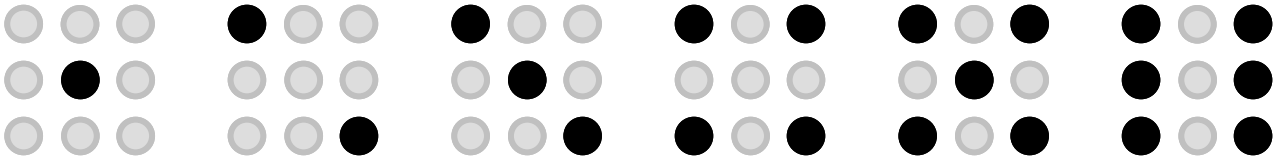
Design Projects - Continued

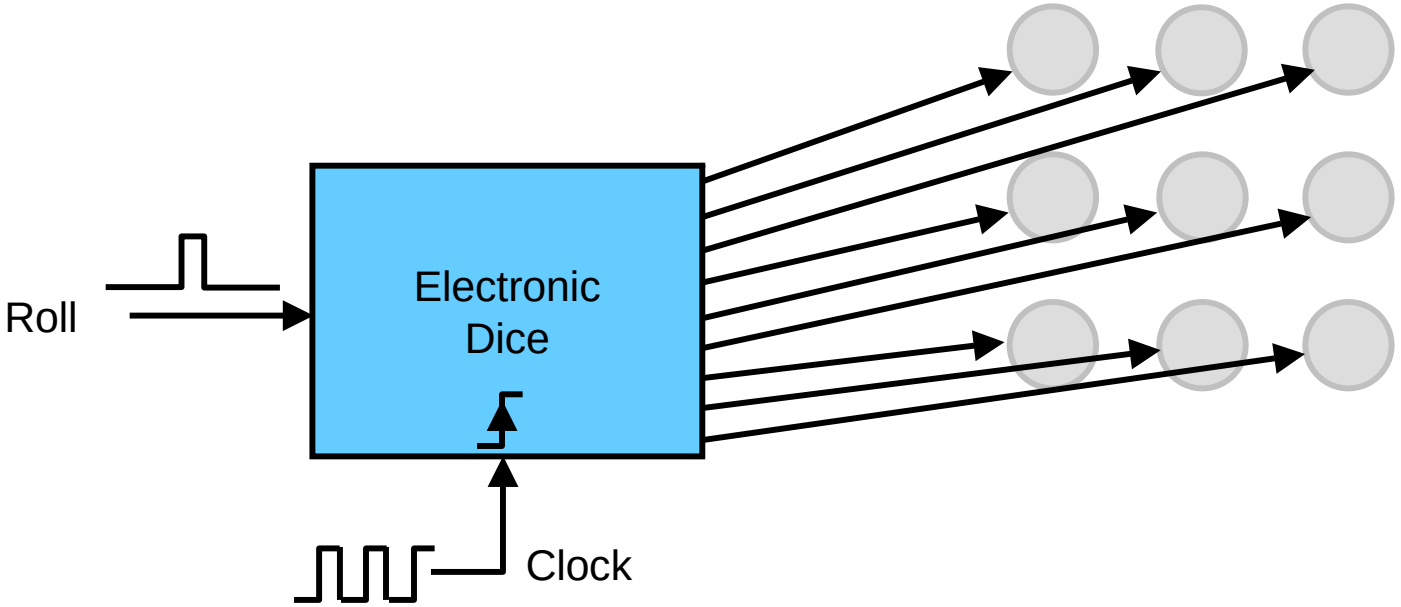
5. Tail Light Sequencer (Difficulty = 6)
   - There are five inputs to the tail light sequencer: Clock, Right, Left, Stop, and Flasher.
   - The tail light sequencer has 7 outputs, corresponding to seven lights across the back of a car, numbered 1-7 from left to right.
   - If the Right input is asserted, the three right lights (5,6, and 7) flash at the rate of 3/second, first 5 for 1/3rd second, then 6, then 7, then 5 again. If the Left input is asserted, Lights 3, 2, and 1 similarly flash. If Flash is asserted, light 4, followed by lights 3 and 5, followed by 2 and 6, followed by 1 and 7 similarly flash. If Stop is asserted, all lights are turned on. If Stop and either Left or Right are asserted, all lights are turned on, but either lights 1,2,3 or 5,6,7 blink out for 1/3rd second each.



Design Projects - Continued

6. Electronic Dice (Difficulty=7)
   - 7 LEDs flash in a seemingly random fashion (20/second) until user presses a button. Flashing stops within 1 second and LEDs display a pattern representing the 6 possible die faces. Probability of any outcome is equally likely.





Homework 4 – due in Class 6

As always, show all work:

- Problems 10-6, 10-11