AN4840

Gate Triggering And Gate Characteristics

Application Note

Replaces September 2000 version, AN4840-3.0

AN4840-3.1 July 2002

In all thyristor datasheets a set of curves showing device gate characteristics is given. This gives information fundamental to the correct triggering of the thyristor but the right interpretation sometimes causes problems. Note, the curves should be used in conjunction with the table of ratings and trigger characteristics given elsewhere in each data sheet. This table gives the relevant test conditions.

In this application note two types of gate curve are shown for DCR1596SW (Fig. 1a to c). Fig 1(a) shows the traditional format with logarithmic 'X' and 'Y' axes. This version allows a wide range of gate current and voltage to be shown. Fig 1(b) and 1(c) show curves with linear axes (2 graphs are needed to be the equivalent of Fig 1(a)). When gate drive load lines are to be superimposed linear versions are much more user friendly - see below.

INFORMATION PROVIDED BY CURVES

I_{GT} and V_{GT}

The value of gate current, I_G and voltage, V_G to be supplied to the thyristor to guarantee simple triggering should always be greater than the appropriate data book values of I_{GT} and V_{GT}. Simple triggering is adequate for low di/dt applications only - see below.

Note, that although the device may trigger at I_G and V_G values below the I_{GT} and V_{GT} values shown, no guarantee can be given.

I_{GD} and V_{GD} are the values of I_G and V_G below which the thyristor can be guaranteed NOT to fire. This is important for guarding against spurious triggering. Because it is very dependent on applied anode - cathode voltage and junction temperature I_{GD} is not provided as standard information in datasheets. However, test information can be provided by the factory in many cases.

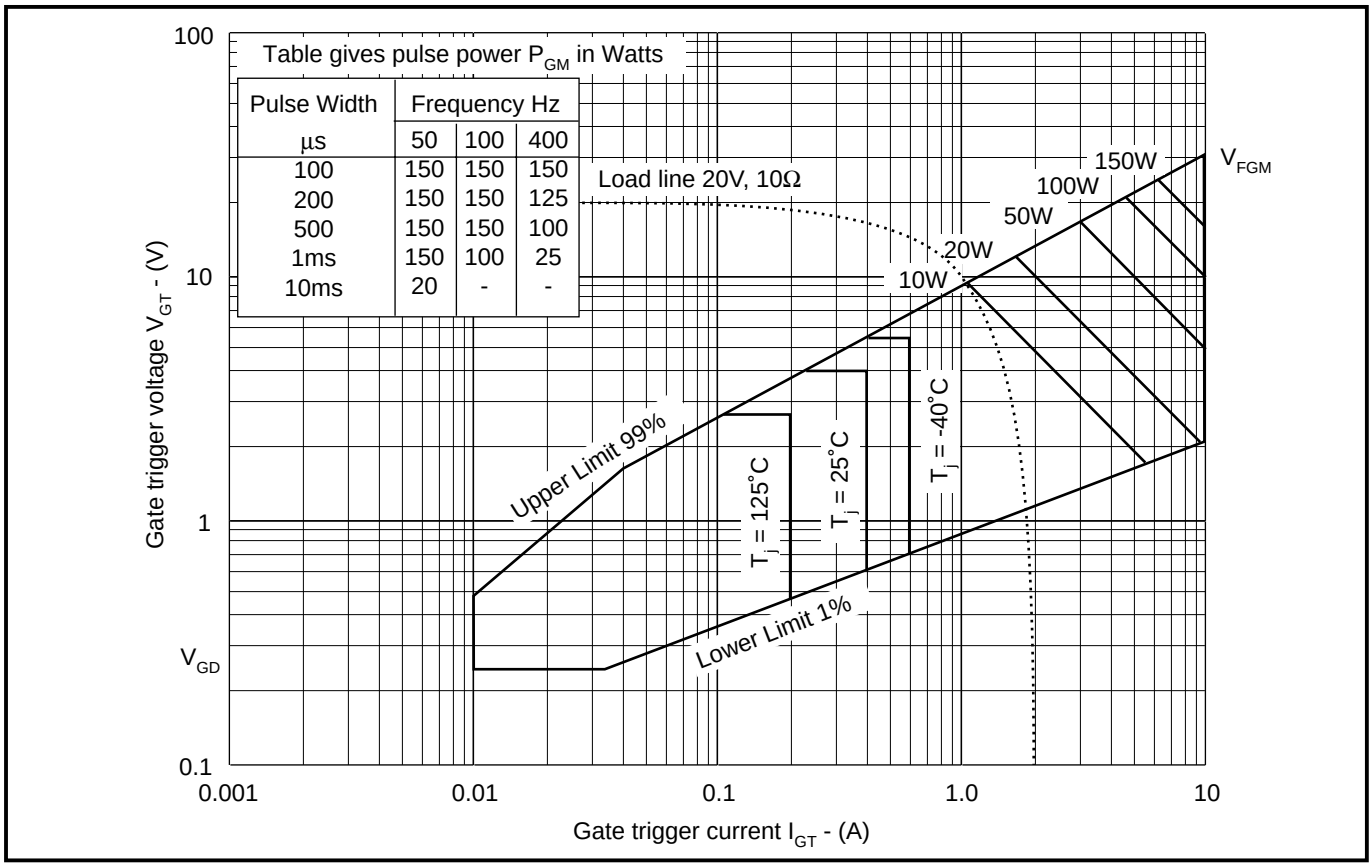

Fig.1a

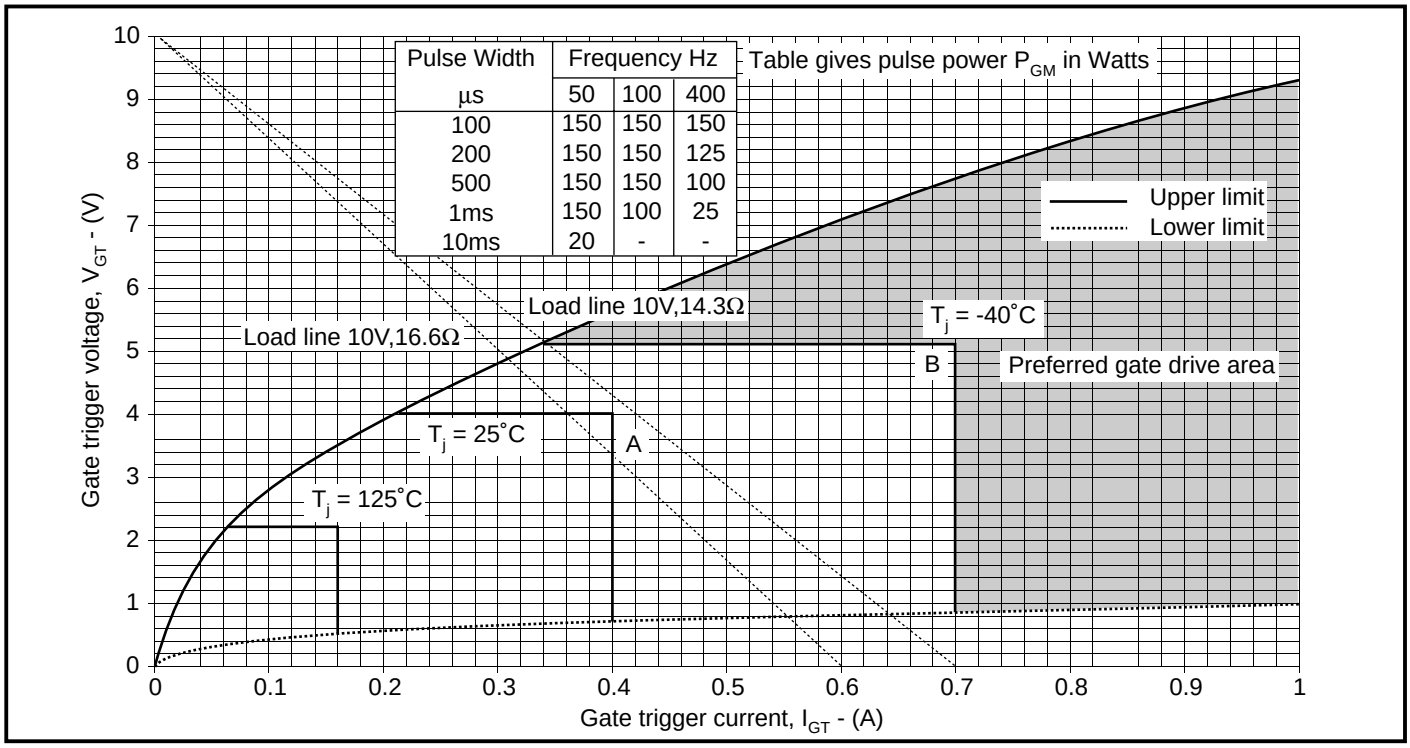
Pulse Width
Frequency Hz
µs
50
100
400
100
150
150
150
200
150
150
125
500
150
150
100
1ms
150
100
25
10ms
20
-
-
Table gives pulse power P_{GM} in Watts
Upper limit
Lower limit
Load line 10V,14.3Ω
Load line 10V,16.6Ω
T_j = -40˚C
B
Preferred gate drive area
T_j = 25˚C
A
T_j = 125˚C
Gate trigger voltage, V_{GT} - (V)
Gate trigger current, I_{GT} - (A)

Fig.1b

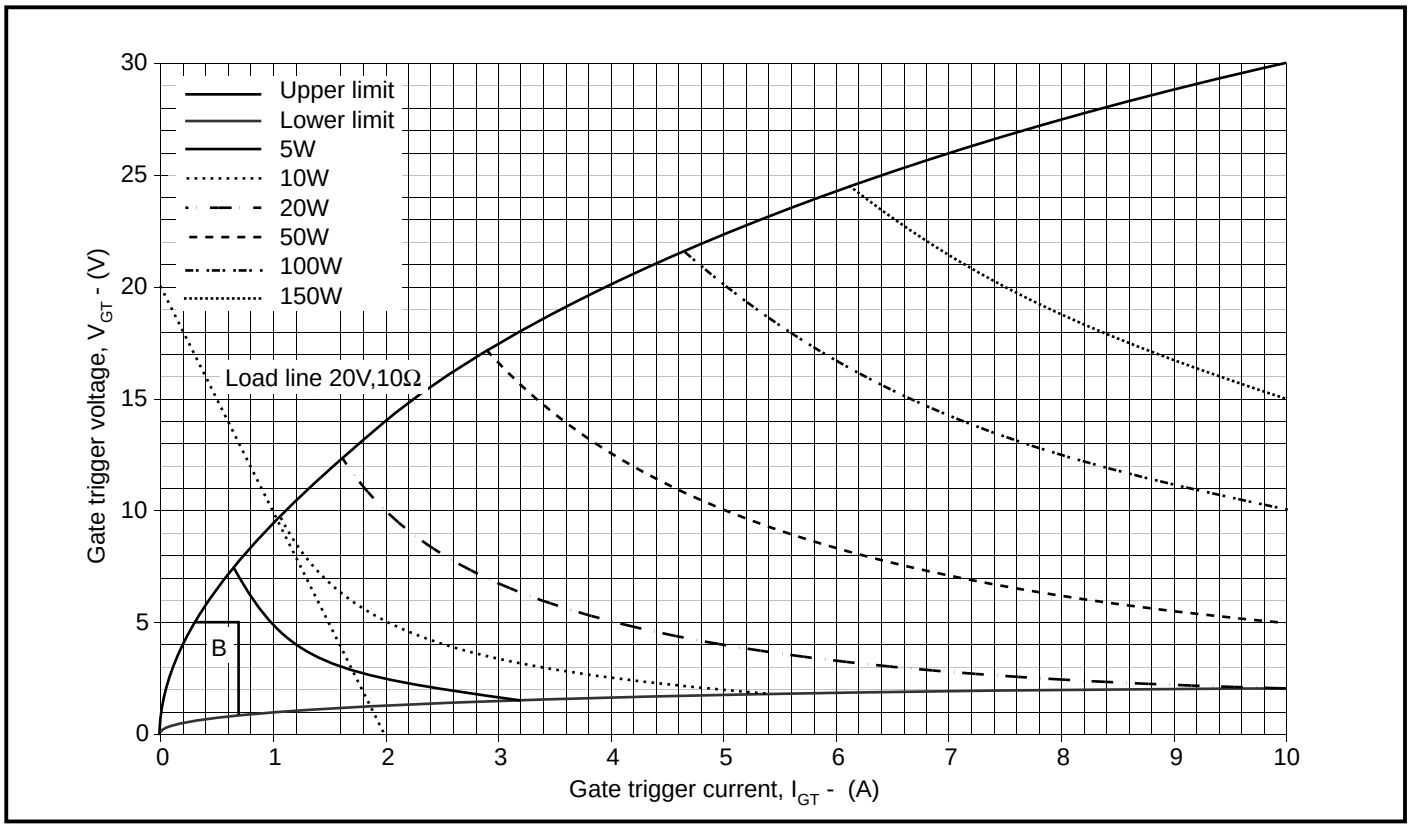
Upper limit
Lower limit
5W
10W
20W
50W
100W
150W
Load line 20V,10Ω
B
Gate trigger voltage, V_{GT} - (V)
Gate trigger current, I_{GT} - (A)

Fig.1c

GATE CHARACTERISTIC

This characteristic is that of the forward biased gate-to-cathode junction, together with associated on-chip series and parallel resistors, e.g. gate-to-emitter shorts. The graph shows the upper limit i.e. highest impedance and lower limit i.e. lowest impedance for all thyristors of that type likely to be manufactured.

The limits take into account the temperature range –40 to +125˚C. All devices will have characteristics between these limits.

Gate characteristic information is used in conjunction with firing circuit output load lines to pre-determine operating values of gate current and voltage - see below.

GATE RATING LIMITS

Thyristors turn on best when Ig and Vg values are well above I_{GT} and V_{GT} limits - see below. However, peak gate current, gate voltage and power rating limits should not be exceeded.

V_{FGM} - PEAK FORWARD GATE VOLTAGE

If the open circuit voltage of the firing circuit exceeds this rating (usually 30 volts) there is a danger of internal voltage breakdown. In practice, 50 or more volts can often be achieved but is not guaranteed since some internal device constructions are limited.

I_{FGM} - PEAK FORWARD GATE CURRENT

This rating is determined by the current carrying capability of internal gate leads, bonds and surface metallisation of the thyristor.

Note that the 'X' axis of the graph is limited to 10 amps so that the Ifgm limit of large thyristors is not shown.

P_{GM} - PEAK GATE POWER

The average heating effect of the gate current is the issue here. Thus, a narrow pulse of high P_{GM} is as permissible as a wide pulse of low P_{GM}. Included on the graph is a table showing maximum permitted peak gate power for various pulse widths and repetition rates. Also on the graph are lines of constant power. These lines are the power limits corresponding to the pulse powers given in the table and are used in conjunction with gate drive load lines.

MATCHING THE GATE DRIVE/FIRING CIRCUIT TO THE THYRISTOR TRIGGERING REQUIREMENTS

The basic approach is to draw the output load line of the firing circuit onto the gate characteristic curve. It is usually assumed that the gate drive has a purely resistive linear characterisation - fig 2. The characteristic is defined by its open circuit source voltage V_{OC} and its short circuit current I_{SC}. The straight line between these 2 points represents the internal source resistance

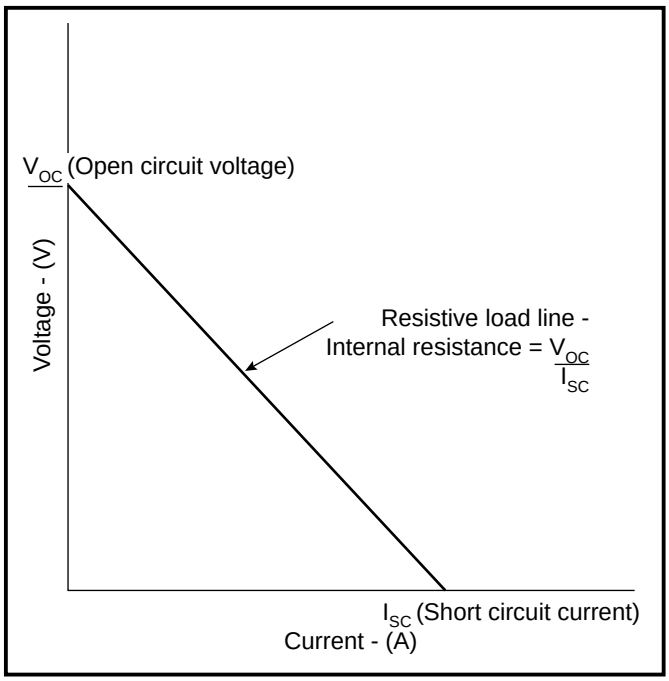

Fig.2 Output load line for gate drive

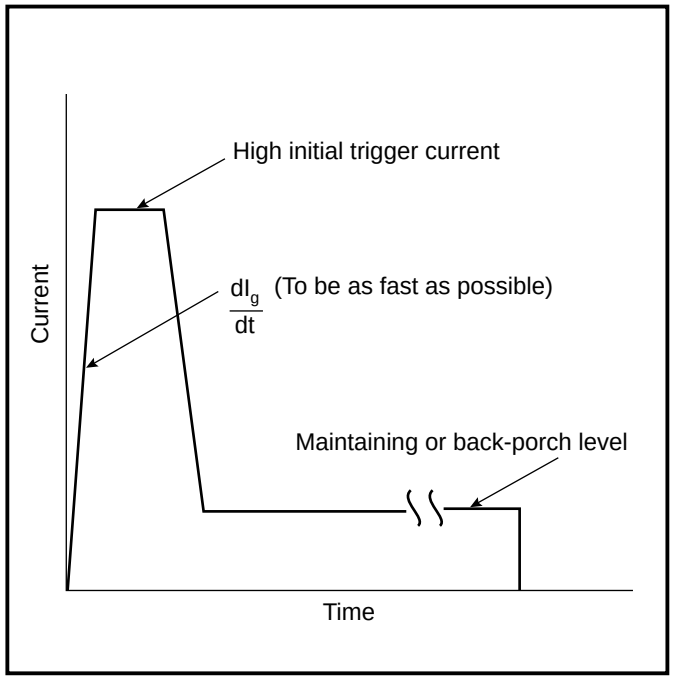

Fig.2 Output load line for gate drive

of the gate drive. Gate drive output is often defined in terms of its open circuit voltage and internal source resistance.

To select the correct gate drive load line it is useful to draw several possibilities onto the characteristic curve (fig 1). Compare the 20V, 10Ω line drawn onto the logarithmic and linear axis versions. Clearly, the linear version is much easier to work with.

The first requirement for the load line is that it must pass through the 'preferred gate drive area' to the right of the appropriate I_{GT}, V_{GT} limit point. For operation down to -40˚C, this is point B. For +25˚C minimum operation temperature, point A applies. Load line 10V, 14.3Ω is adequate for 25˚C operation but load line 10V, 16.6Ω is not since it crosses the 25˚C 'zone of uncertain triggering'.

Unfortunately, most applications demand gate drive levels well above the minimum, with good di/dt performance being the most demanding. For DCR1596 a 20V, 10Ω load line is preferred. This load line lies well to the right of Point B. Note also that 10 watts peak power is not exceeded.

MORE ON I_{GT}, V_{gGT}, GATE PULSE WIDTHS AND RECOMMENDED GATE DRIVE

Two basic circuit connections should be considered.

1) Using single thyristor elements.

2) Using series and parallel combinations.

First consider single thyristor elements.

Low values of triggering I_G and V_G are satisfactory for simple resistive loads with minimal overload currents and low di/dt. In this near-ideal situation a simple pulse of 10µS or less would suffice, with Ig only slightly more than I_{GT}.

In practice, this situation is unrealistic and an appropriate gate pulse shape must be chosen to match the application. Fig. 3 shows the general shape for a single gate pulse. It consists of an initial short, fast rising high amplitude section followed by a longer, low amplitude "back-porch" section.

The back-porch section has to be long enough to allow an inductive load anode current to rise to the device latching current.

In most applications a CR snubber network is connected across the thyristor. Because of the high di/dt of the snubber discharge current on thyristor triggering the initial gate pulse should be of high amplitude and rate of rise. Where the load itself is capacitive, or very low inductance, circuit di/dt levels are even higher and hard gate drives are needed. For example, the gate drive recommendation for DCR1596 to achieve its di/dt ratings of 300A/µs is 20 volt, 10 ohms, with current rise time less than 0.5µs. High gate drive is only necessary for the duration of the turn-on period - a few microseconds. After that the gate amplitude may be allowed to fall to a low maintaining value, i.e. the back-porch current.

The function of the back-porch current is to allow the thyristor to be retriggered if the anode current transiently dips below the holding current value. However, it is quite common for the gate signal to be needed for several milliseconds after initial triggering. This is done by providing a train of pulses for the duration of the triggering period since a single long pulse would require too much power from the gate drive.

SERIES AND PARALLEL COMBINATIONS

All the above remarks relating to triggering of single thyristors apply equally to series and parallel combinations. An additional requirement is to ensure that all thyristors in the combination turn on as nearly together as is possible. This is done by reducing the D t_{GD} value, i.e. the difference between individual device delay times. For this, a hard gate drive is also required.

GATE DRIVE RECOMMENDATIONS

From the above it is clear that a hard gate drive (high current, high voltage, fast rise time) is needed for the majority of applications. A low power gate drive is likely to cause triggering problems. The basic pulse should have a high current front end and low current back-porch. In some situations a train of these pulses may be needed.

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http://www.dynexsemi.com

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD
Doddington Road, Lincoln.
Lincolnshire. LN6 3LF. United Kingdom.
Tel: +44-(0)1522-500500
Fax: +44-(0)1522-500550

CUSTOMER SERVICE
Tel: +44 (0)1522 502753 / 502901. Fax: +44 (0)1522 500020

SALES OFFICES
Benelux, Italy & Switzerland: Tel: +33 (0)1 64 66 42 17. Fax: +33 (0)1 64 66 42 19.
France: Tel: +33 (0)2 47 55 75 52. Fax: +33 (0)2 47 55 75 59.
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North America: Tel: (613) 723-7035. Fax: (613) 723-1518. Toll Free: 1.888.33.DYNEX (39639) /
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