

# **DVI Test and Measurement Guide**

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By DDWG Electrical Test Working Group

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## Overview

The test and measurement guidelines contained in this document are developed in order to aid the deployment of the DVI specification into computer to display communication and support more rapid adoption of the DVI interface. The DVI specification, released in 1999, has been widely implemented by a number of computer OEM's, monitor makers, graphics board vendors, and cable manufacturers. Multiple silicon implementations will soon be available on the market. As evidence of the standardization around the DVI interface, the PC 2001 Design Guide has a requirement that states host systems, which output digital graphics data, must be DVI compliant.

The intent of this document is to provide users of DVI with the necessary knowledge to enable validation of their DVI implementations and ensure compliance with the DVI electrical specifications. It is an elaboration on the requirements and test procedures described in the original specification, and describes specific test hardware and recommended measurement equipment and techniques that should be used. As DVI hardware from multiple vendors becomes more widespread and configurations where hardware from more than one silicon vendor is required to interface with each other, the ability to guarantee compliance with the specification is paramount. Further, due to the high speed signaling supported by the DVI standard, design issues such as board layout, routing and other system parameters can affect the integrity of the DVI transmission link. This test and measurement guide thus focuses on the system level implementation testing, so that all of these factors are considered in the compliance testing.

Intended users of this document include the same customer base implementing DVI today – computer OEM's, monitor and panel makers, and graphics system vendors, as well as cable and connector manufacturers. The test and measurement guide enables independent testing of the transmitter system, the cable used between the transmitter and receiver systems, and the receiver system. This will allow system manufacturers who focus on just one piece of the communication link to separately test their parts, but will also allow complete system implementers the capability of diagnosing potential problems by checking each segment of the link independently.

The document describes first the DVI link and system test points as well as the testing hardware. Subsequent sections describe independent testing of the transmitter, cable and receiver portions of the link. These procedures are briefly described below.

### DVI Transmitter Testing Overview:

For testing the transmitter system, hardware is described which allows a straightforward way of measuring the eye diagram of the TMDS output, using a reference clock that has the same characteristics of the receiver PLL that latches the TMDS input. This ensures that the eye diagram is measured as the receiver would see it – use of other clocks can add noise to the measurement and lead to the conclusion that a transmitter is showing degraded performance. To accomplish this measurement, a specific test board that makes the TMDS data signals readily accessible and a clock recovery unit to provide the reference clock are described. Since the transmitter measurements are of the transmitter system, this technique is equally applicable to discrete transmitter components or to graphics controllers that integrate TMDS output.

Necessary equipment:

- DVI transmitter system with DVI output receptacle:
- TPA-P board
- Digital Oscilloscope (see Section 3 for recommended models)

### DVI Cable Testing Overview:

Testing the cable requires measuring a known eye diagram that can be input to the cable and then measuring the eye at the end of the cable. While to a first order, this can be approximated by measuring a transmitter eye as described above, and then measuring the eye again with a cable is connected, this does not allow sufficient control over shaping the eye diagram. In order to support cable testing, as well as

receiver testing as described below, an equivalent source board is described. Such a board will allow flexibility in shaping the eye, including generation of the minimum acceptable eye that can be output from a transmitter, as well as adding various amounts of jitter and skew to the TMDS transmission. Cable measurements should ideally be done with both minimum signal levels, which stress the attenuation performance of the cable, as well as maximum signal levels, which stress the crosstalk performance of the cable. Finally, since the complexity of eye diagram measurements, and the availability of the transmitter and receiver hardware necessary to perform these tests is not generally familiar to cable manufacturers, another approach to cable qualification is described. While not as rigorous as the eye measurements described above, and in more detail in Section 5, the alternative metrics described are more familiar tests to cable manufacturers and acceptable levels for these parameters are defined based on experience with the more rigorous eye diagram measurements.

Necessary Equipment (for eye measurement characterization):

- DVI Equivalent Source Board
- TPA-P Board
- TPA-R Board
- Digital Oscilloscope

### **DVI Receiver Testing Overview:**

Finally, testing the receiver system requires a slightly different approach than measuring the eye diagram. The receiver specification is defined by demonstrating decoding of TMDS data with a minimum number of pixel errors even when receiving a worst-case eye diagram. In order to validate this requirement, control of the input eye diagram is required, which as noted, is accomplished by the equivalent source board. The second piece of hardware required is a receiver test board, which can check the output of the receiver system under test against the expected data in order to determine the number of pixel errors. This testing system will require the transmission of specific patterns, as described in chapter 6. A less rigorous, but more practical initial test is described which consists of monitoring the output to a display looking for pixel errors. While this is not a guarantee of receiver performance to a specific pixel error rate, it is generally the primary indicator of problems with the link, and could be used as a more qualitative performance indicator that might indicate the need for more rigorous testing if problems are observed. Once again, since the receiver test looks at the system implementation, including the signal layout, power supply performance, etc... the receiver test is equally applicable to systems with discrete TMDS receivers or receivers integrated into other image processing chips.

Necessary equipment:

- DVI Equivalent Source Board
- DVI Cable Assembly
- TPA-R Board
- Pixel Error Rate Test Board (Method 1) or
- Display (method 2)
- Digital Oscilloscope
- TDR Scope (see section 3 for recommended models)

With the release of this test and measurement guide, we are requesting feedback from the user community on the test procedures described within. The specific hardware described in this document is under development and reference design documents sufficient to allow production of this hardware will be made available by the DDWG once the designs are validated. At this time, the TPA-P and TPA-R boards are available, while the equivalent source boards (ESB) and Pixel Error Rate Test board are in development and some additional modifications will be made before they are made available.

It should also be noted that this first version of the test and measurement guide does not cover all DVI applications – specifically, the additional characteristics of dual link and HDCP implementations are not covered at this time. Furthermore, while the DVI connections allow analog signal transmission via DVI-I connectors and cabling, testing of analog signal quality is not described.

# 1 Introduction

## Context

This document provides measurement guidelines for the evaluation of DVI components against the DVI specification. The components that are tested are those elements of the link bounded by test points TP2 and TP3' as defined in the DVI specification (Figure 1-1).

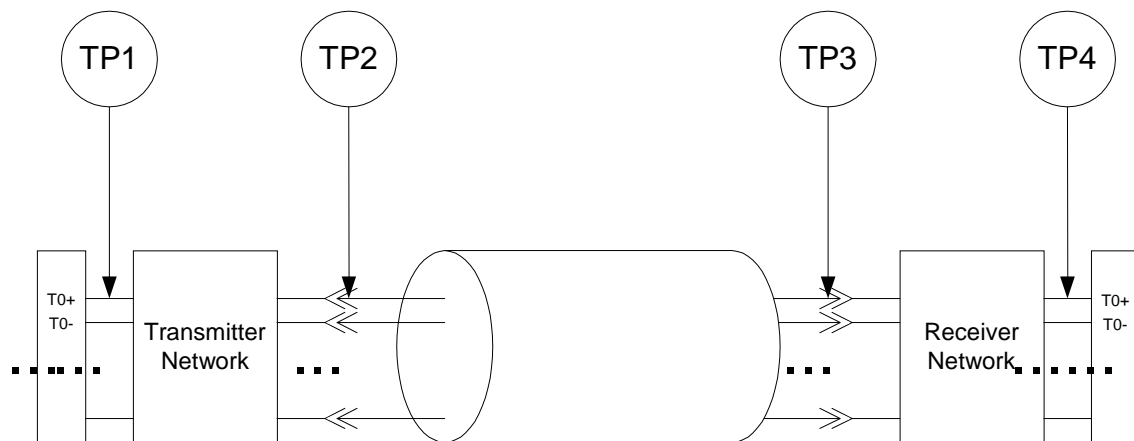


Figure 1-1 T.M.D.S. Test Points

These test points are defined to be at the contact point between the mated connector pairs of the cable assembly. In practice, test point access will require a mated connector to be present to give access to the test point. The recommended test procedures always err toward understating system performance by moving test points to one side or the other of the mated connector pair based on which element is under test and which test is being performed. With unidirectional transmission, the effective test point will normally be to the downstream (to the right on the figure) side of the connector pair. The exception is the receiver impedance measurement, which views a reflected waveform and as such moves TP3 to the cable assembly side of the connector. All measurements include the effects of an additional mated connector pair.

The elements to be tested are thus the transmitter, cable assembly, and receiver. The transmitter includes the transmitter component, connector, and interconnecting circuit board network. The receiver similarly includes the receiver component, connector, and interconnecting network. Hence in this document it is noted that the transmitter and the receiver mean subsystems of the T.M.D.S. link not components. This document includes recommendations for test fixtures, test equipment, and test methods for the evaluation of these elements.

## Test Philosophy

Although skew, rise time, and jitter test procedures are described, the critical measure of DVI component operation is the eye pattern. For the transmitter, it is the eye pattern when driving a test load across all operating conditions. For the cable assembly it is the degradation of the eye pattern. For the receiver it is the response to degraded eye patterns. The eye pattern masks of the DVI specification are essential for the testing of link components.

For the eye pattern and jitter measurement to be able to guarantee the  $10^{-9}$  pixel error rate, more than one billion acquisitions are required. But this takes too long to be practical and the statistical inference method is applied (in this document this method is called **Method I**) to reduce the number of acquisitions to a reasonable number. However, oftentimes due to the systematic jitter and/or noise in the system the

distribution is not quite random gaussian, and hence it is very difficult to infer the correct amount of signal degradation. Also in the visual application when the pixel noise is random and the pixel error rate is smaller than  $10^{-6}$ , it is almost impossible to detect any pixel noise from display. Hence in practice the eye pattern and jitter data can be collected based on a less rigorous but much more practical way (in this document this method is called **Method II**). In each of those sections the two different methods (a mathematically rigorous but impractical one and a less rigorous but much more practical one) will be presented for jitter and eye pattern measurement.

Transmitter tests are relatively simple, but cable assembly and receivers are more difficult because they require a source for maximally degraded eyes, or worst-case eyes. The complexity of this testing is unavoidable for manufacturers of receivers, however this is not the only complexity which the receiver manufacturer must deal with and this guide does not attempt to provide any relief. For cable assembly manufacturers, however, for who this type of testing may not be familiar, alternative test procedures have been defined. These tests use familiar performance metrics and are described in Section 5.4.

## 2 Test Fixtures

The test fixturing described in this section should be constructed using good known practice. The test point access boards provide access to most necessary test points through SMA connectors with minimal signal degradation. Two variations for the TPA board are required, one with a DVI receptacle (TPA-R) and one with a DVI plug connector (TPA-P). The boards are otherwise identical.

Because the test setups in some cases will be done with the plug version and measurements made on the receptacle version, it is important that these fixtures be closely matched in electrical characteristics for a given set of measurements. This can be accomplished through the use of the fixturing described below.

### 2.1 Receptacle differential Test Fixture (TPA-R)

The receptacle test fixture is used for cable assembly and receiver tests. The receptacle footprint is placed on an FR4 substrate layer using guarded microstrip construction and porting to test equipment using SMA connectors. Depending on the probes used for the differential data measurements, short stubs may need to be soldered to the active and ground points for the signals to be measured. Use of the vertical receptacle connector on this board is recommended, in order to minimize fixture effects on the test system. For transmitter testing the termination value must be set to 45 ohms (-10%) and 55 ohms (+10%). Each of the TPA boards also has a receptacle where an EDID PROM may be inserted. This will allow a valid EDID to be read if required by the graphics controller.

Because the differential data lines are not connected to the clock recovery unit, some transmitters may not detect the receiver as active, and may shut down the digital output. If a driver is not available to maintain the digital port as active, reworking the board to connect the differential inputs to the clock recover unit may be required, but will degrade the signal measured. The TPA-R board will require an external power supply for operation.

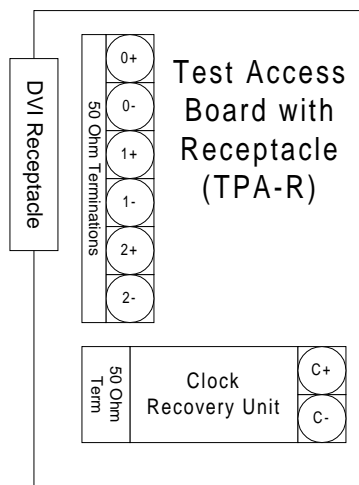


Figure 2.1 Test Point Access Board, with receptacle

## 2.2 Plug differential test fixture (TPA-P)

The plug test fixture is used for cable assembly and transmitter tests. The plug footprint is placed on an FR4 substrate layer using the same construction as the TPA-R board, and ideally the two should be panelized in production to assure matched board characteristics between the two. For the plug fixture, a vertical mounted plug is used on the opposite side of the SMA connectors. This allows the TPA-P board to be plugged into a PC, for example, and still provide convenient access to the test points.

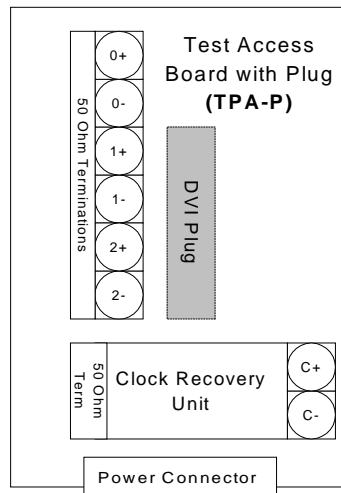


Figure 2-2: Test Point Access Board, with plug



## 2.3 Clock Recovery Unit

The clock reference that is transmitted on the T.M.D.S. link contains low-frequency jitter components that are tracked by the receiver phase-locked loop and high-frequency components, which are not tracked. The purpose of the clock recovery unit is to remove these high frequency jitter components, producing a clock that will give an accurate representation of link performance when used as a trigger for eye pattern measurements. The clock recovery unit may be any circuit, including a full T.M.D.S. receiver, provided that it meets the requirements of the DVI specification, Section 4.7.3, as illustrated in Figure 2-1 below.

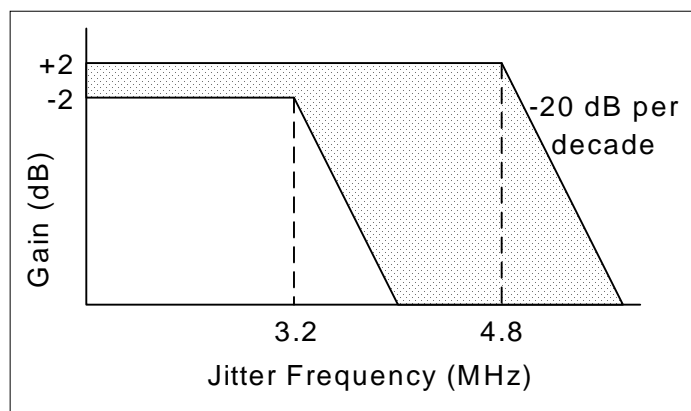


Figure 2-3 Clock Recovery Unit Frequency Response

The clock recovery unit output must be at the pixel clock frequency or higher, with filtering characteristics that fall within the shaded boundaries of Figure 2-3 across the entire operating clock frequency range. The gain of a clock recovery circuit should be measured using the test configuration shown in Figure 2-4. Gain should be recorded for the following discrete jitter frequencies driven by a waveform generator: 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.3, 3.6, 4.0, 4.4, 4.8, 5.2, 5.6, 6.0, 7, 8, 10, and 15 MHz. The test clock frequencies should include some or all of the following depending on the maximum allowed operating speed: 25MHz, 40MHz, 65MHz, 112MHz, and 165MHz.

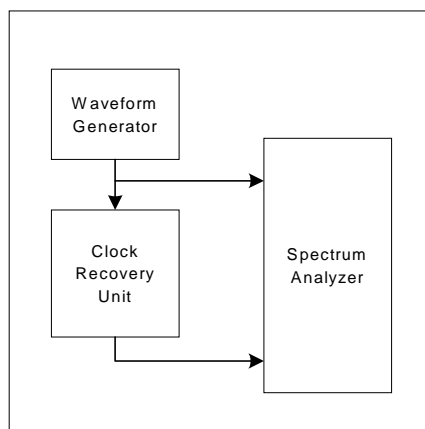


Figure 2-4 Clock Recovery Unit Test

## 2.4 Equivalent source test boards

This test board is necessary for cable assembly and receiver tests. Functionally, the board contains a test pattern generator, a clock source, which can add jitter of a controlled frequency and amplitude, a TMDS source, and a DVI receptacle for driving the cable assembly or receiver under test.

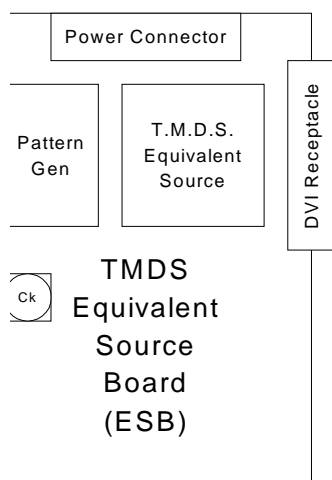


Figure 2-5 Equivalent Source Board

In practice, it is often simpler to provide an equivalent source board as a system of multiple boards, as shown below. In this configuration, the clock generation and power distribution are provided on one board, the pattern generation capability and user interface are provided on a second board, and the TMDS transmitter and adjustment capabilities on a third board. This allows reuse of the clock and pattern generation boards with multiple transmitter boards, which can be optimized for different tests.

The first board used is the clock generator. This board is used for the clock source board, and may be used to inject jitter into the clock of a controlled frequency and amplitude. Currently this board is designed to provide up to 2 MHz of jitter, although future iterations will allow up to 10 MHz of jitter, for a more comprehensive measurement.

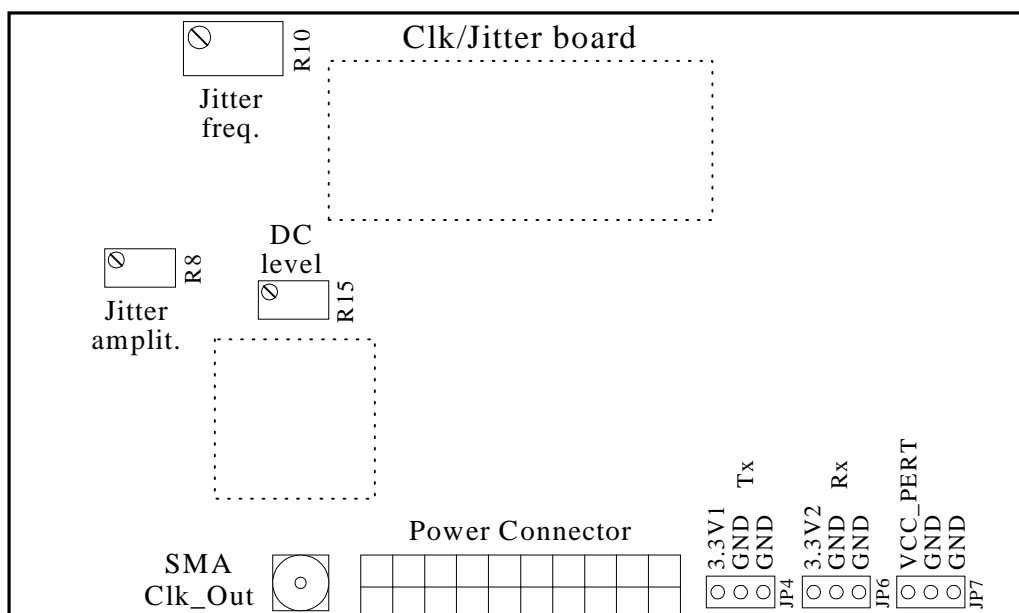


Figure 2-6, Jitter Clock Source Board

The second board contains a test pattern generator as well as an LCD module for a user interface to set test modes (pattern choices and durations) and view results (pixel error quantity). The pattern generator functions are described in more detail below. Pattern data may be output on a 12, 24, or 48 bit pixel bus, depending on the transmitter being used. The maximum clock speed for the pattern generation function is 85 MHz, so testing at 165 MHz will require either a 48 bit pixel input, or double data rate clocking of a 12 bit interface. As will be noted in the next section, it is convenient to also incorporate a pattern comparator function in this board to allow for quantitative pixel error rate measurements. Again, the pattern comparator is limited to 85 MHz operation, so for full speed testing of a DVI link at 165 MHz, 2 pixel per clock output mode must be used for the TMDS receiver operation. The pattern generator also supplies Hsync, Vsync, and DE signals according to VESA timing specifications. The board will operate in XGA or SXGA mode depending on the PROM loaded into the test board.

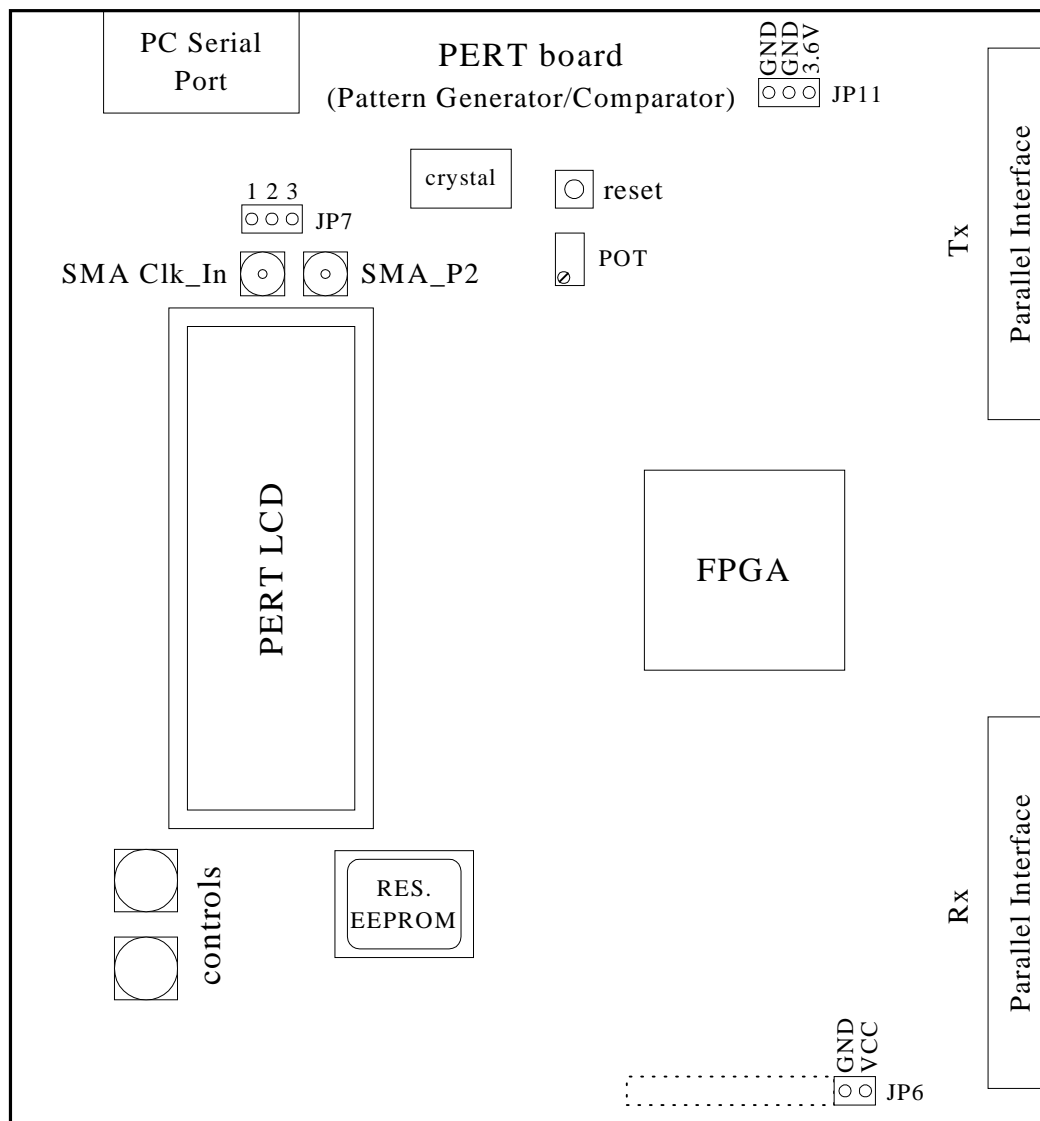
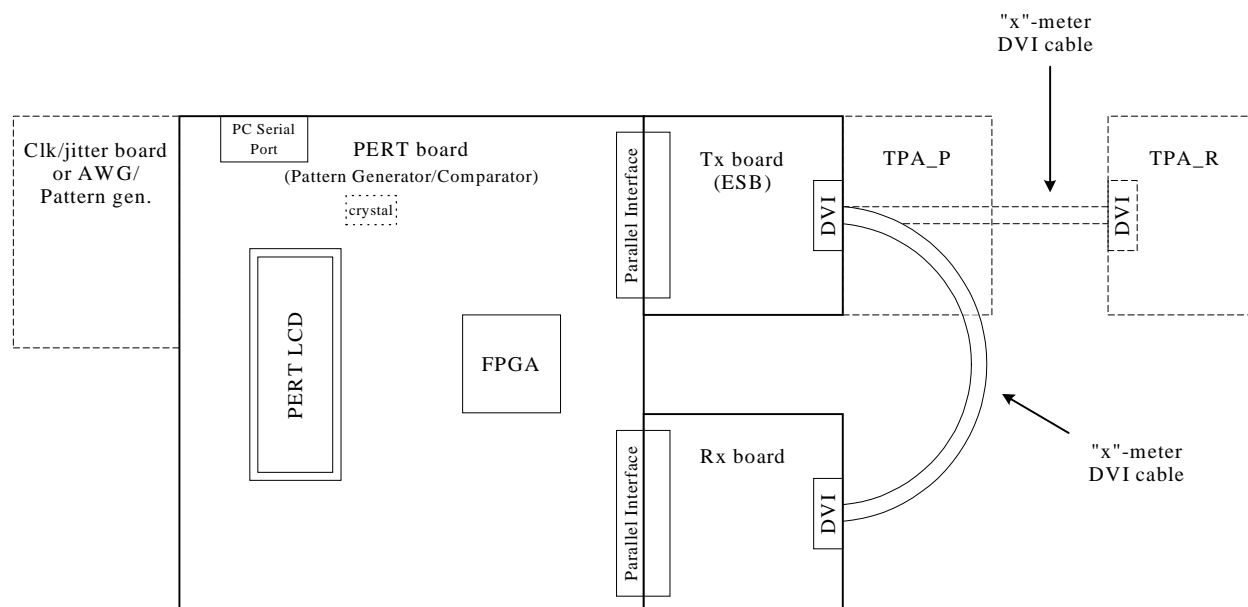


Figure 2.7 Pattern Generator and Comparator Board

The output of the pattern generator is supplied to the third board, containing a T.M.D.S. transmitter. This board has capabilities to vary the rise time, skew and amplitude of the differential data signals. Figure 2.8 shows the complete system of boards for the Equivalent Source Board, including the use of a TPA-P or TPA-R board to be used to calibrate the board, and the optional use of a receiver board to decode TMDS data for measuring pixel error rates, as

described in the next section. Collectively, the three boards are considered an equivalent source system, and will be shown as a single board for simplicity throughout the remainder of this guide.



*Figure 2.8 Equivalent Source Board System*

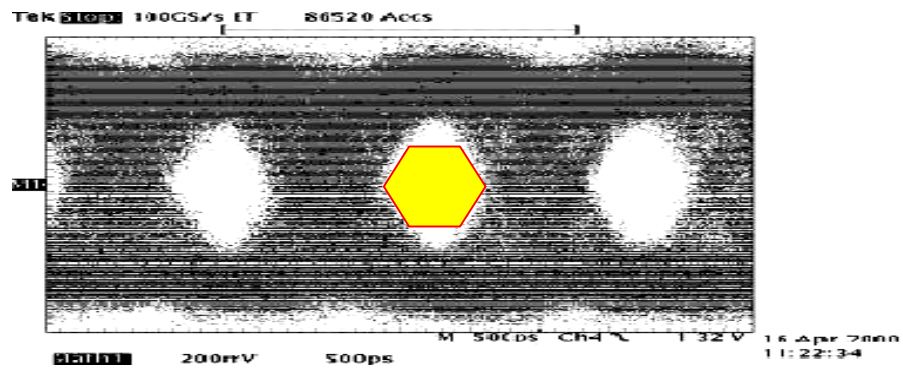
#### **TMDs Equivalent Source:**

Verification of cable assembly functionality must be done at the boundaries of transmitter signal quality, and receiver functionality must be verified at the boundaries of signal quality through the transmitter and cable assembly pair. The equivalent source provides T.M.D.S. signals with adjustments to certain parameters to enable these boundary conditions to be applied to cable assemblies and receivers under test. The parameters that must be adjusted are swing voltage, jitter, rise time, and skew.

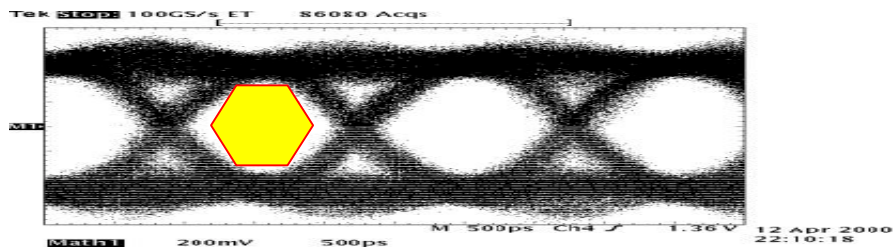
It is recommended that a transmitter with variable swing voltage be used for the equivalent source board. Rise time degradation may be accomplished through the addition of RC networks, and a waveform generator may drive the input clock source with a controlled jitter. Set up of the equivalent source board requires the adjustment of the variable parameters to match the output of the source to an eye pattern template within a tolerance band. These requirements are specified in the test setup sections of the cable assembly and receiver test sections.

Note that these parameters are not all easily adjustable. Thus, with a variety of source setups required for testing, it may be most practical to have unique boards set up for different tests. For instance, changing a resistor value may vary a transmitter swing voltage, and RC networks may require several iterations to achieve the desired rise time degradation.

In practice, it is difficult to provide a maximally degraded eye, which meets both the minimum amplitude and jitter openings, as shown in Figures 2.9 and 2.10. Thus it is appropriate to have two equivalent source boards, one of which can provide minimum amplitude, with some margin above the jitter spec, and another with minimum jitter tolerance and somewhat higher amplitudes. Each different clock speed (dependent on display resolution) will likewise require a specifically optimized board with an RC network tuned for that particular frequency.



*Figure 2.9 – Maximum Jitter Degradation of Eye Pattern*



*Figure 2.10 – Maximum Amplitude Degradation of Eye Pattern*

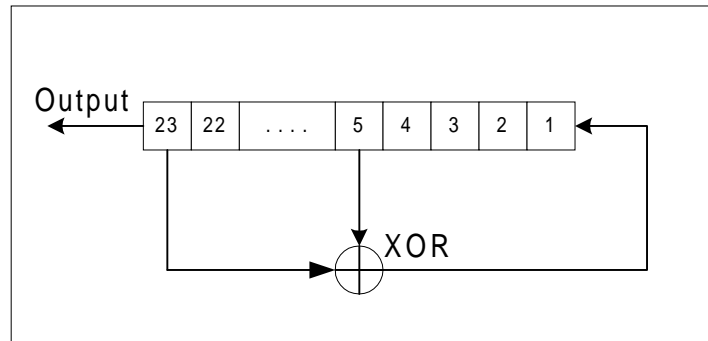
Although validation of the equivalent source is done when eye patterns are correctly adjusted for the test procedures that follow, it will be desirable to verify the pattern generator in a simplified system environment, using a nominal cable and receiver.

Using these three boards, it is possible to drive a variety of different waveforms into a cable or a receiver system to determine whether or not they are DVI compliant. In either case, an iterative approach of setting up the equivalent source to provide for example, a worst-case eye, verifying it with the TPA boards, and then driving this waveform into the device under test would be used.

### **Pattern Generator**

Two data patterns are required for the test measurements of this guide. For rise time and skew measurements, a data pattern with fewer transitions in the serial bit stream is used. This is referred to as the half clock pattern. For eye pattern measurements and pixel error rate tests, a pseudo random data pattern is used. When driving either test pattern the DE signal should be made inactive for a duration of 128 pixel clocks at the minimum DVI specified rate of once every 50 ms.

The half clock data pattern consists of alternating 0x3FF (all ones) and 0x000 (all zeros) T.M.D.S. characters. This data pattern occurs when alternating values of 0x01 and 0xFF are driven into the encoder, which will produce alternating 0x3FF and 0x000 characters on the serial T.M.D.S. signal lines. Note that the character boundary is not necessarily aligned with the pixel clock boundary. This low-frequency data pattern is used to determine the nominal high and low levels on the link as well as to measure skew and rise time. All T.M.D.S. data channels should be driven simultaneously with this same pattern.



*Figure 2-11 Pseudo Random Sequence Generator*

The pseudo random data pattern is a maximal-length sequence produced by a 23-bit linear feedback shift register (LFSR) with generator polynomial  $x^{23} + x^5 + 1$ . The logic diagram of Figure 2-11 produces the desired sequence when initialized to any non-zero value. The output serial stream becomes the input to the encoder, with the least significant bit of the input byte loaded first. This sequence contains a maximum run lengths of 23 ones and 22 zeroes for input to the T.M.D.S. encoder, and repeats after  $2^{23}-1$  bits. Simulation of  $10^9$  encoded bytes from this input sequence has shown maximum run lengths of 21 ones and 21 zeroes in the encoded bit stream, with all possible encoded values exercised.

When generating the pseudo random data pattern, each T.M.D.S. channel should be driven by a different phase of the shift register output. This may be done by implementing a separate shift register with unique initial values per channel or by taking the output from different bits of the register. To achieve the required speed, the LFSR may be run at the parallel clock rate, advancing the pipeline one position for each pixel clock.

It is strongly recommended that T.M.D.S. transmitters integrate this test pattern generator capability. For interoperability we recommend that the implementation should use the value of 0x000001 (all 22 bits are zeros except the LSB, bit 1 in Figure 2-11) as a seed. The 24 bits for channel 2[7:0], channel 1[7:0], and channel 0[7:0] data should be taken from {shift\_out, bit[23:1]}. For the receiver side pattern generation system to be able to synchronize the initialization should take place at a pre-defined timing. The first DE rising edge after VSYNC should be used as a load signal of the seed. The pipeline should be advanced by one position for each pixel clock.

## 2.5 Receiver Test Board

For receiver testing the visual test method is often the first measurement which is used. In this case the receiver test board is not needed. However, when the receiver manufacturer wants to quantify the pixel error rate then they will need this board or some equivalent instrument. As noted in Section 2.4, it is often convenient to incorporate a pattern reader and comparator into the pattern generation board used in the equivalent source system.

The receiver test board may be used for testing cables, but it is more likely to be used for testing receivers. No signal test points are necessary on this board, but some arrangement for the interface and the test pattern reader is required. Note that this test board can be completely replaced with other equipment such as a logic analyzer provided it implements the interface and pattern reader functions described below.

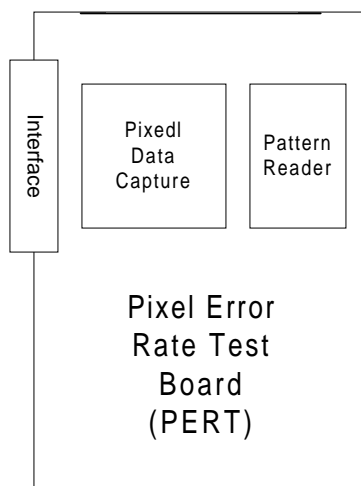


Figure 2-1 Receiver Test Board

### Interface

The interface unit reads the parallel pixel data from the receiver and feeds them to the data capture logic. To minimize the signal quality degradation the interface unit must have minimal physical dimensions so the loading capacitance is small and will not interrupt the normal operation. These signals are easier to handle than the T.M.D.S. signal, however, since they are slower signals and have a larger signal swing.

### Pattern Reader

The test board or the system must have a pseudo-random pattern reading capability (or an interface to such a reader) for pixel error rate test (PERT) measurements. The reader must be capable of auto-sync on the  $2^{23}-1$  bit data sequence defined in section 2.4, and must have a pixel error counter with reset. Any number of errors within the realigned three bytes of a single T.M.D.S. link constitutes one pixel error. A simple implementation of the PERT board would include a manual-reset error counter with a seven-segment LED display. The test may be performed over a time interval representing a known number of pixels and since the error count should be very low not many digits are necessary in the display.

For proper operation with the transmitter side random pattern generator, the pattern reader should be able to achieve the synchronized initialization as defined in section 2.2.

### 3 Test Equipment

Minimum requirements for and recommended models of test instruments are presented. Note that the list is not intended to be exhaustive and other brands of equipment can be used if their performance is equivalent to or better than the specifications below.

#### **TDR Scope**

For receiver impedance measurements one of the following digital sampling oscilloscopes with a TDR module can be used. The most important parameters are the rise time of the TDR module and the scope bandwidth. The rise time must be smaller than 50 ps and the bandwidth must be greater than 20 GHz.

- Tektronix 11801B/C Digital Sampling Oscilloscope with SD24 Sampling Head
- HP 54750A Digitizing Oscilloscope with HP 54753A TDR/TDT Module

#### **Spectrum Analyzer**

For clock recovery unit validation the jitter that is intentionally added by a waveform generator will be measured at the input and the output of the clock recovery unit (Figure 2-4). Since the frequency range of the pixel clock is from 25MHz to at most a few hundred MHz, the frequency range of the spectrum analyzer is not an issue, i.e., almost all spectrum analyzers can meet the requirement. More important parameters are the frequency response and the resolution bandwidth. Amplitude accuracy of frequency response must be within +/-1.5dB over the measurement range and the minimum resolution bandwidth must be less than or equal to 1KHz.

- Tektronix 2712
- HP 8590L
- HP E4411B

#### **Waveform Generators**

Waveform generators are used for clock input to the equivalent source board, for clock recovery unit validation, and for jitter measurements. The jitter of the master clock of the waveform generator must be at most 20 ps rms at 1 GHz or less than 2 percent of the period of the finest time scale of the equipment.



## 4 Transmitter Test Measurements

### 4.1 Test Setup

All transmitter tests are completed using the test setup of Figure 4-1. With both the half clock and the pseudo-random data patterns required for test measurements, it is recommended that the source driving the transmitter should implement pattern generator described in section 2.4.

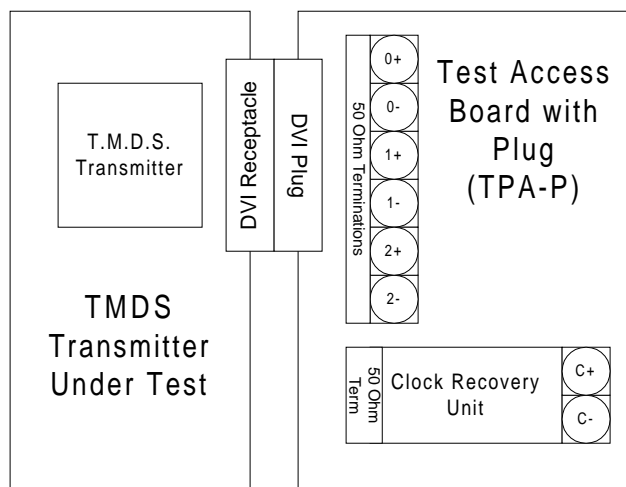


Figure 4-1 Transmitter Test Configuration

Normalized amplitude measurements are necessary for both single-ended and differential testing of the T.M.D.S. interface. These measurements are made with transmission of the half clock test pattern, and with the time base of the measurement equipment set to a scale that is coarse enough to observe at least two full pixel times. The average high-level and low-level amplitudes are determined at the point where signal ringing has subsided. These averages establish the swing voltage and are used to normalize the eye diagram.

### 4.2 Rise/Fall

Rise time is a differential measurement across the outputs of a differential pair while the half clock data pattern is transmitted. The trigger source of the scope is the half clock itself, i.e., the scope is self-triggered by the half clock data signal. Both rising and falling edges are measured. The rise time is defined as the time interval between the normalized 20% and 80% amplitude levels. It is recommended that the averaging feature of the equipment be used to read more stable values.

When the equipment's rise time is not negligible compared to the signal's rise time, the effect of the equipment should be removed using the equation:

$$Trise, fall = \sqrt{(Trise, fall \text{ _measured})^2 - (Trise, fall \text{ _equipment})^2}$$

In order to reduce the measurement error when using this equation, it is recommended that the equipment rise time be less than one third of the signal rise time.

### 4.3 Skew

The transmitter skew is the time difference between the two differential signals measured at the normalized 50% crossover point. This measurement is taken using two single ended probes. The trigger source can be either one of the two differential signals. Skew in the test set-up must be calibrated and removed from the recorded measurements by connecting both probes to the same signal. All of the signal pairs must be measured and the worst case recorded.

### 4.4 Jitter

Jitter measurement is performed as a differential measurement of the rising edge of the clock signal (clk+ minus clk-). The clock signal from the clock recovery unit in Section 2.1 must be used as a trigger source.

**Method I:** The differential clock signal must be accumulated for at least 100,000 acquisitions. The scope is used to determine the standard deviation of the 50% crossings in measuring time statistics of the differential clock signal. The random jitter at  $10^{-9}$  pixel error rate will be the  $\pm 6$  sigma limit points of the distribution. When the jitter includes any systematic components, care must be taken in obtaining the sigma value from the scope, otherwise the overestimated sigma value can lead to an excessively large value of the jitter limit.

**Method II:** As an easier and more practical alternative, accumulate at least 1,000,000 acquisitions and read the peak-to-peak jitter amount

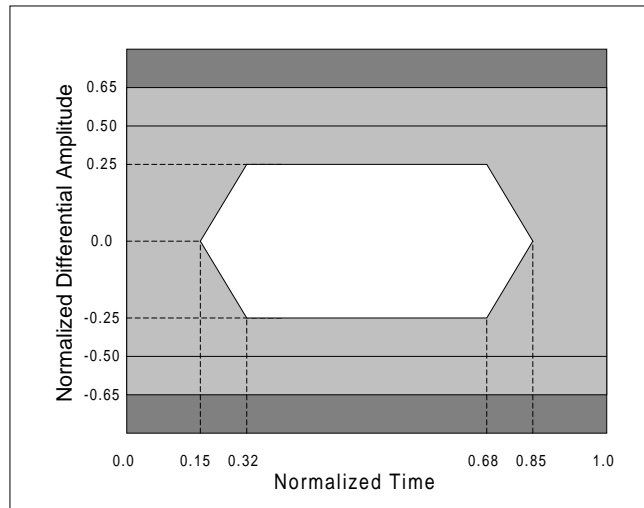
### 4.5 Eye Pattern

Eye measurement is performed as a differential measurement and the clock signal from the clock recovery unit in Section 2.1 must be used as a trigger source.

**Method I:** This test is made as a measurement of 100,000 acquisitions to achieve 99% confidence within 1% error of the mean value assuming normal distribution of the waveforms in the eye diagram. Referring to DVI transmitter eye pattern requirement of Figure 4.2, there are eight critical locations to collect the data of the means and standard deviations: at six horizontal segments of  $(0 < x < 0.15, y=0)$ ,  $(0.85 < x < 1.0, y=0)$ ,  $(0 < x < 0.32, y=0.25)$ ,  $(0.68 < x < 1.0, y=0.25)$ ,  $(0 < x < 0.32, y=-0.25)$ ,  $(0.68 < x < 1.0, y=-0.25)$ , and at two vertical segments of  $(x=0.5, 0.25 < y < 0.65)$  and  $(x=0.5, -0.65 < y < -0.25)$ .

The mean and standard deviation at each of the eight critical regions around the eye are used for time statistics at the six horizontal locations and for amplitude statistics at the two vertical locations. In all cases the eye must be degraded by  $\pm 6$  sigma limit points for the pixel error rate of  $10^{-9}$ .

**Method II:** This test is made as a measurement of 1,000,000 acquisitions and the result is recorded as the final eye diagram without any degradation.



*Figure 4-2 Normalized Eye Pattern Mask at TP2*

This test should then be repeated across all operating conditions of temperature, termination voltage, and termination resistance while the transmitter drives the pseudo-random data test pattern to ensure that the eye diagram limits given by the DVI spec are not exceeded.

## 5 Cable Assembly Test Measurements

### 5.1 Equivalent Source Setup

The T.M.D.S. equivalent source is connected to the TPA-P board and the equivalent source is adjusted to produce a low-amplitude eye pattern (Figure 5-2) and high-amplitude eye pattern (Figure 5-3) for input to the cable assembly under test. In each case the equivalent source must be adjusted to have, over the course of 1,000,000 acquisitions, points within the stippled regions of the mask but to have no points outside of the dark gray regions of the mask.

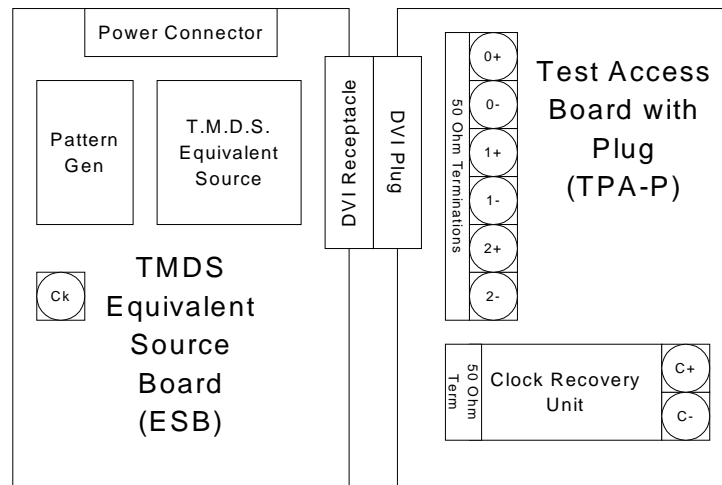


Figure 5-1 Cable Assembly Test Setup Configuration

Note that these masks are represented in absolute voltage levels.

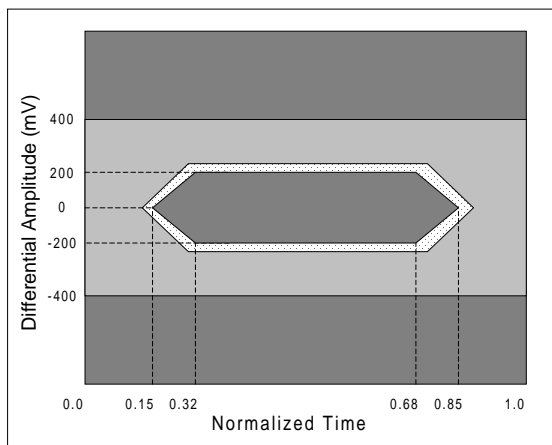


Figure 5-2 Cable Test Low-amplitude Eye Mask

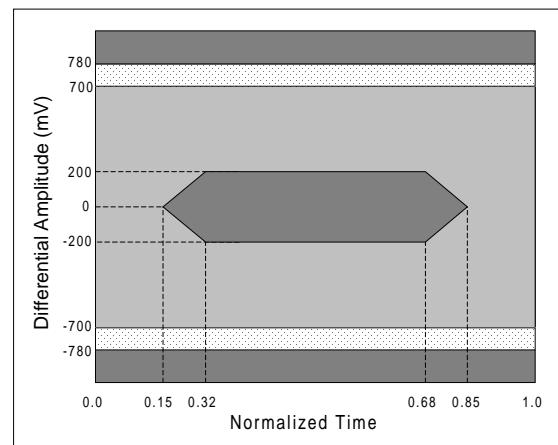


Figure 5-3 Cable Test High-amplitude Eye Mask

Once the eye has been adjusted the TPA-P is removed and is replaced by the cable assembly to be tested and a TPA-R (Figure 5-4). If it is desired to complete pixel error rate testing, a receiver test board is used in place of the TPA-R board.

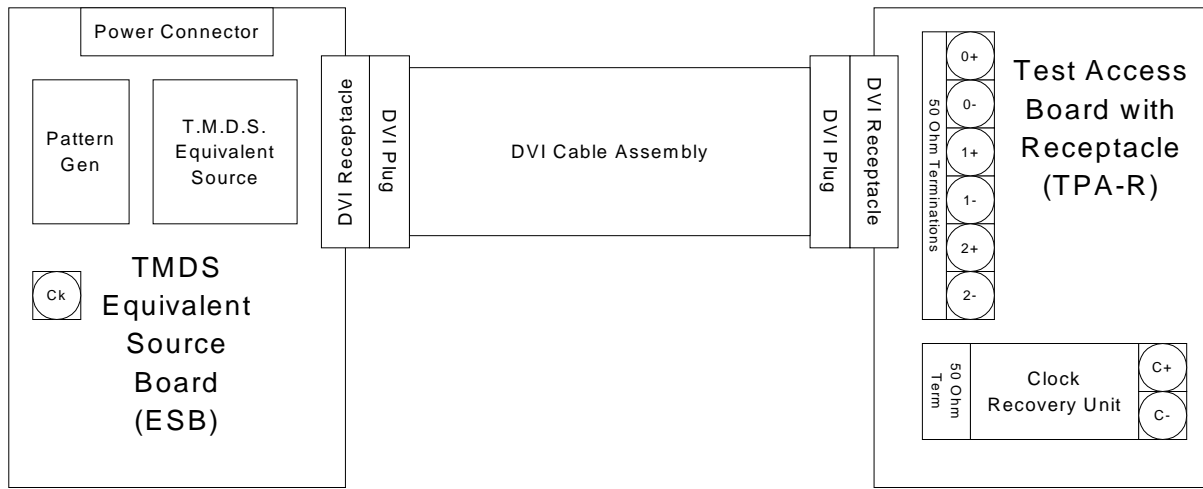


Figure 5-4 Cable Assembly Test Configuration

## 5.2 Skew

The cable assembly skew is the time difference between the two differential signals measured at the normalized 50% crossover point. TDR methods for the measurement of intra-pair and inter-pair skew on the cable assemblies are suggested for implementation, instead of TMDS signaling. These methodologies are well-defined, and can allow for greater precision in the measurement.

Alternatively, this measurement can be taken using two single-ended probes on the TPA board. Skew in the test set-up must be calibrated and removed from the recorded measurements. The equivalent source board transmits a continuous half clock character pattern. The data is averaged using an averaging scope. An easy method to view and measure the skew between these signals is to invert one of the signals. All of the signal pairs must be measured and the worst case recorded.

## 5.3 Eye Pattern

This test is made as a differential measurement at the TPA board of 1,000,000 acquisitions. The resultant eye diagram must be equal or better than the one shown in Figure 5-5.

## 5.4 Parametric Measurements

The cable assembly performance metrics listed in Table 1 are intended to offer the cable assembly manufacturer an alternative to eye pattern testing. These have been derived from well-known variables of assembly performance, in order to equivalently meet the eye pattern and PERT requirements of the link.

The impedance specification should be applied using the same interpretation as that stated on page 38 of the DVI specification, table 4-7, note a: “Within the exception window no single impedance excursion shall exceed the through connection impedance tolerance for a period of twice the TDR rise time specification. The maximum excursion within the exception window shall not exceed +75% and –25% of the nominal cable impedance.”

Parameter	Value
Near End Crosstalk	4%
Far End Crosstalk	3%
Differential Attenuation	8 dB at 825 MHz
Intra-pair Skew	151 picoseconds
Propagation Delay	5.05 nanoseconds/meter
Differential Impedance	100 ohms +/- 20

*Table 5-1 Cable Assembly Test Parameters*

## 6 Receiver Test Measurements

### 6.1 Equivalent Source Setup

The T.M.D.S. equivalent source is connected to the TPA-R board through a DVI cable assembly and the equivalent source is adjusted to produce low-amplitude eye pattern (Figure 6-2) and high-amplitude eye pattern (Figure 6-3) for input to the receiver under test. In each case the equivalent source must be adjusted to have, over the course of pre-defined number of samples, points within the stippled regions of the mask but to have no points outside of the dark gray regions of the mask. Note that these masks are represented in absolute voltage levels.

In case of **Method I**: The equivalent source must be adjusted so that the degraded eye diagram by  $\pm 6$  sigma should fit Figure 6-2 and Figure 6-3. As a differential measurement at the cable end with TPA-R board 100,000 acquisitions must be obtained to achieve 99% confidence within 1% error of the mean value assuming normal distribution of the waveforms in the eye diagram. There are eight critical locations to collect the data of the means and standard deviations: at six horizontal segments of  $(0 < x < 0.25, y=0)$ ,  $(0.75 < x < 1.0, y=0)$ ,  $(0 < x < 0.30, y=75\text{mv})$ ,  $(0.70 < x < 1.0, y=75\text{mv})$ ,  $(0 < x < 0.30, y=-75\text{mv})$ ,  $(0.70 < x < 1.0, y=-75\text{mv})$ , and at two vertical segments of  $(x=0.5, 75\text{mv} < y < 780\text{mv})$  and  $(x=0.5, -780\text{mv} < y < -75\text{mv})$ .

The mean and standard deviation at each of the eight critical regions around the eye are used for time statistics at the six horizontal locations and for amplitude statistics at the two vertical locations.

In case of **Method II**: The equivalent source must be adjusted so that the eye diagram with 1,000,000 acquisitions should fit Figure 6-2 and Figure 6-3.

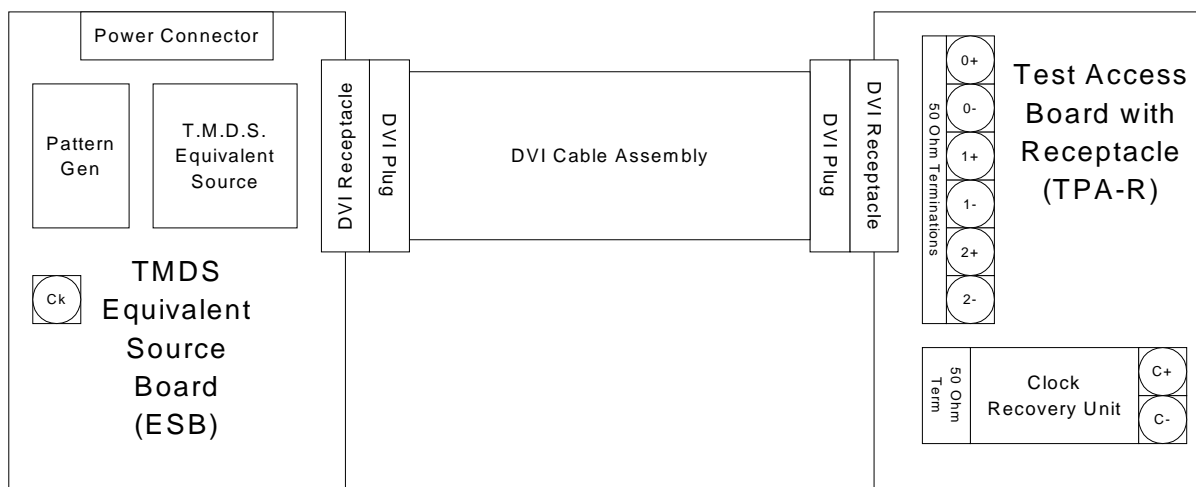


Figure 6.1 Receiver Test Setup Configuration

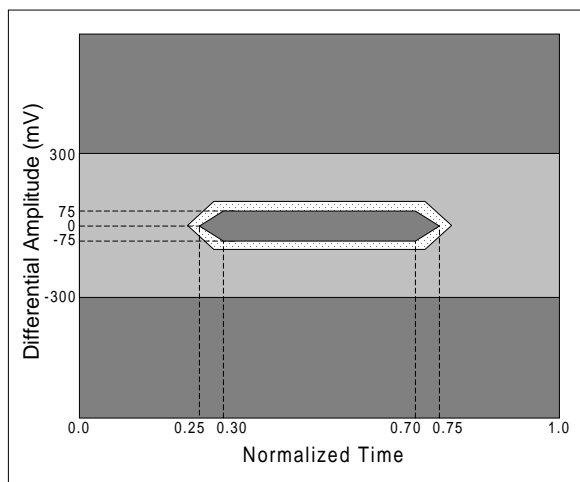


Figure 6-2 Receiver Test Low-amplitude Eye Mask

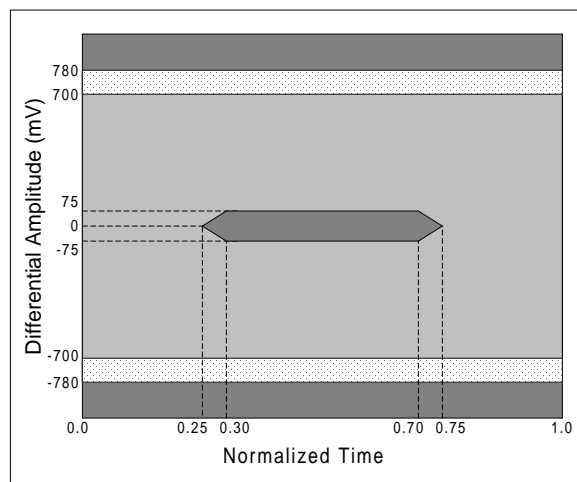


Figure 6-3 Receiver Test High-amplitude Eye Mask

## 6.2 Receiver Test

**Method I:** In this case the receiver pixel error rate is measured with the source set up according to Method I using the receiver test board or instrument described in Section 2.3.

### Duration of the pixel error rate test

For the pixel error rate of  $10^{-9}$ , at least one billion pixels should be tested. The following table shows the required amount of time for one billion pixels at each of the major resolutions of display, assuming a 60Hz refresh rate.

Resolution	Clock Frequency	Time for one billion pixels
VGA	25 MHz	40 Sec
SVGA	40 MHz	25 Sec
XGA	65 MHz	15 Sec
SXGA	112 MHz	9 Sec
UXGA	165 MHz	6 Sec

Table 6-1: Time required for 1 billion pixels at different display resolutions

To collect a statistically valid data for the pixel error rate, measurements should be made at least ten times independently.

**Method II:** In this case the display is checked to see if there is any noise on the recovered image. Meticulous observation during at least one minute must reveal no pixel noise.



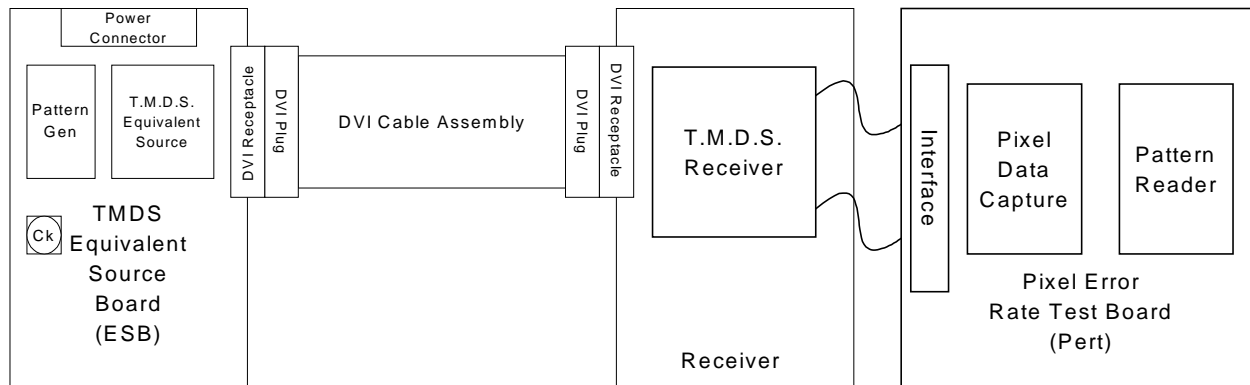


Figure 6-4 Receiver Test Configuration (Method I)

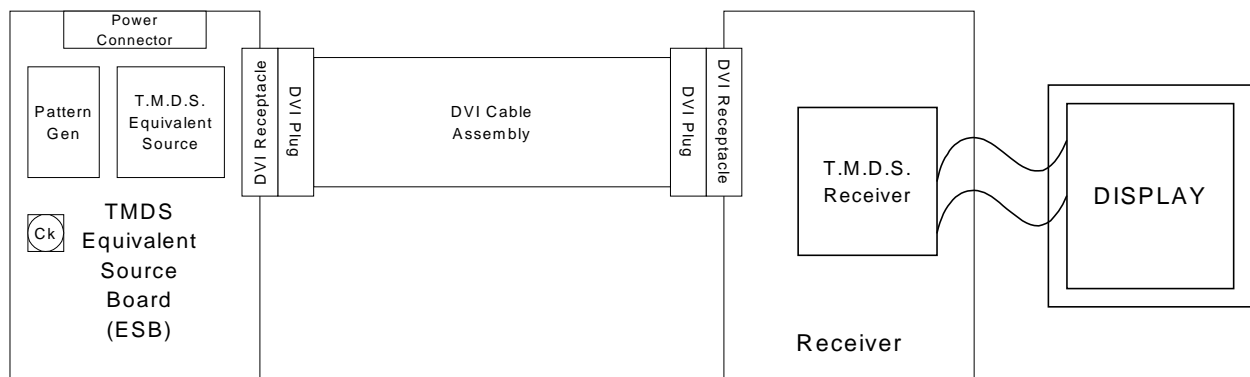
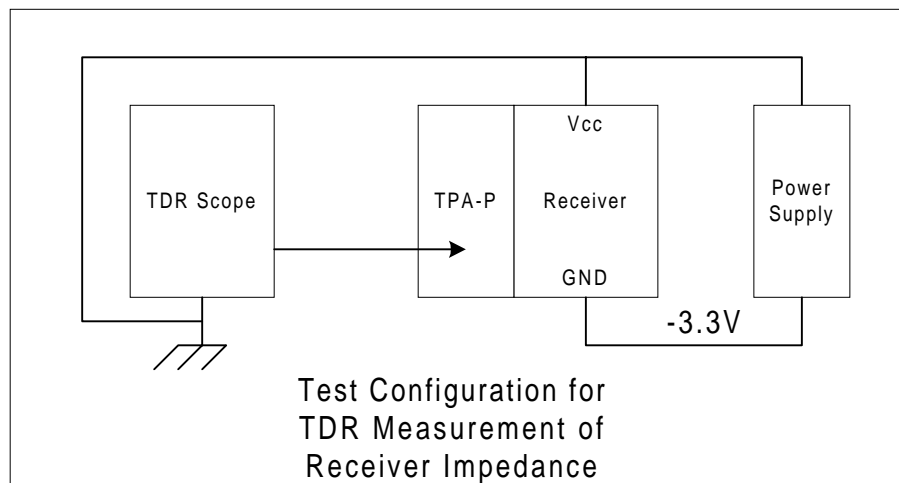


Figure 6-5 Receiver Test Configuration (Method II)

### 6.3 Receiver Impedance



*Figure 6-6 Receiver Impedance Test Measurement*

The differential time-domain reflectometry (TDR) test setup measures the reflected waveform returned from a load when driven with a step input. It is obtained by driving the load under test with a step waveform using a driver with a specified source impedance and rise time. The reflected waveform is the difference between (a) the observed waveform at the device under test when driven with the specified test signal, and (b) the waveform that results when driving a standard test load with the same specified test signal. From this measurement result we can infer the impedance of the device under test.

The driving waveform source is a balanced, differential 100-ohm source with a 75 ps rise time.