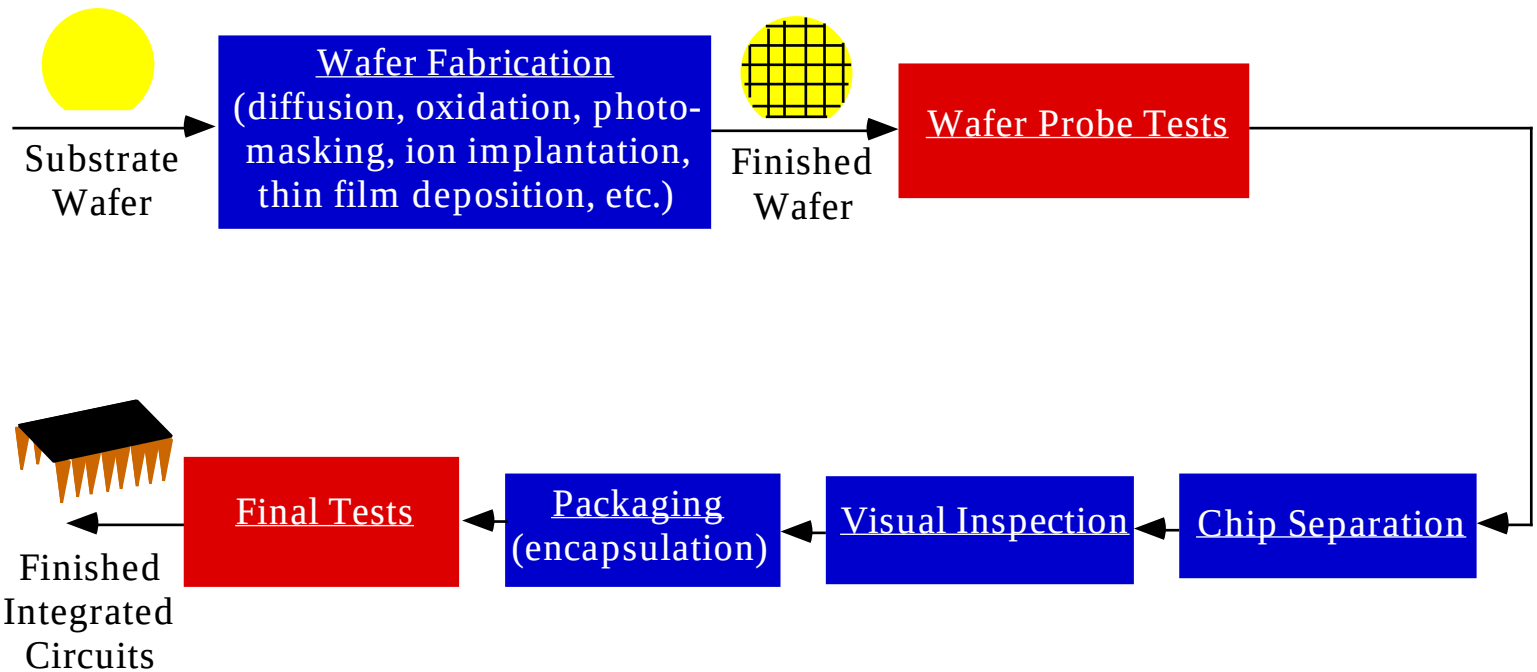
EE 560
FABRICATION OF MOS CIRCUITS

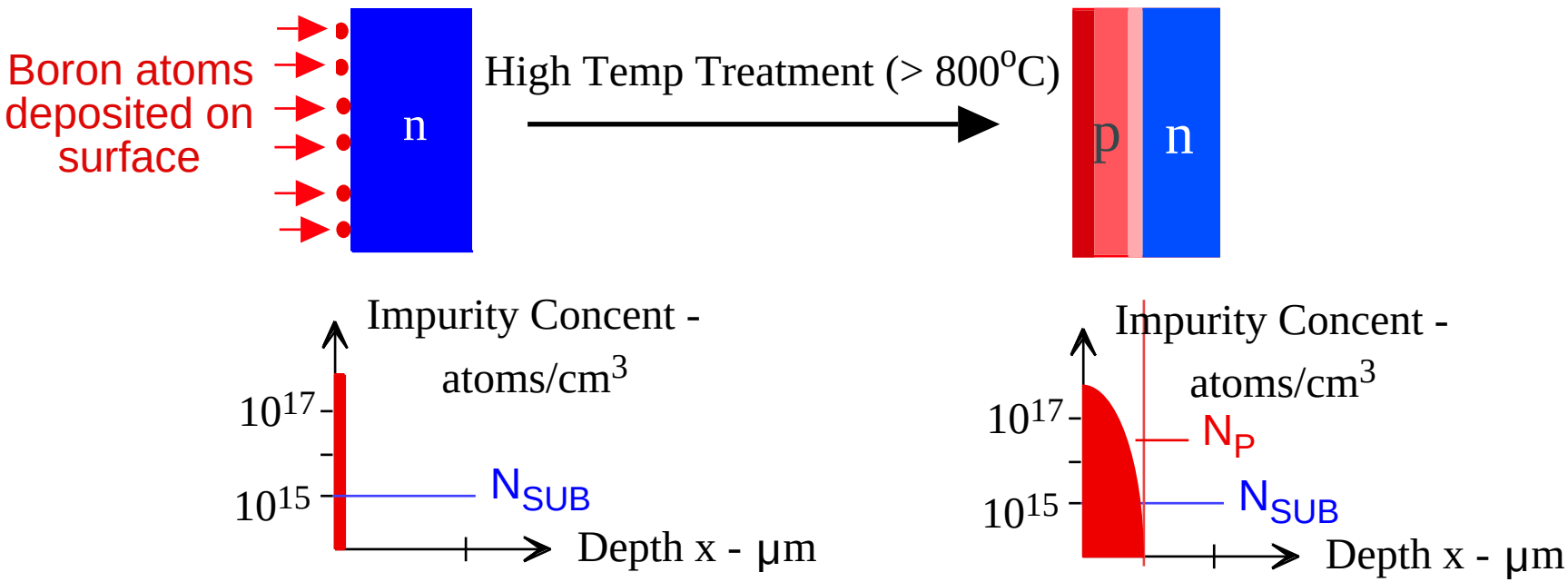
Kenneth R. Laker, University of Pennsylvania

CMOS CHIP MANUFACTRING STEPS



CMOS PROCESSING TECHNOLOGY

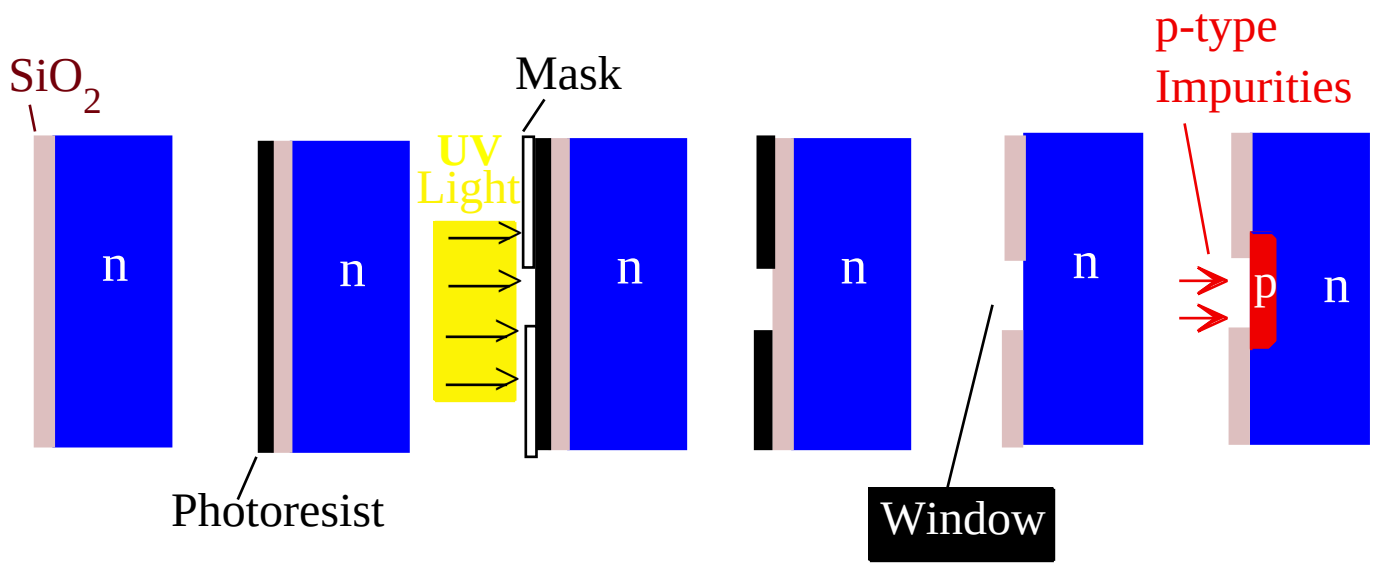
DIFFUSION PROCESS



-> Boron typically used for p-type doping

-> Arsenic and Phosphorus are typically used for n-type doping.

PHOTOLITHOGRAPHY



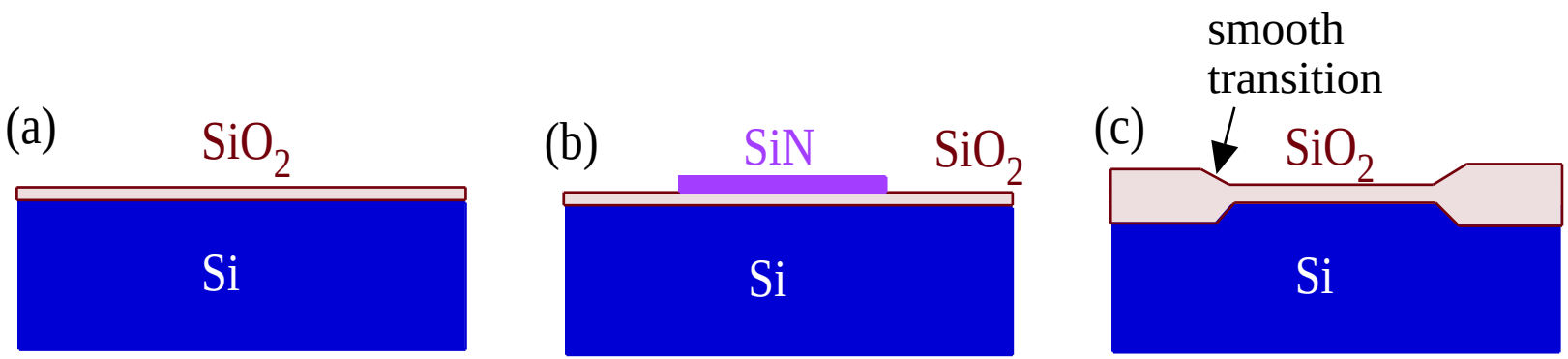
Methods for inserting impurity atoms into Si substrate

- ✗ Diffusion (high temperature)
- ✗ Epitaxial growth followed by diffusion
- ✗ Ion implantation (high velocity)

Local Oxidation of Silicon (LOCOS)

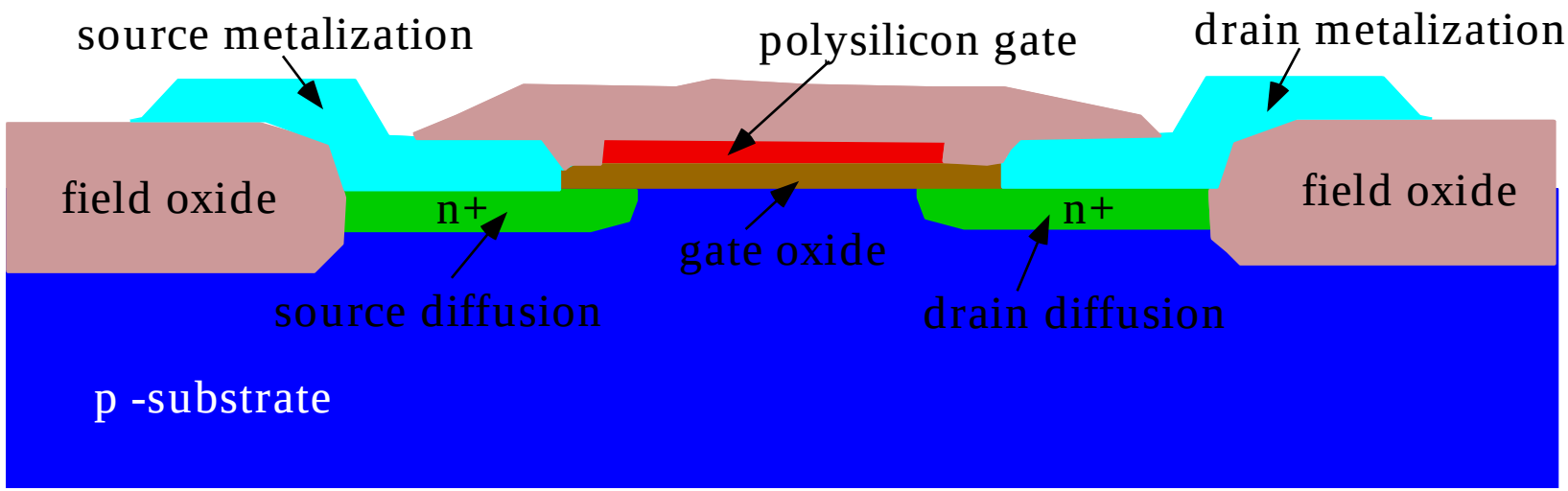
-> Fabricate thin SiO_2 layer adjacent to THICK SiO_2 layers.

-> Transition from THICK to thin SiO_2 layers fabricated WITHOUT creating sharp vertical transitions.

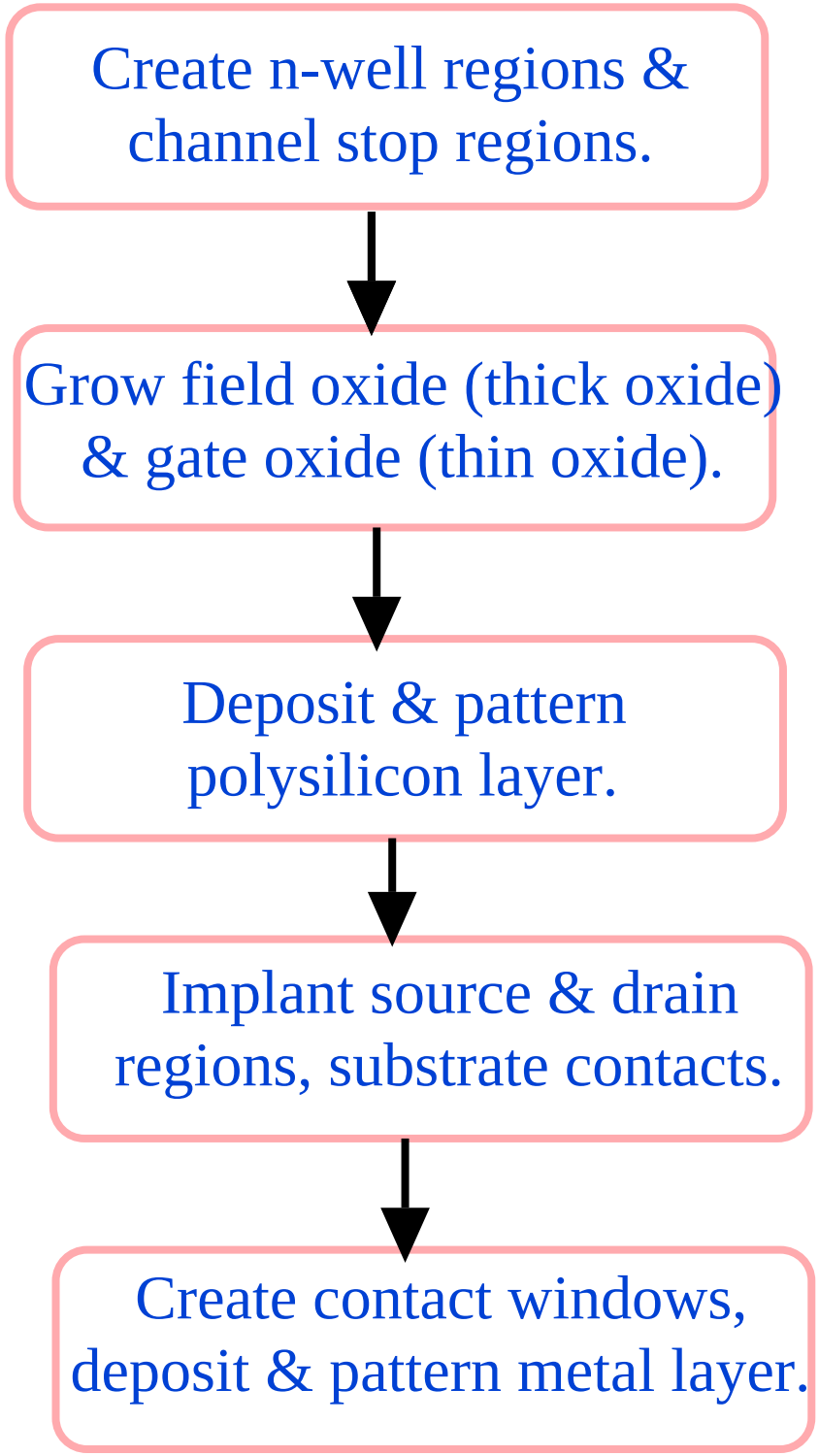


SiN acts as barrier to oxygen atoms, stops further oxidation at SiN-SiO_2 interface.

A FABRICATED n-MOS TRANSISTOR



Simplified process sequence for the fabrication of an n-well CMOS IC with a single polysilicon layer



Fabrication Steps in Si-Gate NMOS Process

Patterning SiO_2 Layer

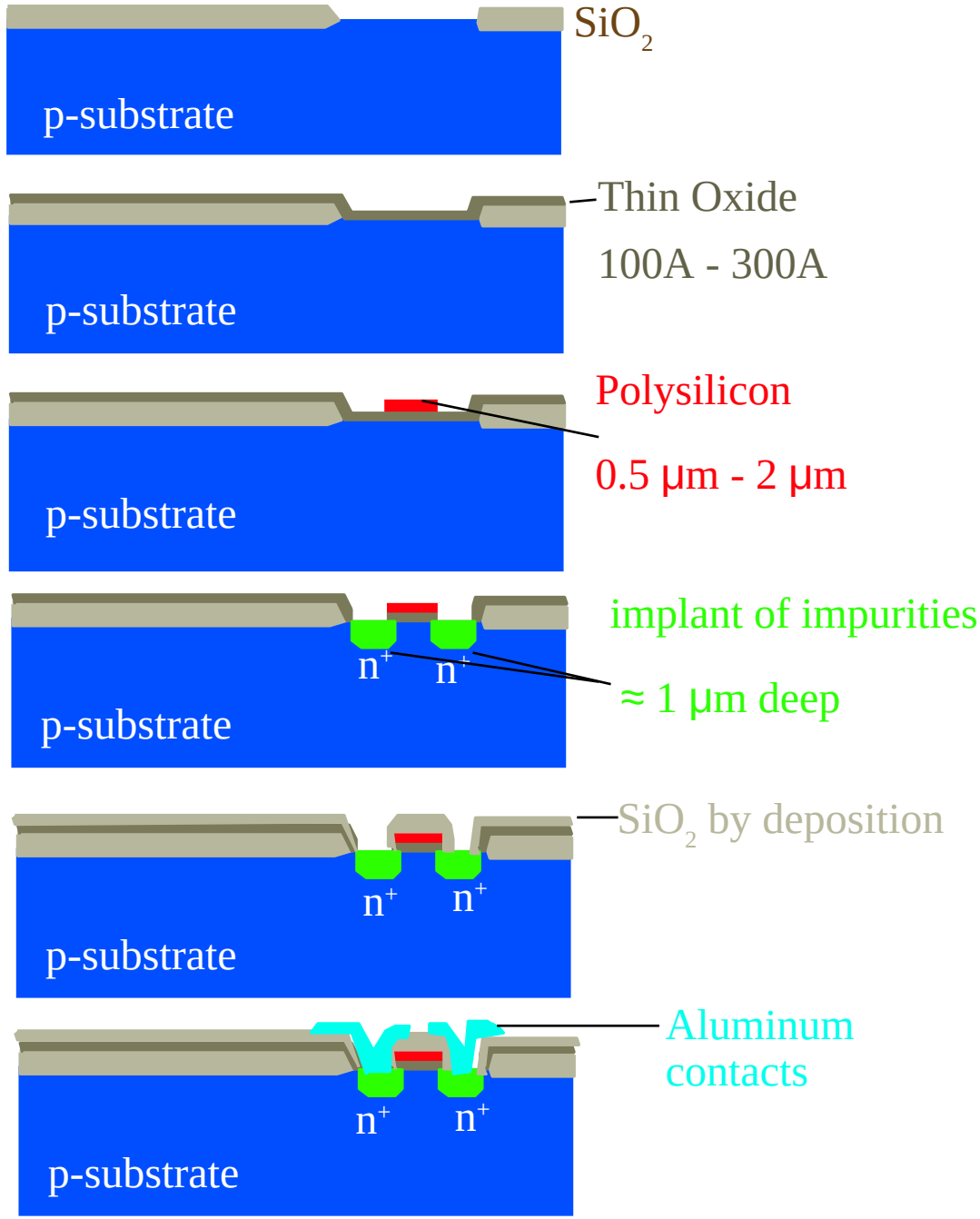
Gate Oxidation

Patterning Polysilicon

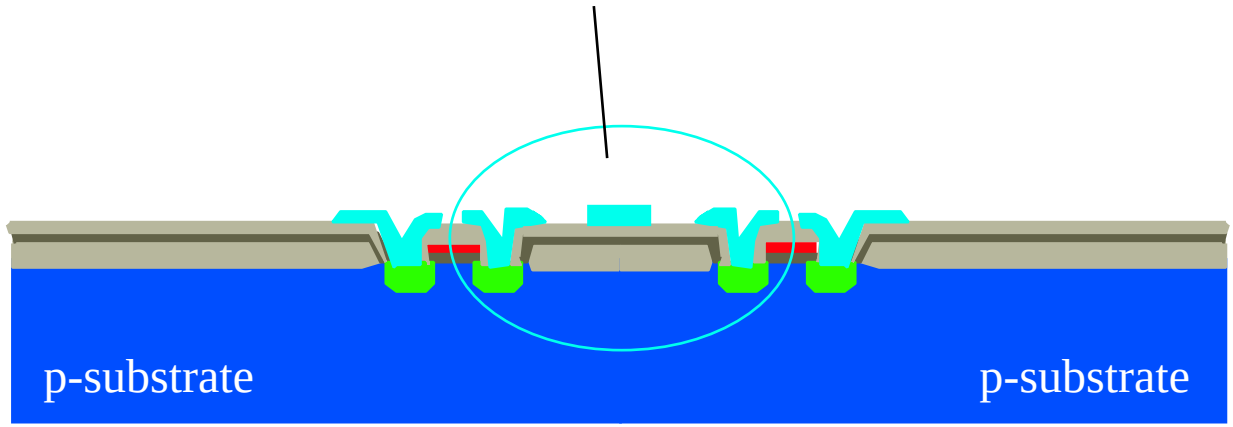
Source, Drain Inplants or Diffusions (self aligned)

Contact Cuts

Patterning Al Layer

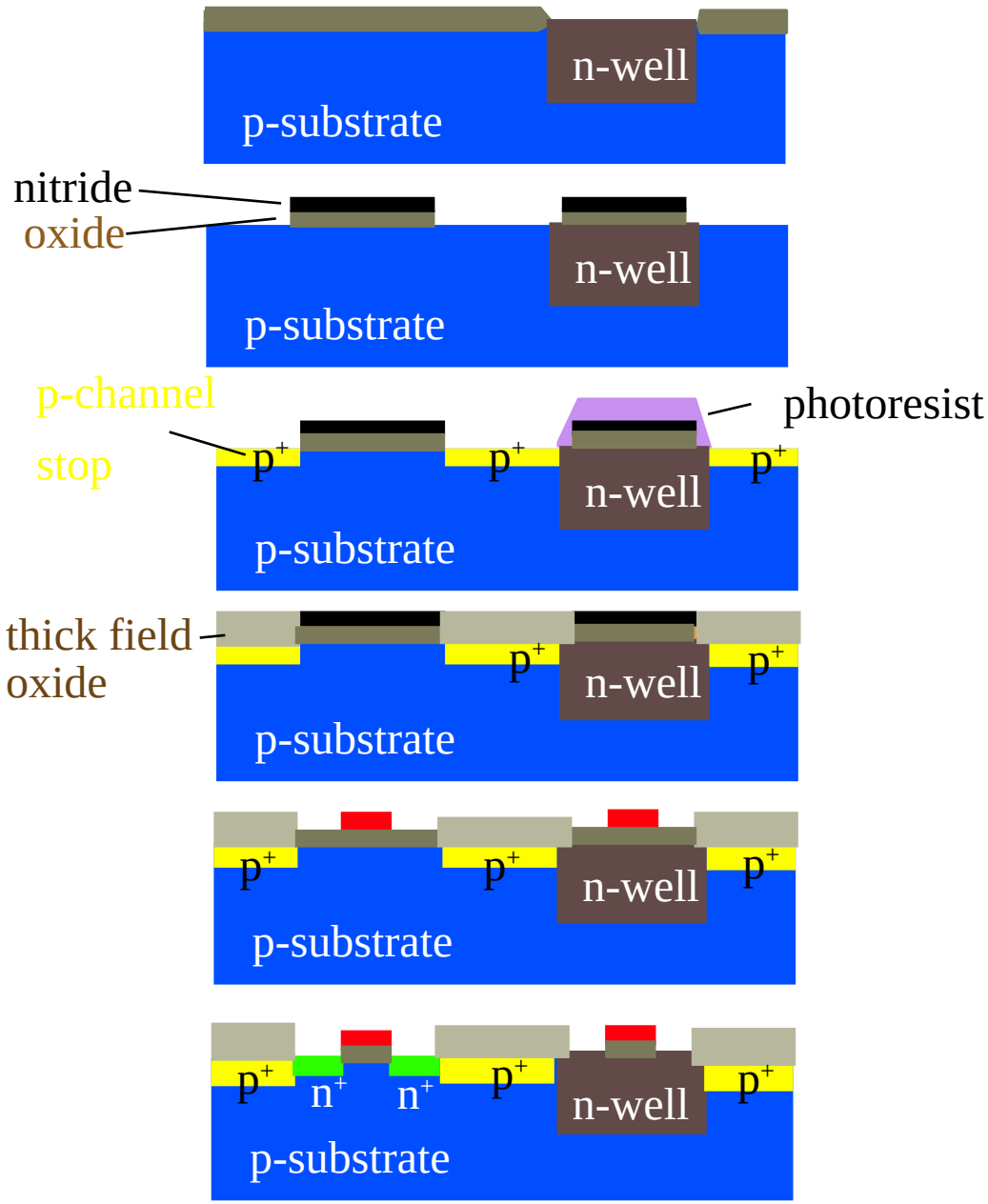


Parasitc MOS Transistor or Field Device

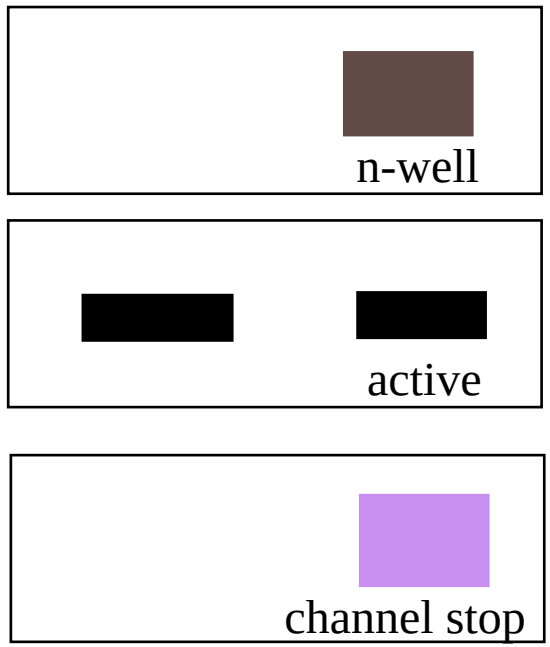


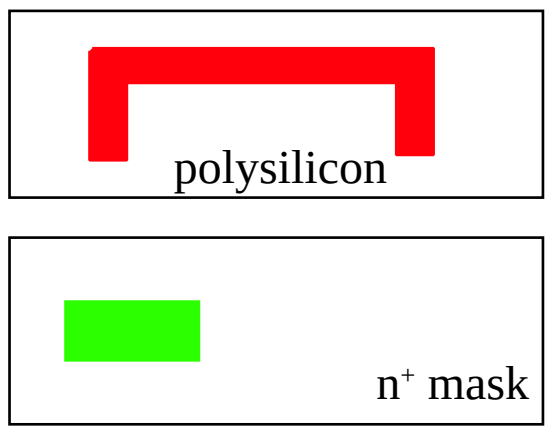
Typical N-Well CMOS Process

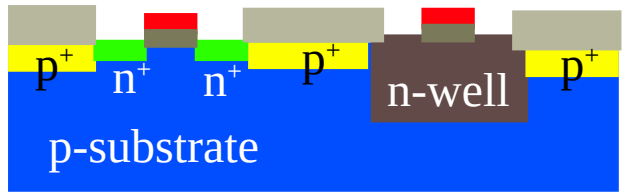
Physical Structure



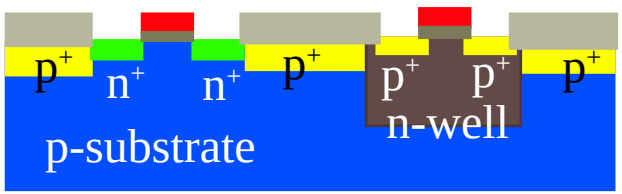
Mask Top View

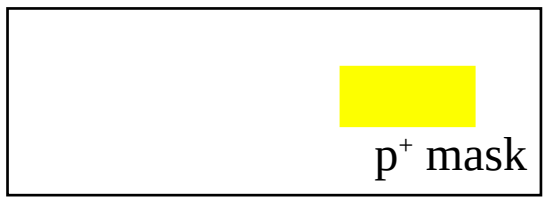


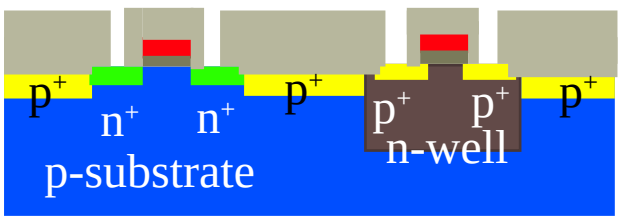


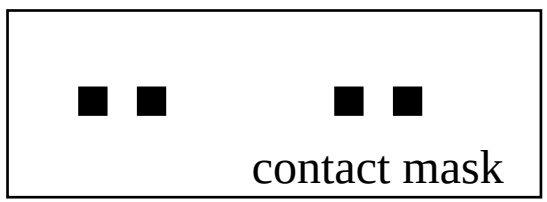

p+
n+
n+
p+
n-well
p+
p-substrate

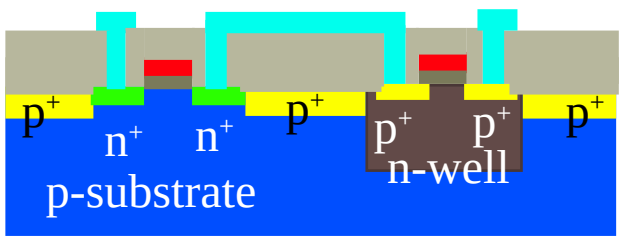

n+ mask

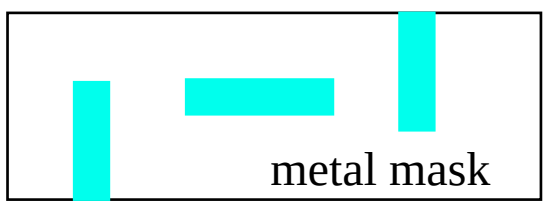

p+
n+
n+
p+
p+
p+
n-well
p+
p-substrate


p+ mask

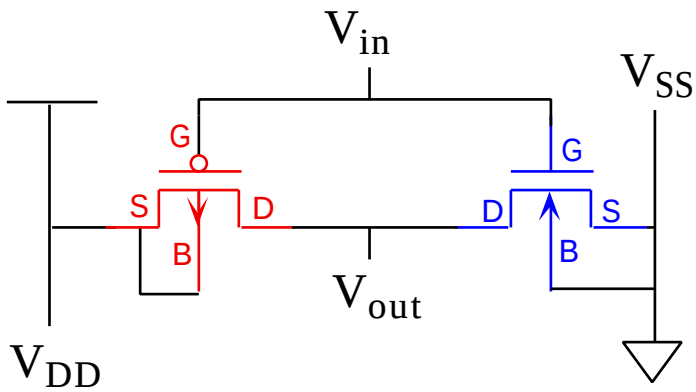

p+
n+
n+
p+
p+
p+
n-well
p+
p-substrate


contact mask


p+
n+
n+
p+
p+
p+
n-well
p+
p-substrate

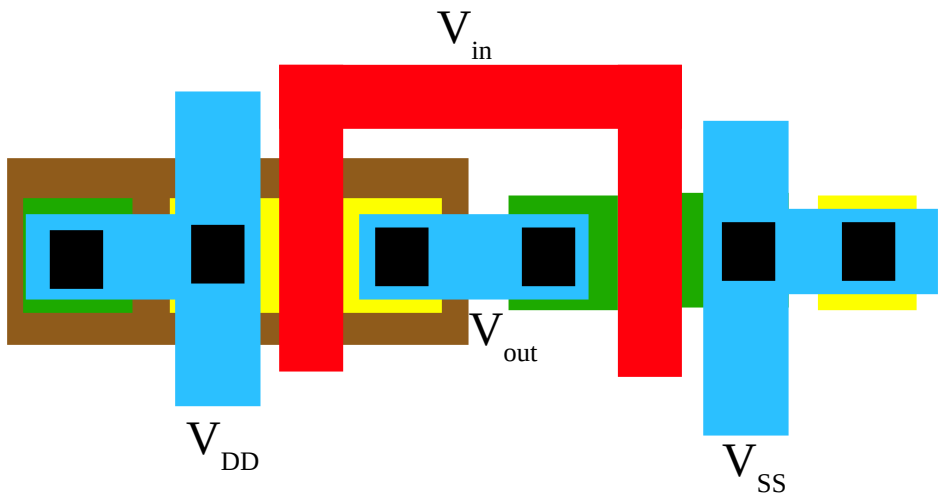

metal mask

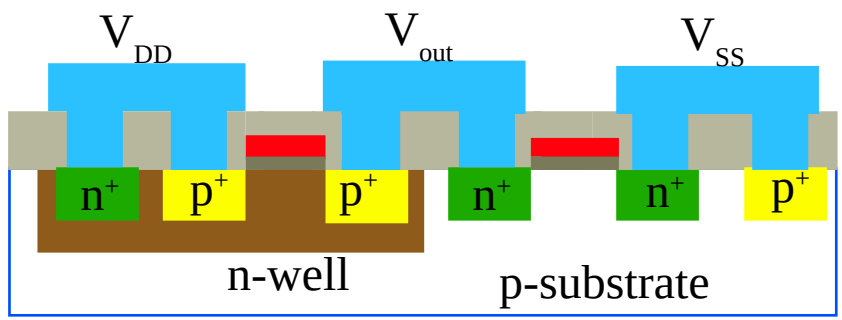
CMOS INVERTER LAYOUT IN AN N-WELL CMOS PROCESS



COLOR LEGEND

- n-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

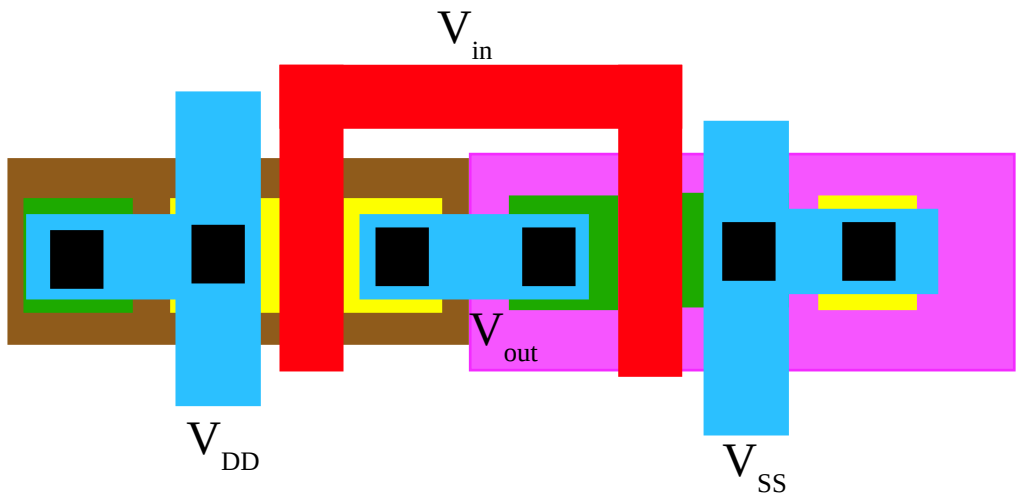


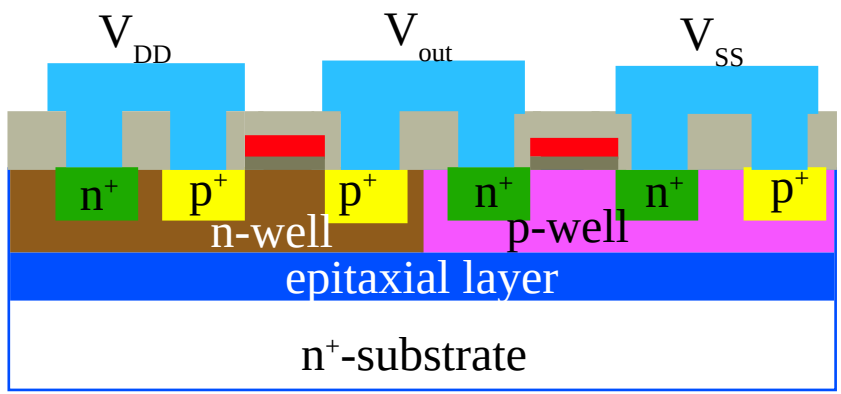


CMOS INVERTER IN TWIN-WELL CMOS PROCESS

COLOR LEGEND

- n-Well
- p-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

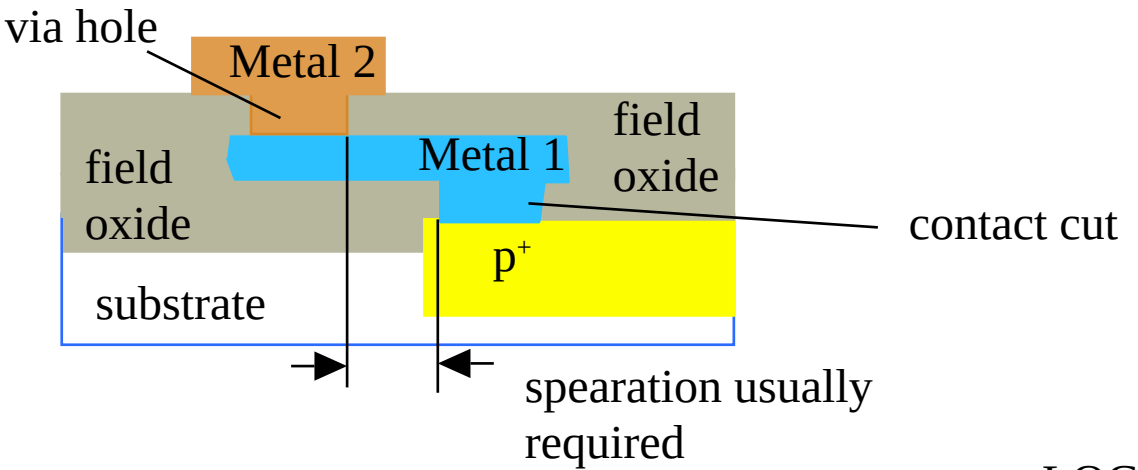




CMOS PROCESS ENHANCEMENTS

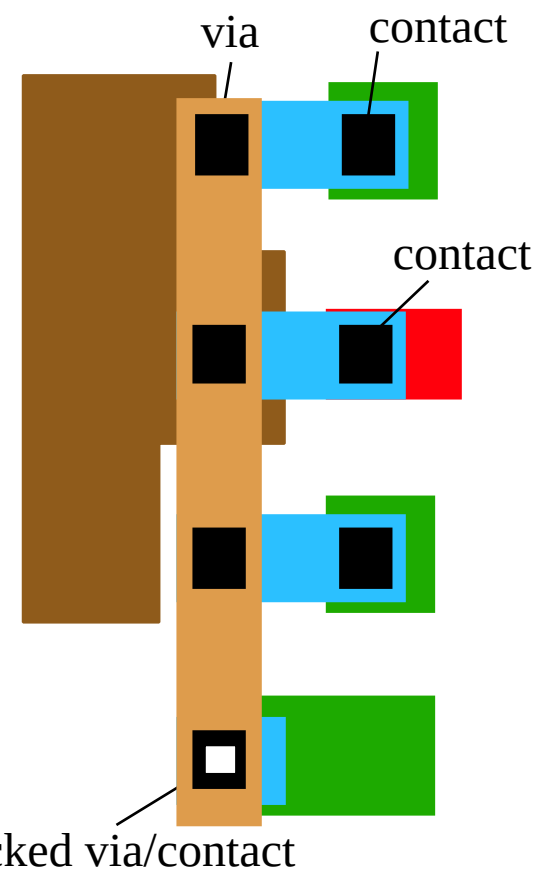
1. INTERCONNECT
    A. Metal Interconnect (two, three, four or more levels)
    B. Polysilicon (two or more levels, also for high quality capacitors)
    C. Polysilicon/Refractory Metal Inteconnect
    D. Local Inteconnect

2. CIRCUIT ELEMENTS
    A. Resistors
    B. Capacitors
    C. Electrically Alterable ROM (EAROM - EEROM - EEPROM)
    D. Bipolar Transistors

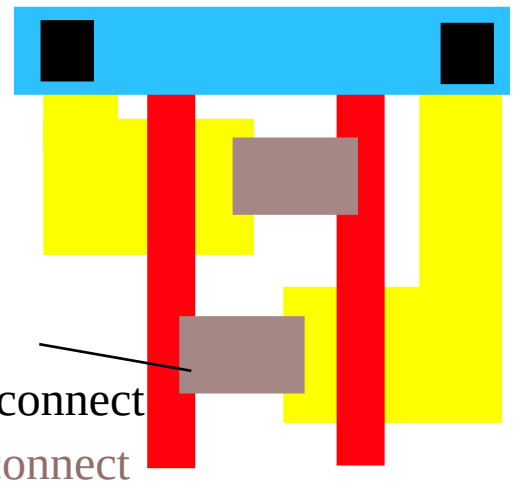


COLOR LEGEND

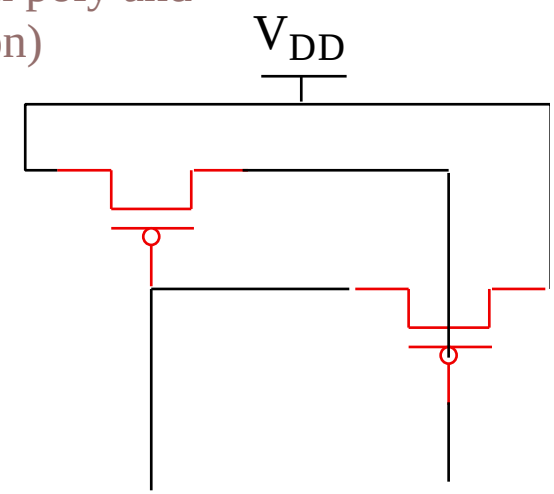
- n-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via



LOCAL INTERCONNECT

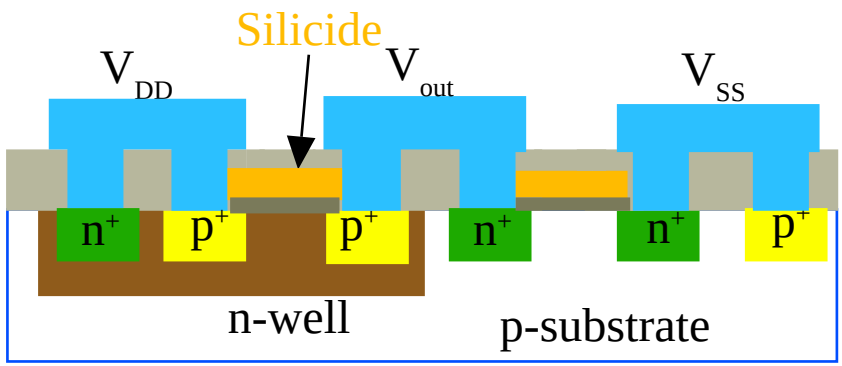


(direct connect between poly and diffusion)



Polysilicon/Refractory Metal or Silicide Gate/Interconnect Structures

(A)

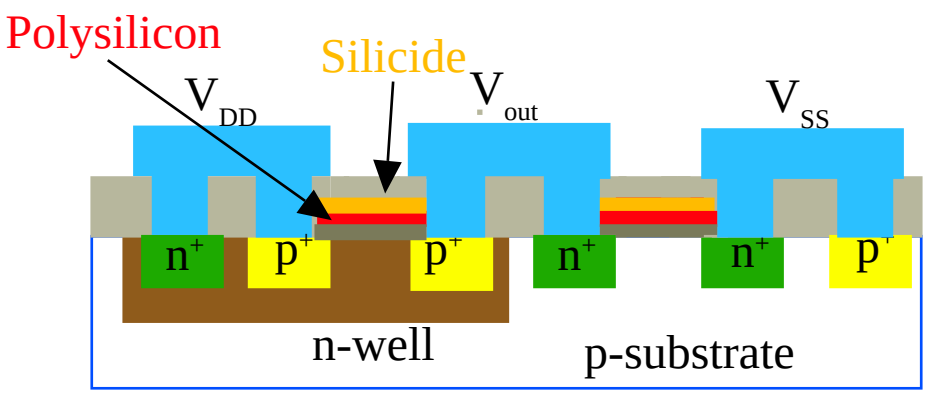


Silicide Gate (e.g. silicon and tantalum)

Doped Polysilicon: R_{sheet} = 20 to 40 Ω/Square

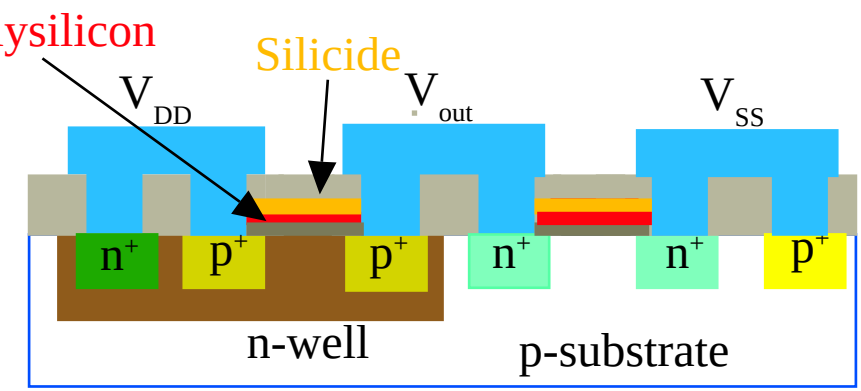
Silicide: R_{sheet} = 1 to 5 Ω/Square

(B)



Polysilicon/Silicide (Polycide) Gate

(C)

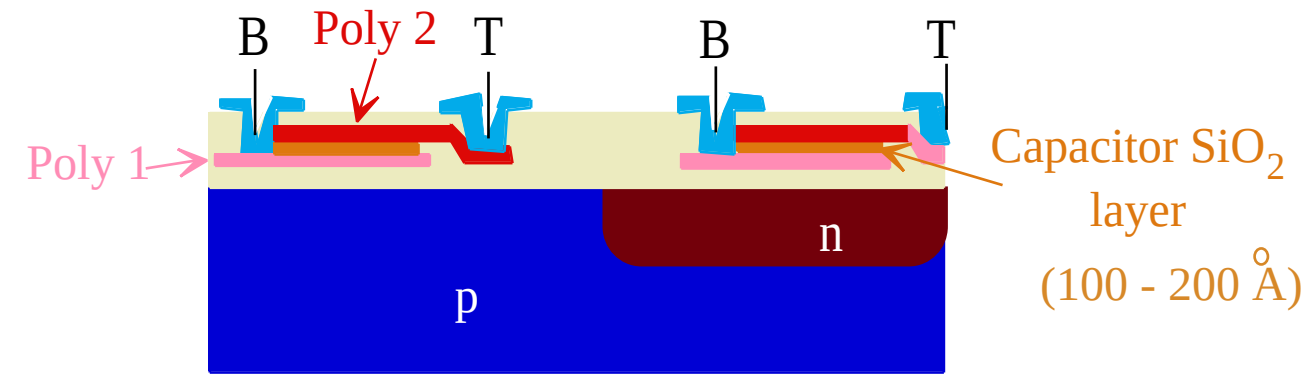


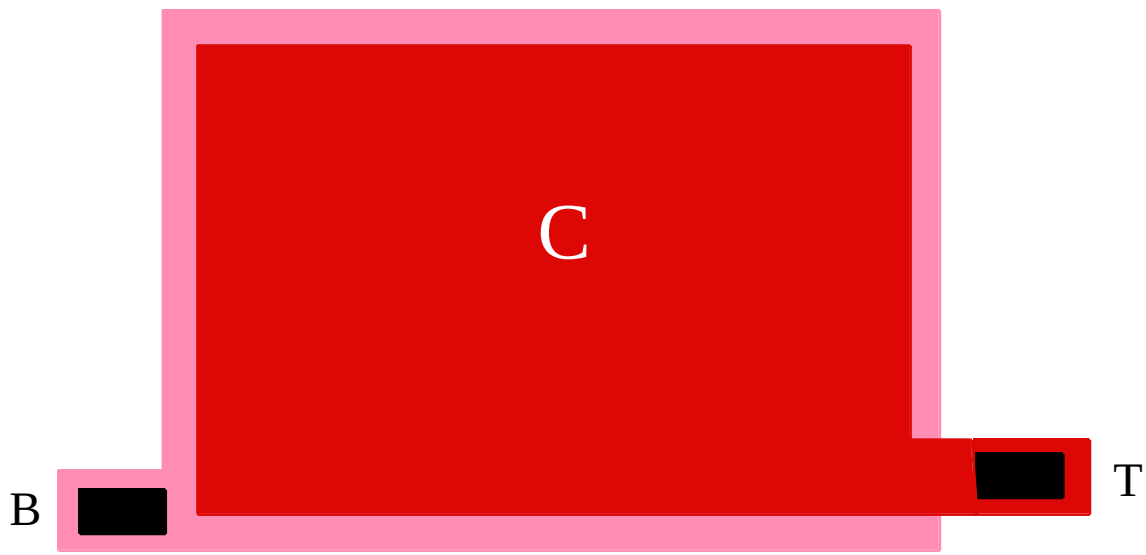
Self-Aligned Polysilicon/Silicide (Salicide)

(i) Polysilicon/silicide gate,

(ii) Silicide source/drain(s) p^+ n^+

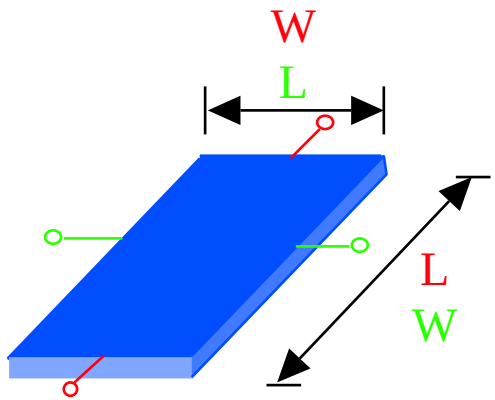
CMOS DOUBLE POLY CAPACITORS





$$C = C_{oxC} WL \qquad C_{oxC} = \frac{\varepsilon_{ox}}{t_{oxC}}$$

RESISTORS



$$R = \left(\frac{\rho}{t}\right)\frac{L}{W} = R_s\frac{L}{W} \quad \Omega$$

ρ = resistivity

t = thickness

L = conductor length

W = conductor width

R_s = sheet resistance Ω/sq

Typical Sheet Resistance for Conductors (R_s - Ω/sq)

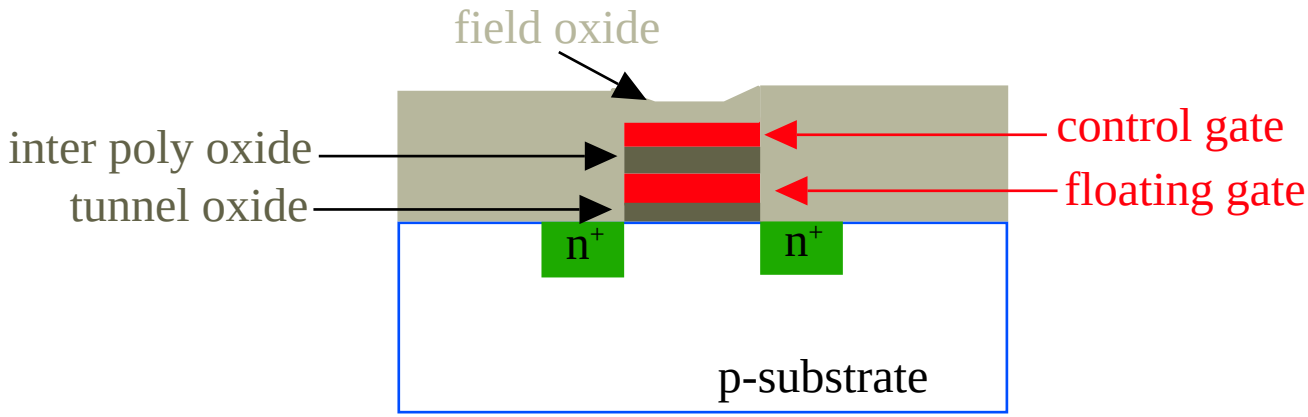
Material	Min	Typ	Max
Metal - Meal 2	0.05	0.07	0.1
Metal 3	0.03	0.04	0.05
Polysilicon	15	20	30
Silicide	2	3	6
n^+, p^+ Diffusion	10	25	100
n-Well	1K	2K	5K

$$R_c = k\frac{L}{W} \quad \Omega$$

$$k = \frac{1}{\mu C_{ox}(V_{gs} - V_T)}$$

MOS Resistor

EEPROM TECHNOLOGY



$$I_{FN} = C_1 W L E_{ox}^2 e^{-E_o/E_{ox}}$$

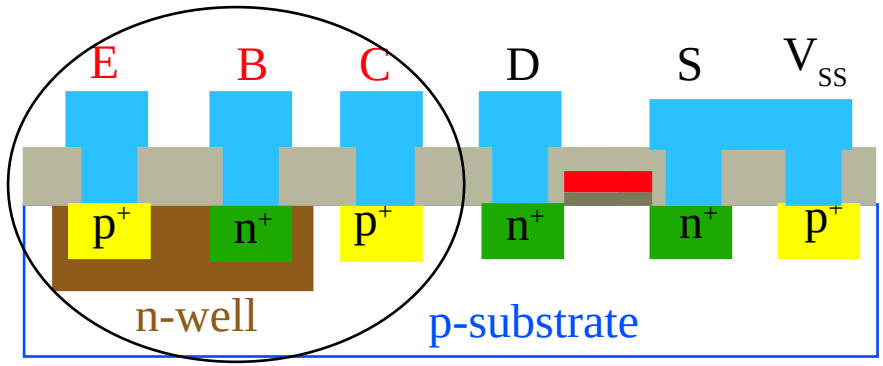
where

$$E_{ox} = \frac{V_{gs}}{t_{ox}}$$ electric field across tunnel oxide

E_0 and C_1 are process dependent constants

BIPOLAR TRANSISTORS IN STANDARD CMOS

Substrate pnp Bipolar Transistor



LAYOUT DESIGN RULES

PHYSICAL LAYER: prescription for preparing photomasks used in fabrication of ICs. Specify to the designer geometric constraints on the layout artwork so that patterns on the processed wafer will preserve the intended topology and geometry of the design.

PURPOSE: realize fabricated circuits optimum yield in smallest area possible without compromising the reliability of the circuit.

DESIGN RULE WAIVER: any significant and/or frequent departure from design rules.

TWO TYPES OF DESIGN RULES:

a. line widths and separations

b. interlayer registration

DESIGN RULE SPECS:

a. 'micron' rules - minimum feature sizes and spacings in μm units (normal spec in industry)

b. 'lambda (λ)' rules - minimum feature sizes and spacings speced in terms of a single parameter λ (popularized by Mead and Conway and permits first order scaling)

LAYOUT DESIGN RULES

The Design Process can be Abstracted to Manageable Number of Layout Levels that Represent the Physical Features on the Processed Silicon Wafer, i.e.

-> Two different substrates (i.e. original substrate + well or twin wells)

-> Doped regions p- and n- transistor forming materials (e.g. sources and drains)

-> Transistor gate electrodes

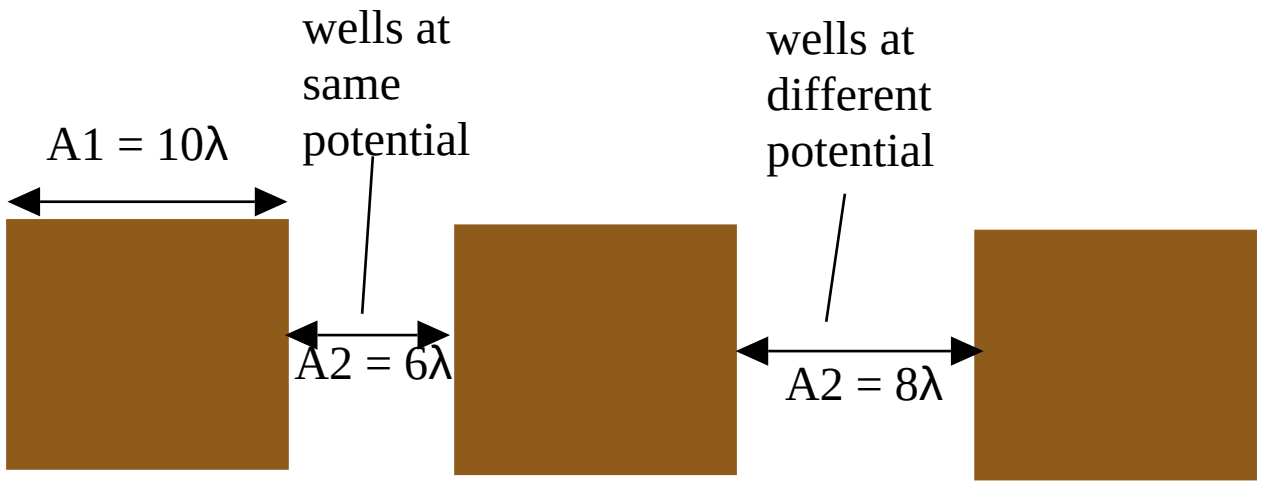
-> Interconnect paths

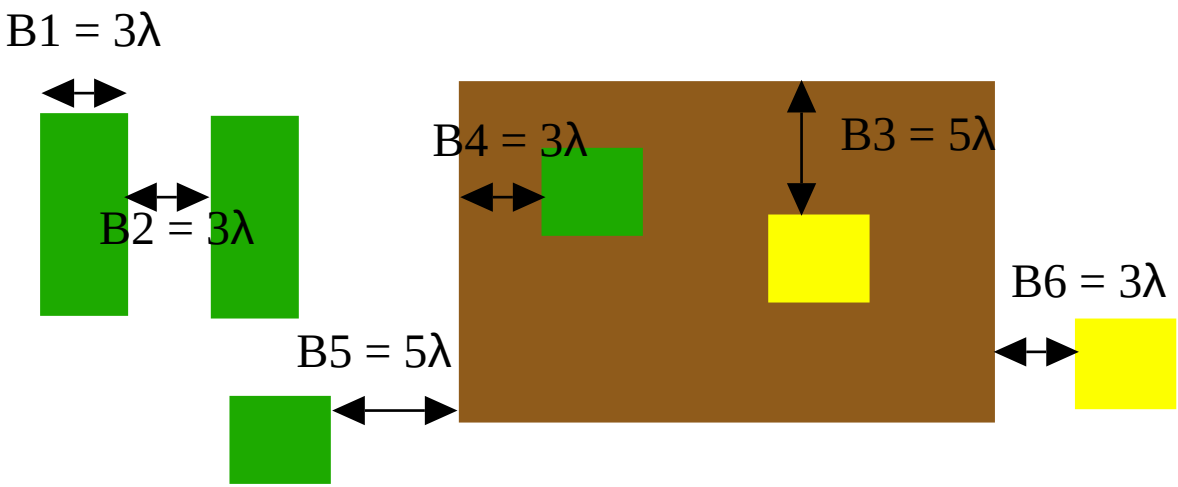
-> Interlayer contacts

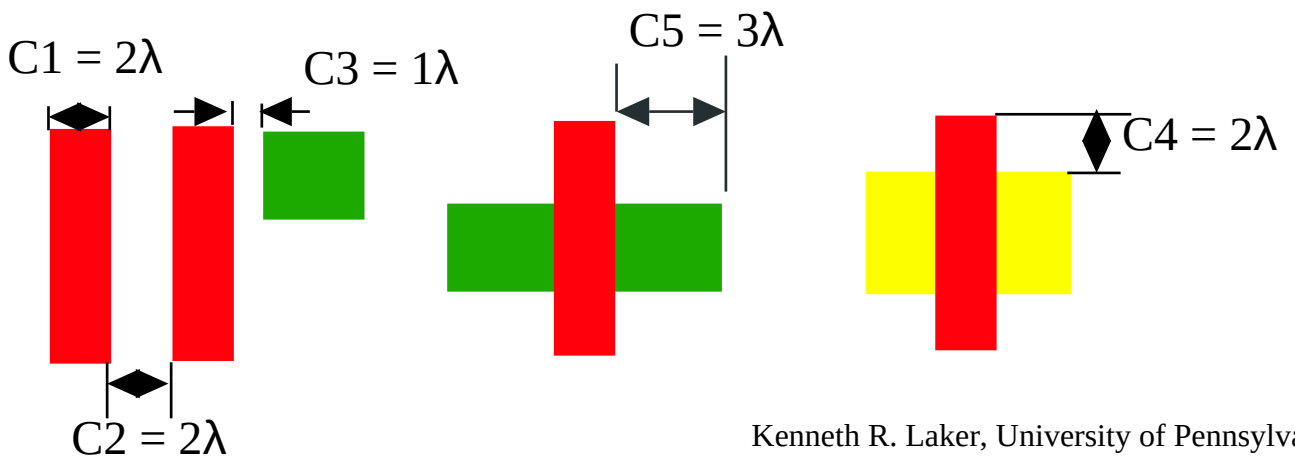
CMOS N-WELL DESIGN RULES

COLOR LEGEND

- n-Well
- p-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via





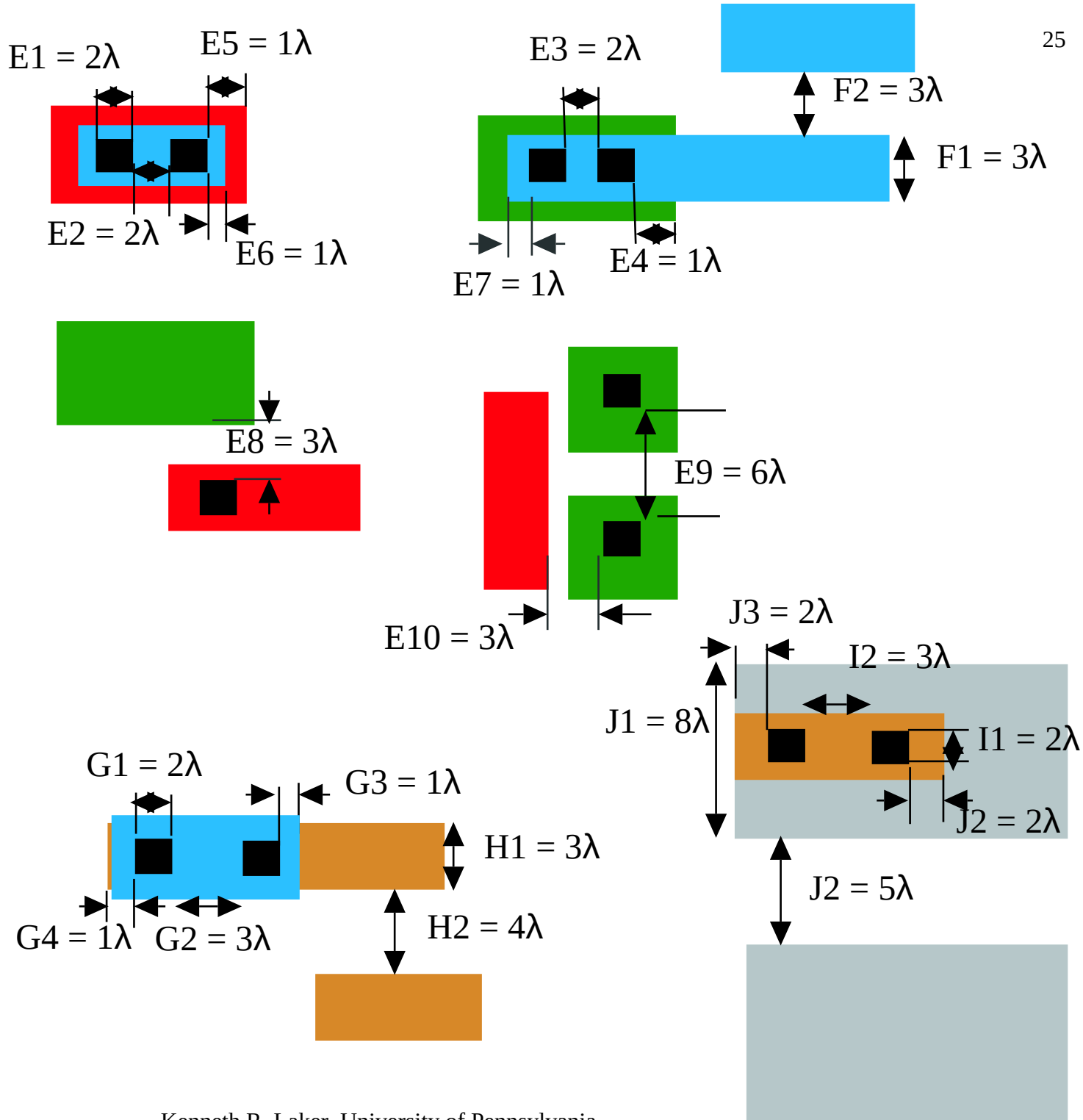


B1 = TEXT - R1
B2 = TEXT - R2
C1 = TEXT - R3
C2 = TEXT - R4
C3 = TEXT - R6
C4 = TEXT - R5 C5 = TEXT - R7

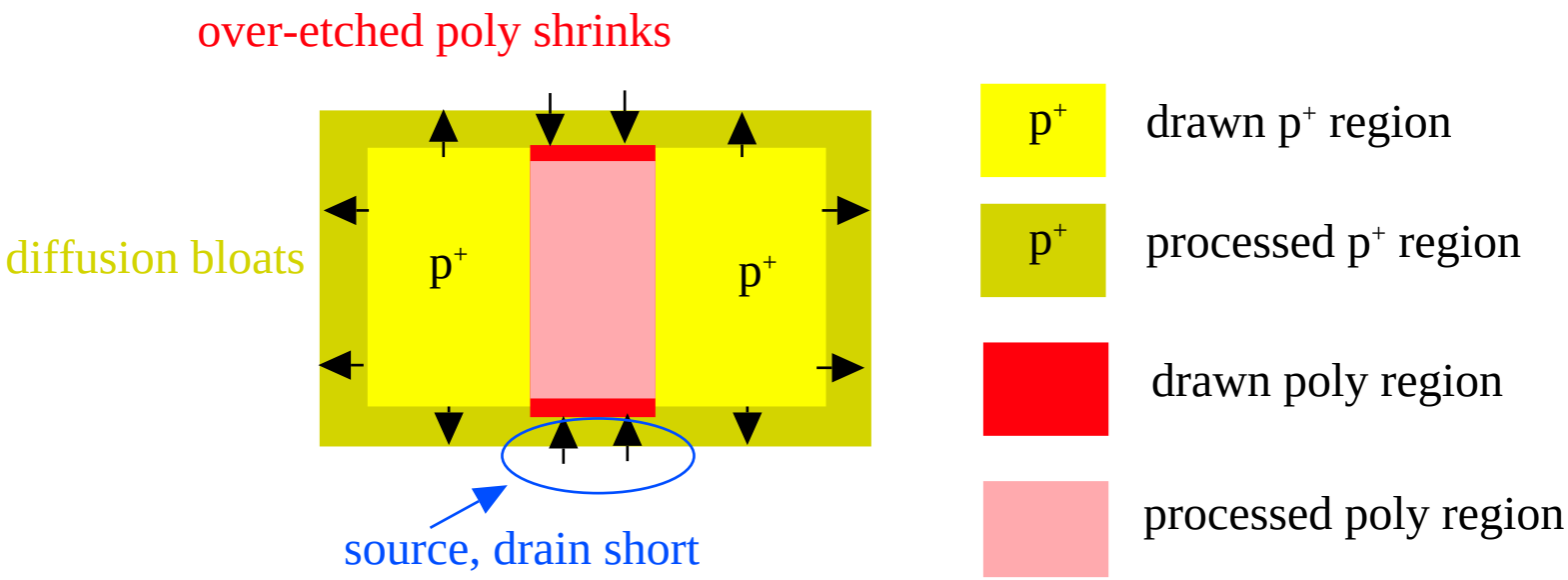
COLOR LEGEND

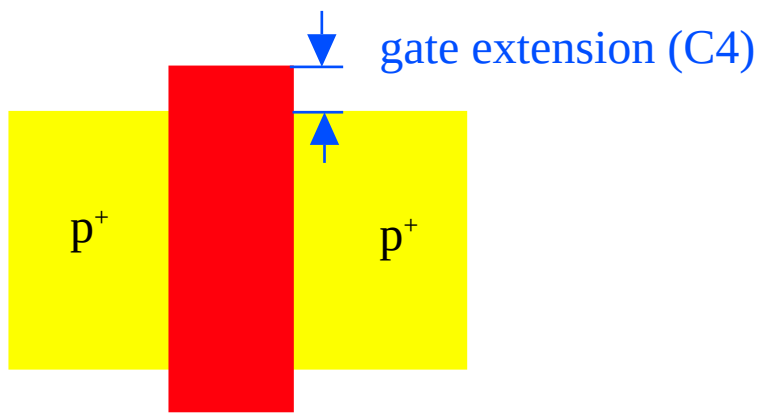
- n-Well
- p-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

E1 = TEXT - R10
E2 = TEXT - R11
E5 = TEXT - R12
E6 = TEXT - R13
E3 = TEXT - R16
E4 = TEXT - R17
E7 = TEXT - R18
E8 = TEXT - R14
E9 = TEXT - R20
E10 = TEXT - R19
F1 = TEXT - R8
F2 = TEXT - R9



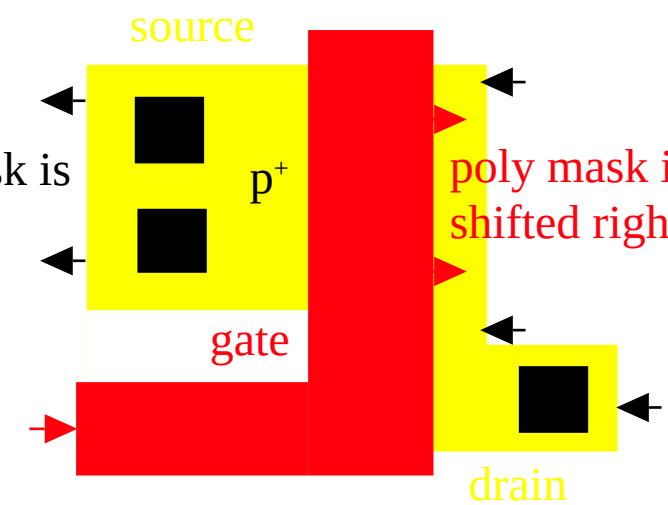
EFFECT OF INSUFFICENT GATE EXTENSION



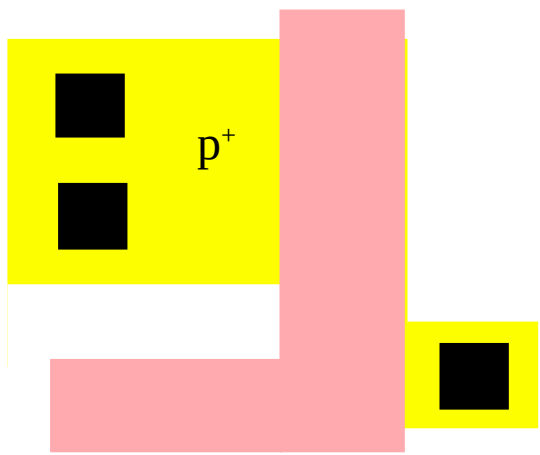


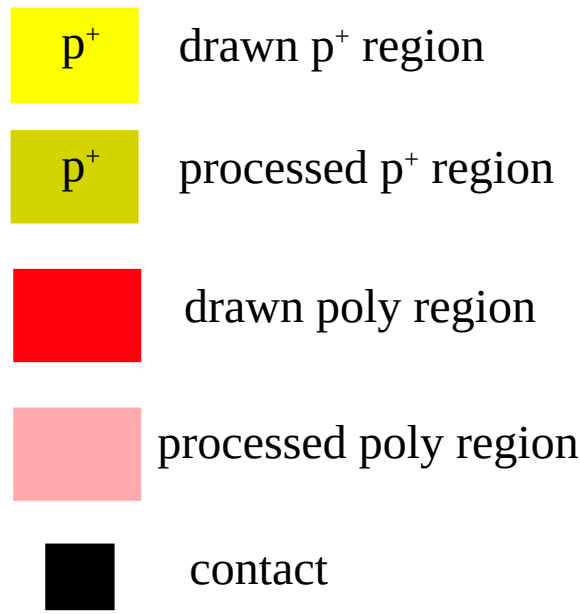
EFFECT OF INSUFFICENT SOURCE-DRAIN EXTENSION

diffusion mask is shifted left



mask misalignment changes width of device and sometimes completely eleminates it.





TECHNOLOGY RELATED CAD ISSUES

TWO BASIC CHECKS MUST BE COMPLETED TO ENSURE THE MASK DATBASE DEVELOPED IN LAYOUT CAN BE TURNED INTO A WORKING CHIP:

a. To verify specified Design Rules have been obeyed

(DESIGN RULE CHECK or DRC)

b. To verify masks produce correct interconnected set of circuit elements

(MASK CIRCUIT-EXTRACTION)

TYPICAL DESIGN FLOW FOR THE PRODUCTION OF AN IC MASK SET