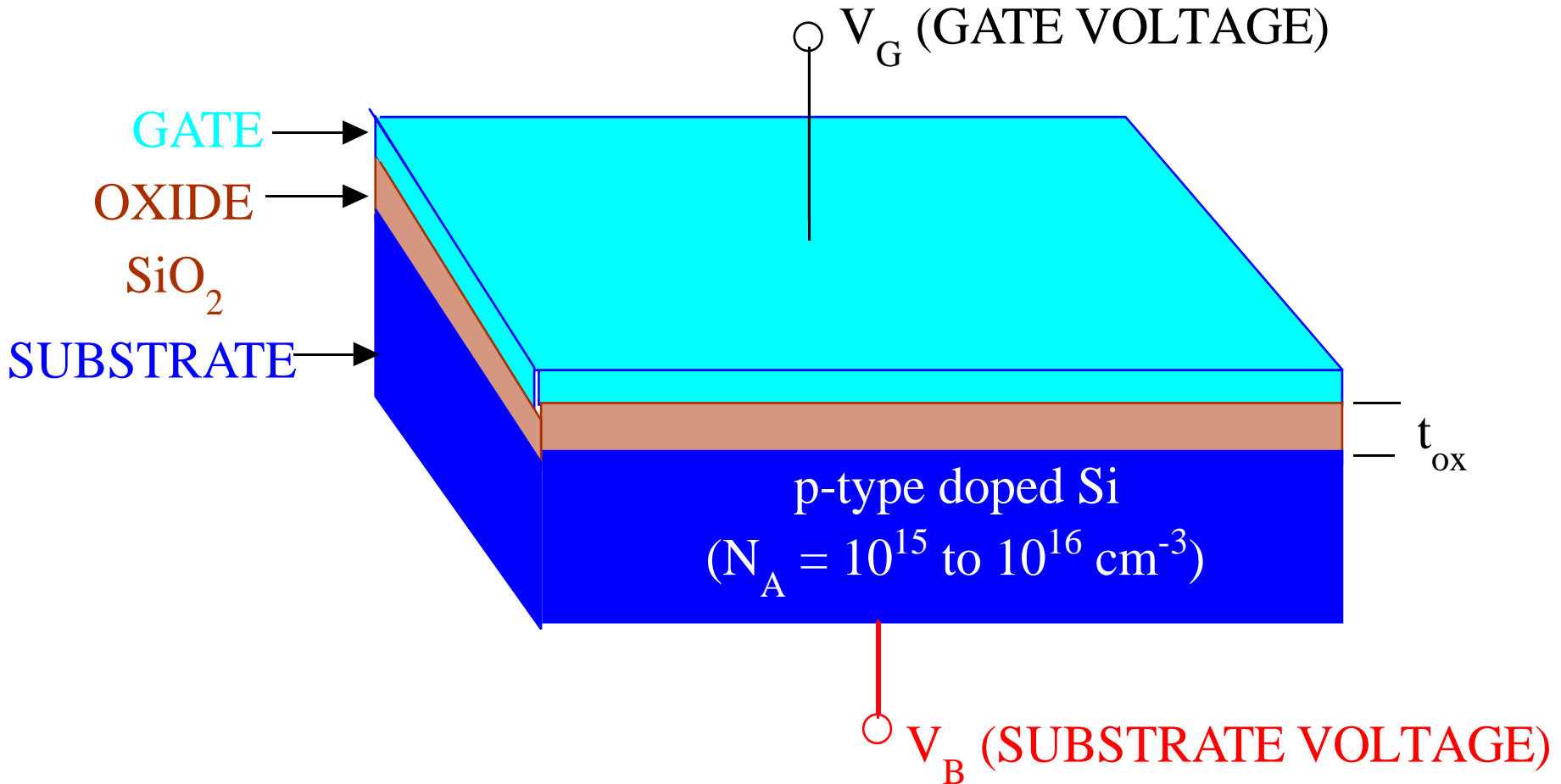


EE 560
MOS TRANSISTOR THEORY
PART 1

TWO TERMINAL MOS STRUCTURE



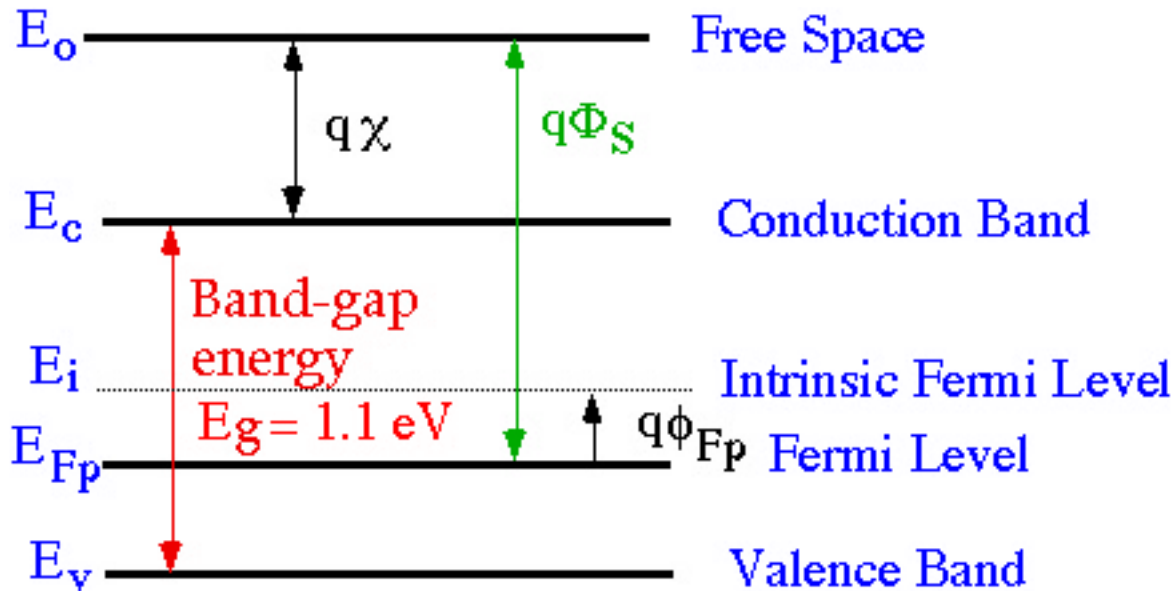
EQUILIBRIUM: $n p = n_i^2$ ($n_i = 1.45 \times 10^{10}$ cm^{-3})

Let SUBSTRATE be uniformly doped @ N_A

$$n_{p0} = \frac{n_i^2}{N_A} \quad \text{and} \quad p_{p0} = N_A$$

(BULK concentrations)

ENERGY BAND DIAGRAM FOR p - TYPE SUBSTRATE



q = electron affinity of Si

$$\phi_F = \frac{E_F - E_i}{q}$$

Work Function

$$q_s = q + (E_c - E_F)$$

$$E_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A} \quad (N_A \gg n_i)$$

$$E_{Fn} = \frac{kT}{q} \ln \frac{N_D}{n_i} \quad (N_D \gg n_i)$$

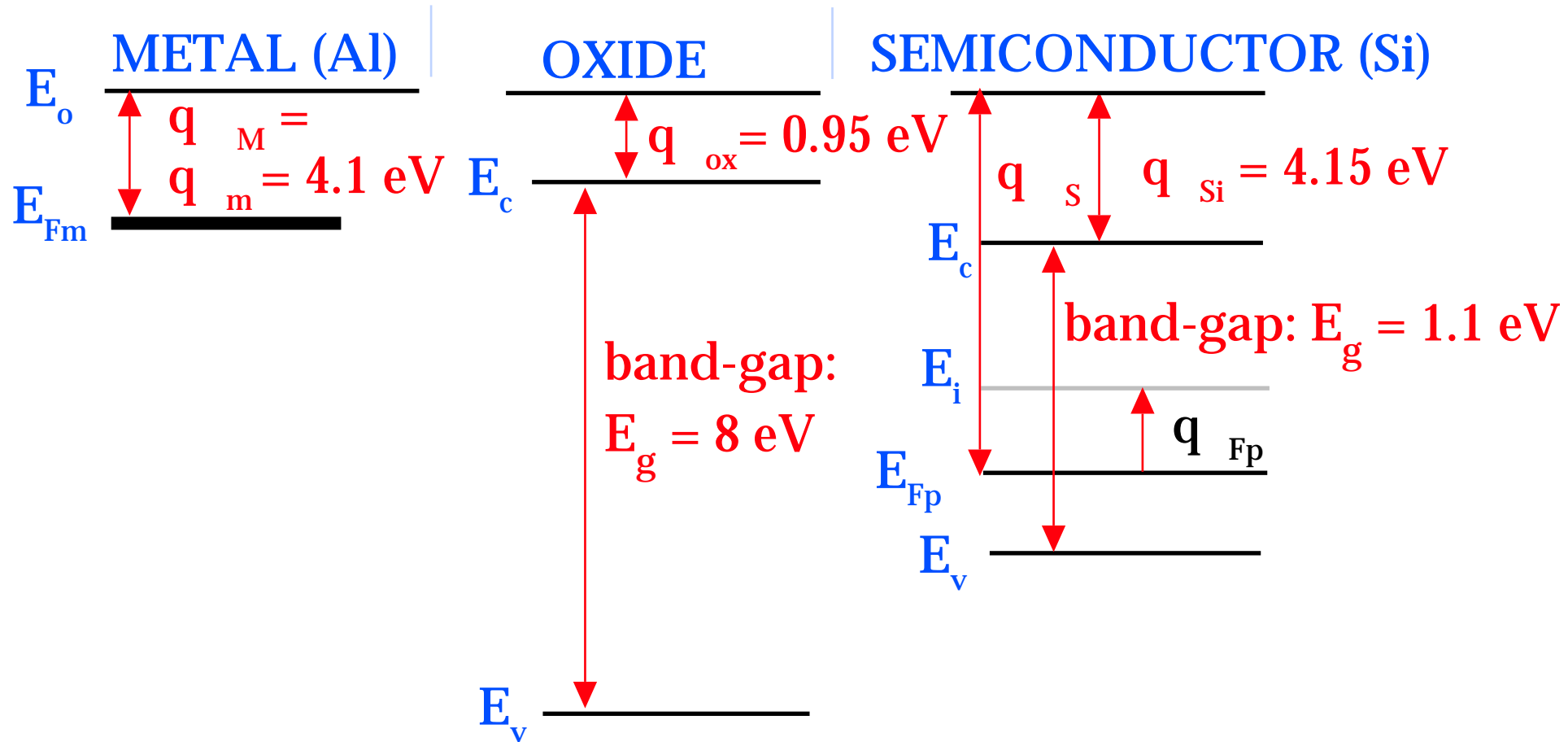
$n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ @ room temp,

$k = 1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$,

$q = 1.6 \times 10^{-19} \text{ C}$

$\Rightarrow kT/q = 26 \text{ mV @ room temp}$

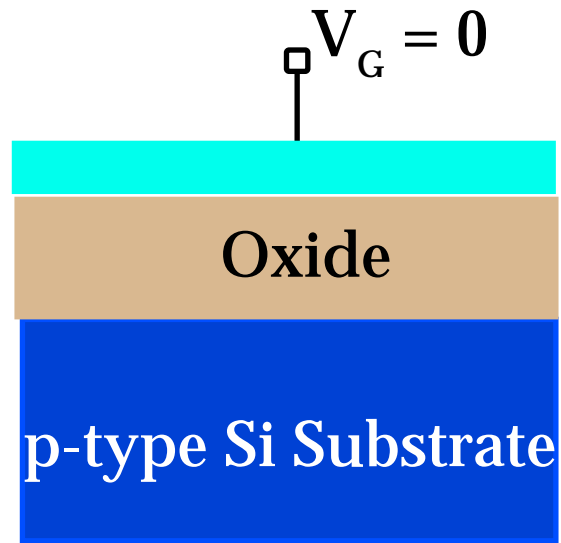
ENERGY BAND DIAGRAMS FOR COMPONENTS OF MOS STRUCTURE



$s > M \Rightarrow \text{p-type Si}$

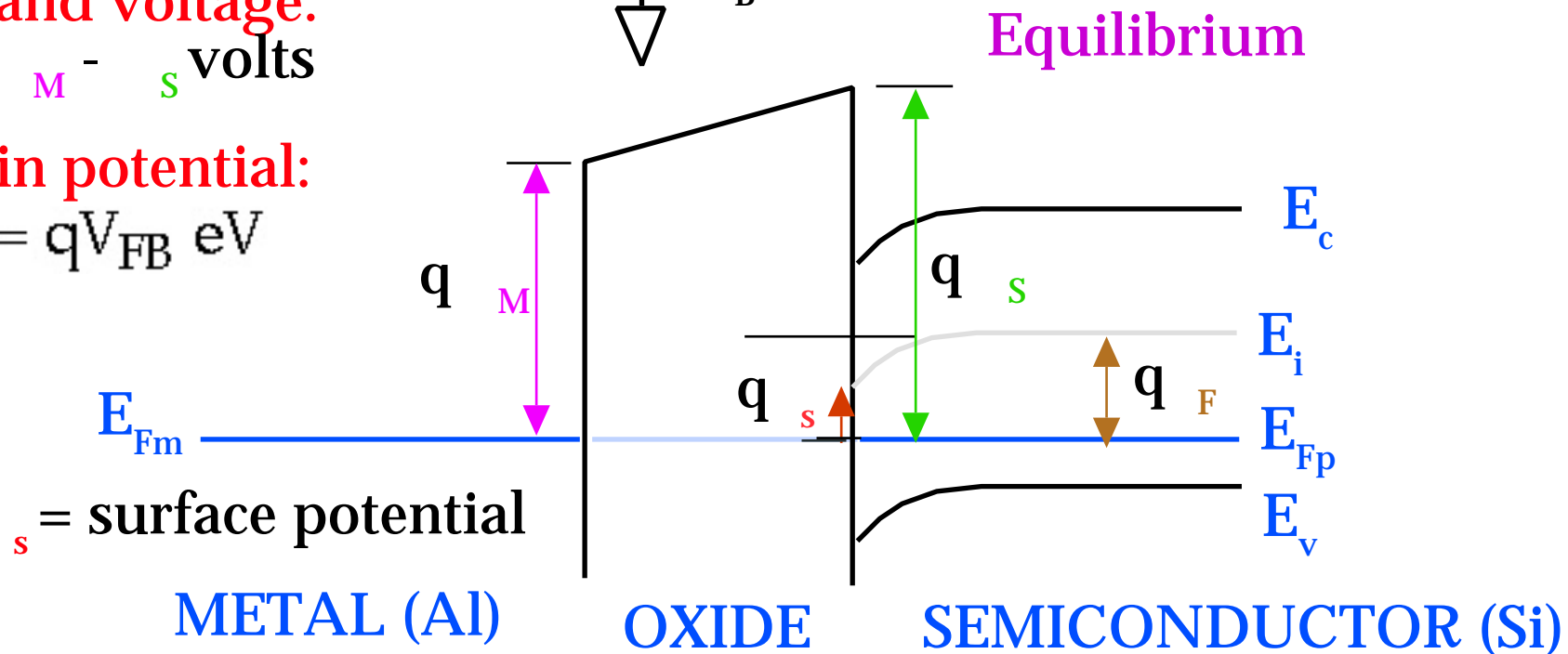
$M > s \Rightarrow \text{n-type Si}$

Equilibrium



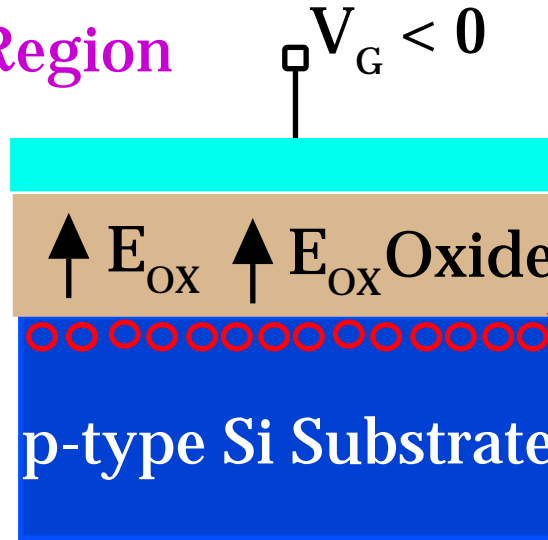
Flat-band voltage:
 $V_{FB} = \phi_M - \phi_s$ volts

Built-in potential:
 $\Phi_{MS} = qV_{FB}$ eV

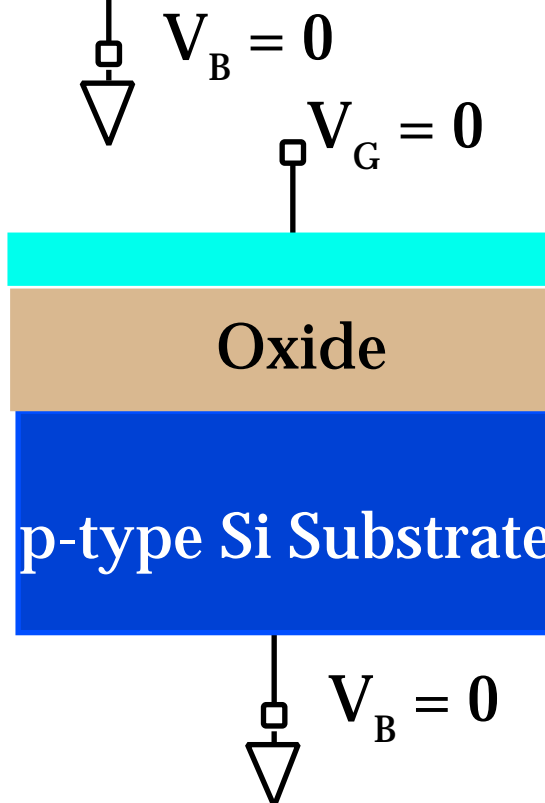


MOS SYSTEM WITH EXTERNAL BIAS

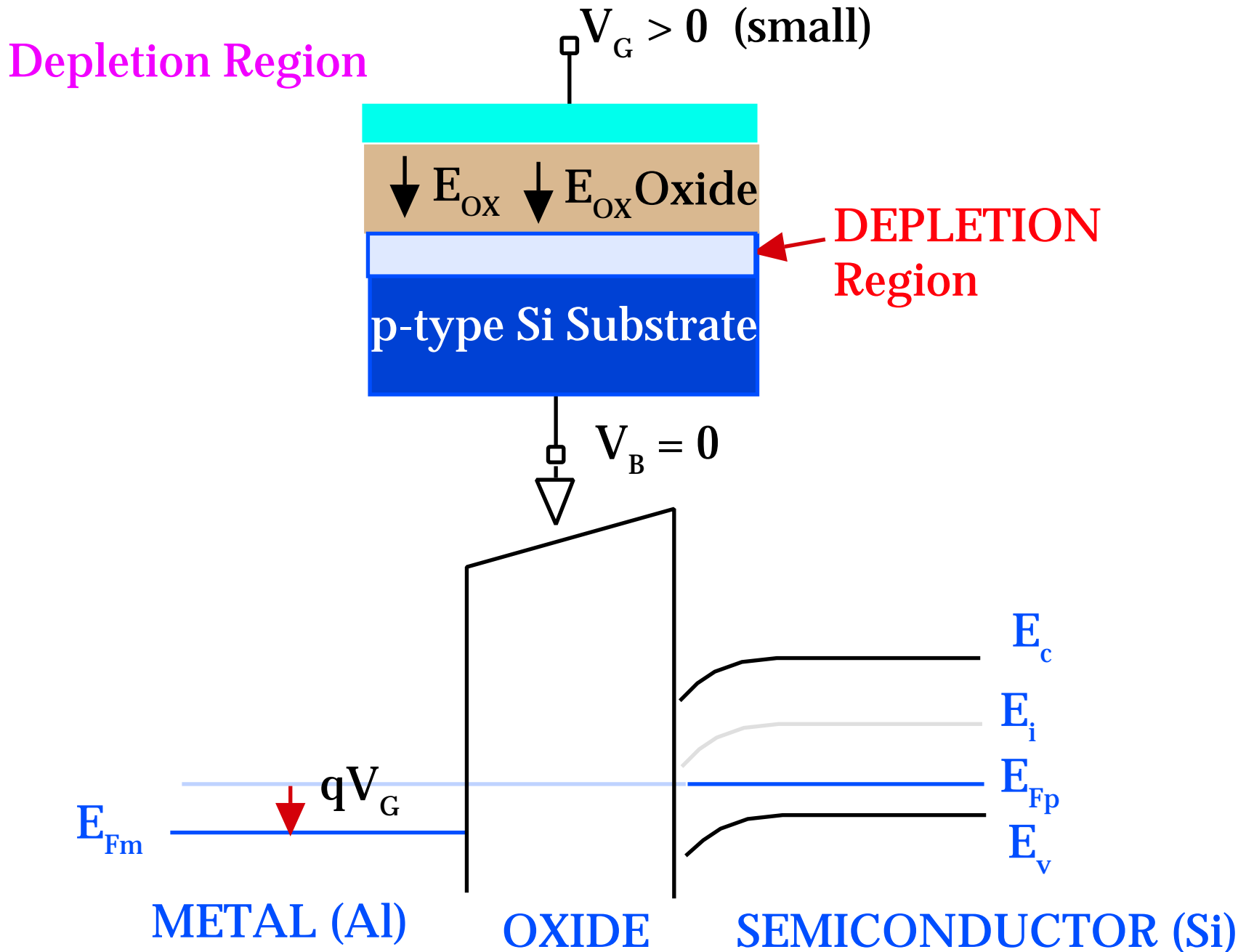
Accumulation Region



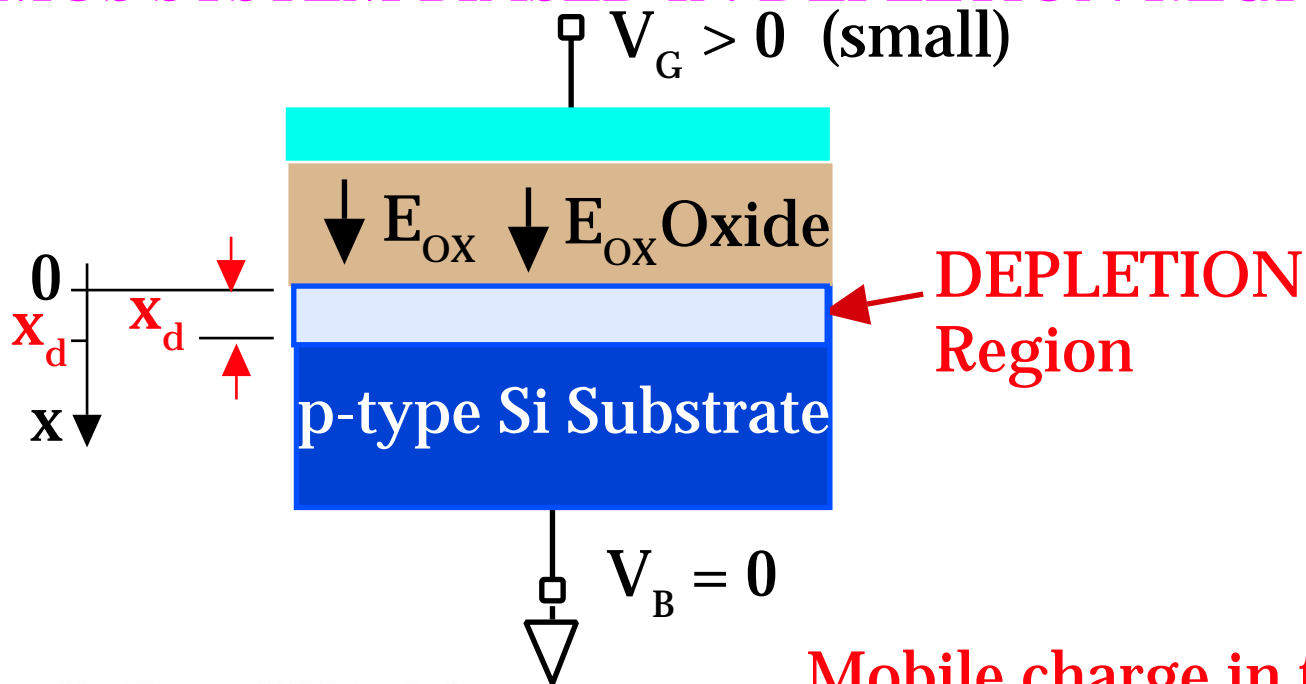
Equilibrium



MOS SYSTEM WITH EXTERNAL BIAS



MOS SYSTEM BIASED IN DEPLETION REGION



$$dQ = -qN_A dx \quad \longrightarrow \quad \text{Mobile charge in thin layer parallel to Si surface}$$

$$d\phi = -\frac{x}{\epsilon_{Si}} dQ = x \frac{qN_A}{\epsilon_{Si}} dx \quad \longrightarrow \quad \text{Change in surface potential to displace } dQ$$

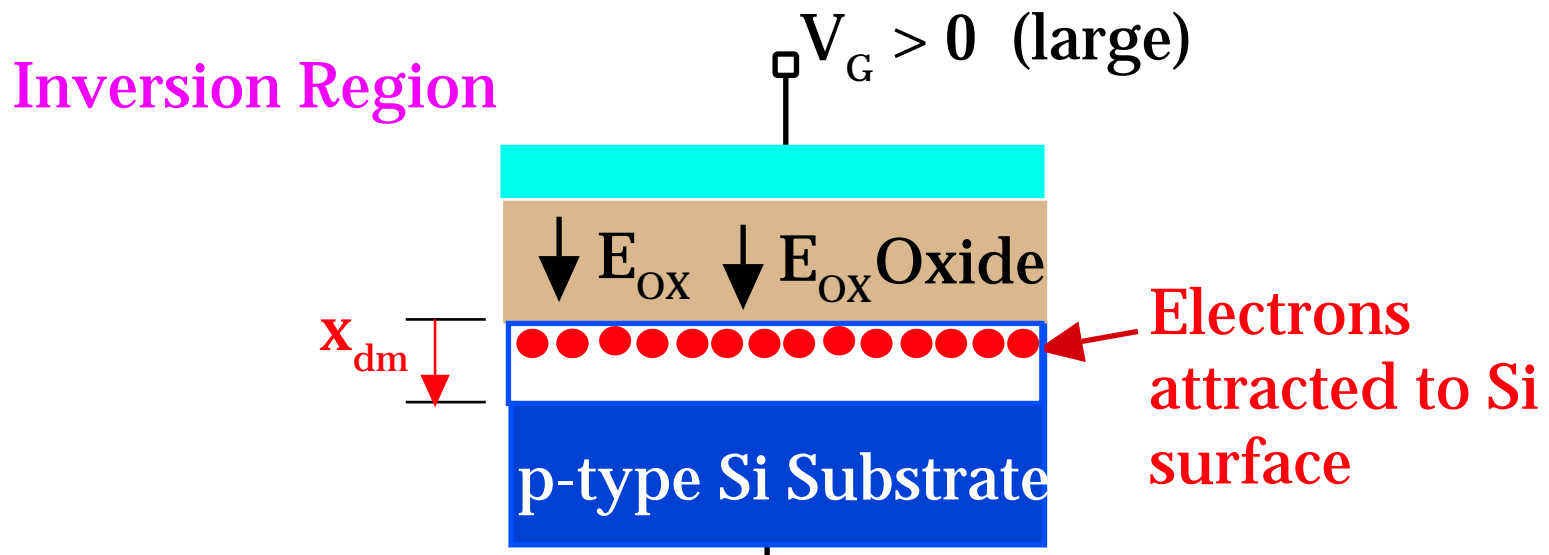
$$\int_{\phi_s}^{\phi_F} d\phi = \int_0^{x_d} x \frac{qN_A}{\epsilon_{Si}} dx \quad \longrightarrow \quad \phi_F - \phi_s = \frac{qN_A}{2\epsilon_{Si}} x_d^2$$

$$x_d = \sqrt{\frac{2\epsilon_{Si}|\phi_F - \phi_s|}{qN_A}}$$

Depletion Region Charge

$$Q = -qN_A x_d = -\sqrt{2qN_A \epsilon_{Si}|\phi_F - \phi_s|}$$

MOS SYSTEM WITH EXTERNAL BIAS

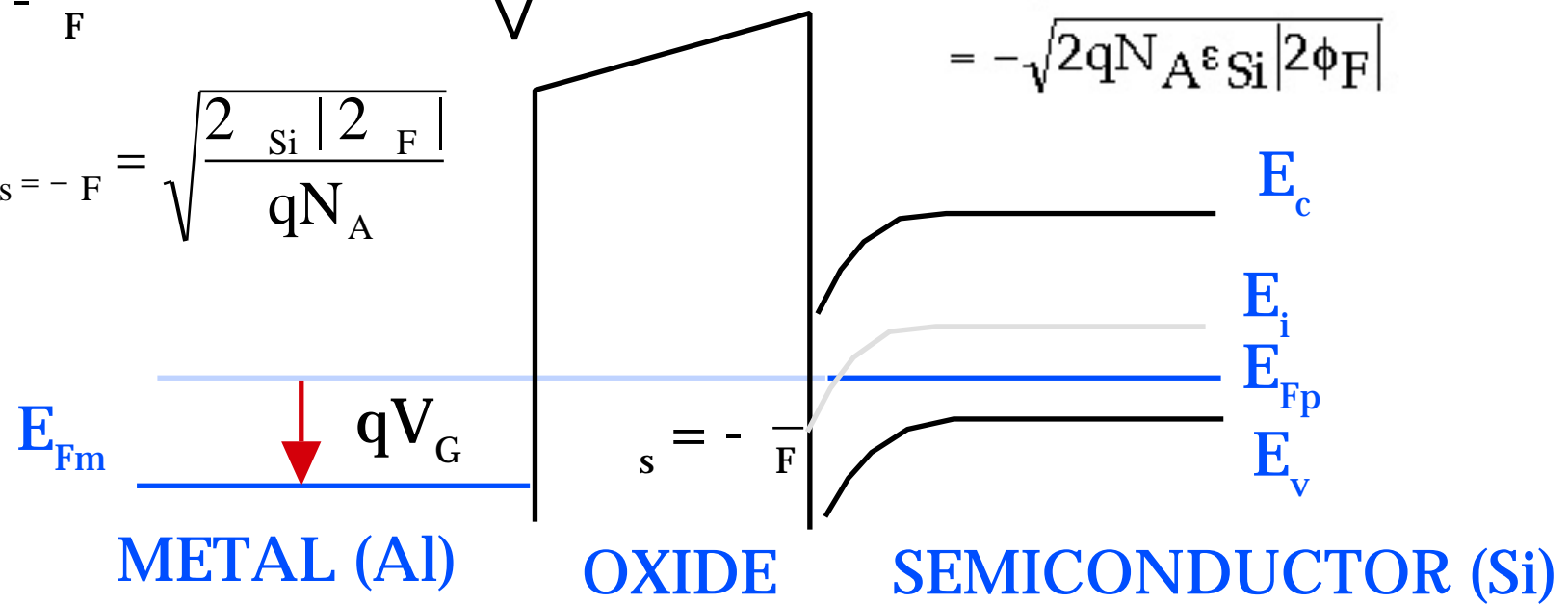


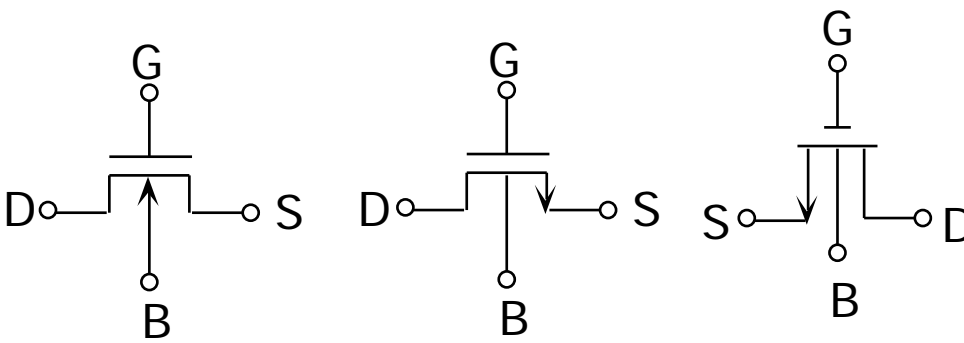
Inversion Condition

$$x_{dm} = x_d \Big|_{s = -F} = \sqrt{\frac{2 \epsilon_{Si} |2 \phi_F|}{q N_A}}$$

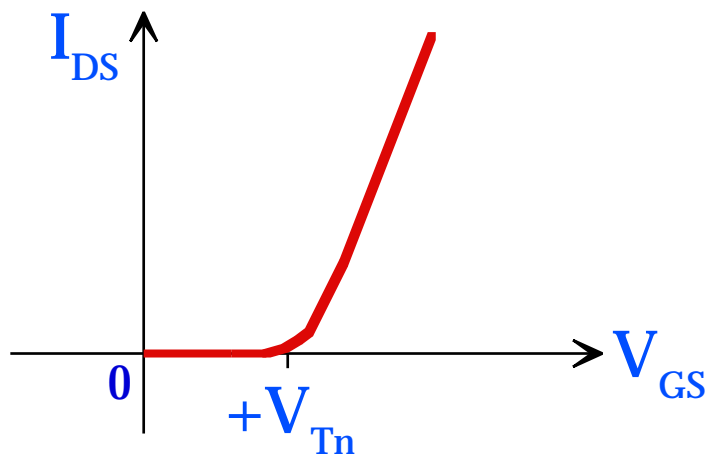
$V_B = 0$

$$Q_{B0} = Q \Big|_{x_{dm} = x_d} - q N_A x_{dm} = -\sqrt{2 q N_A \epsilon_{Si} |2 \phi_F|}$$

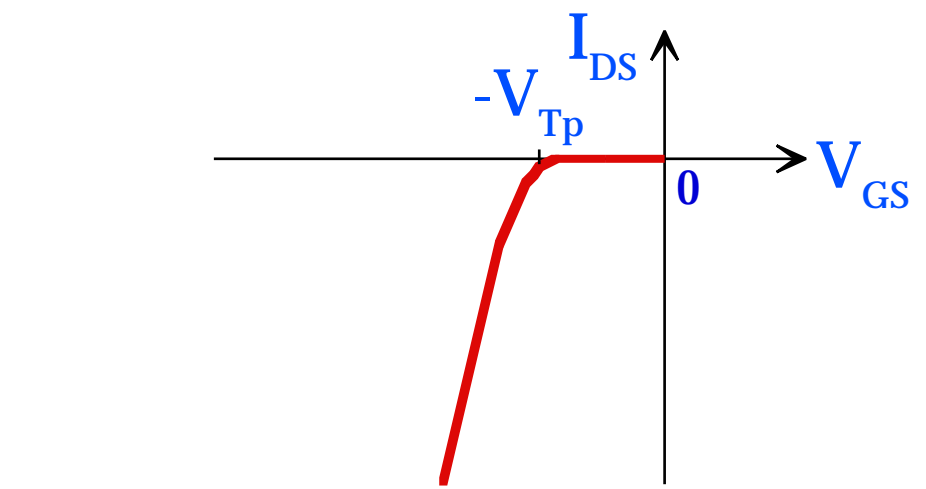




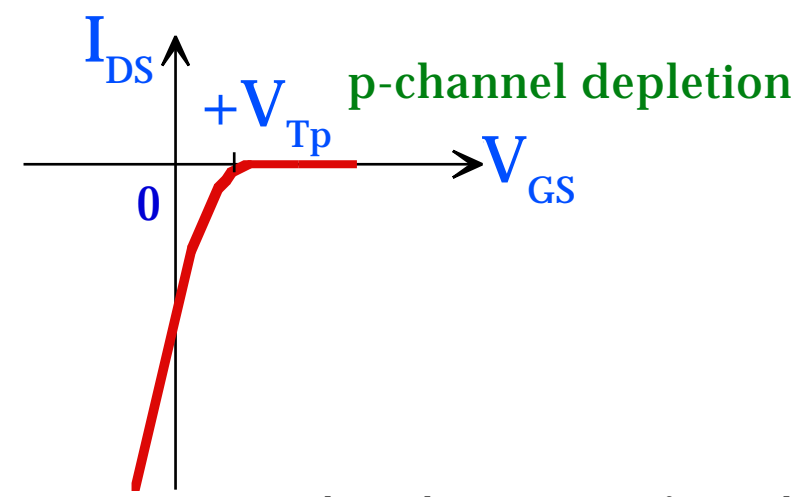
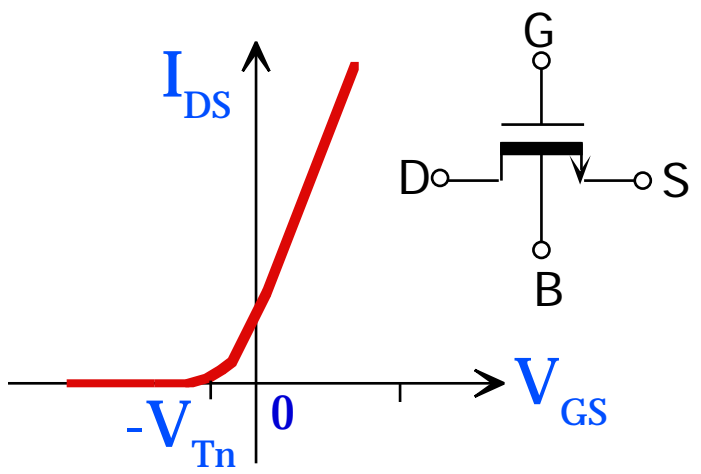
n-channel enhancement

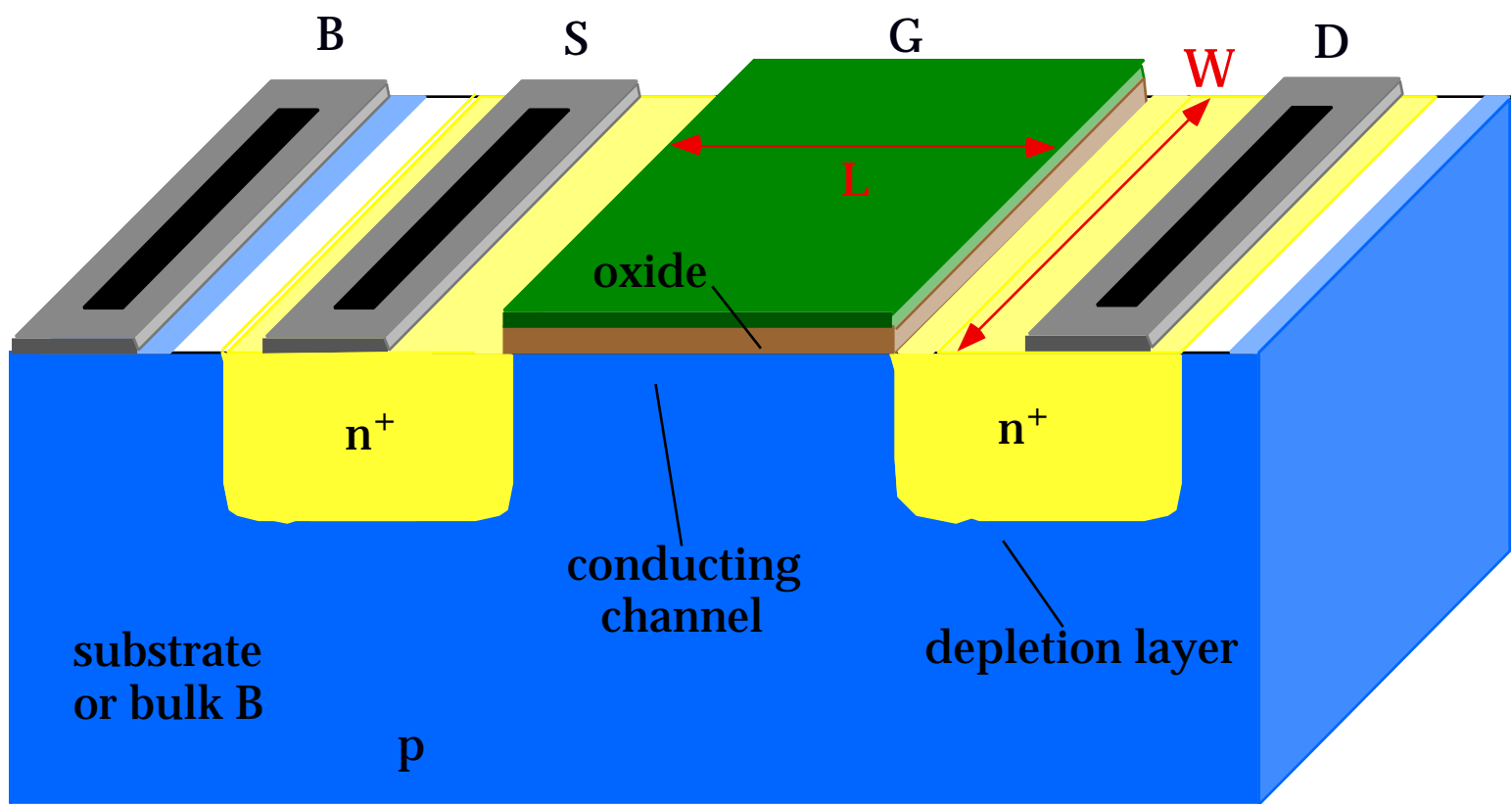


p-channel enhancement

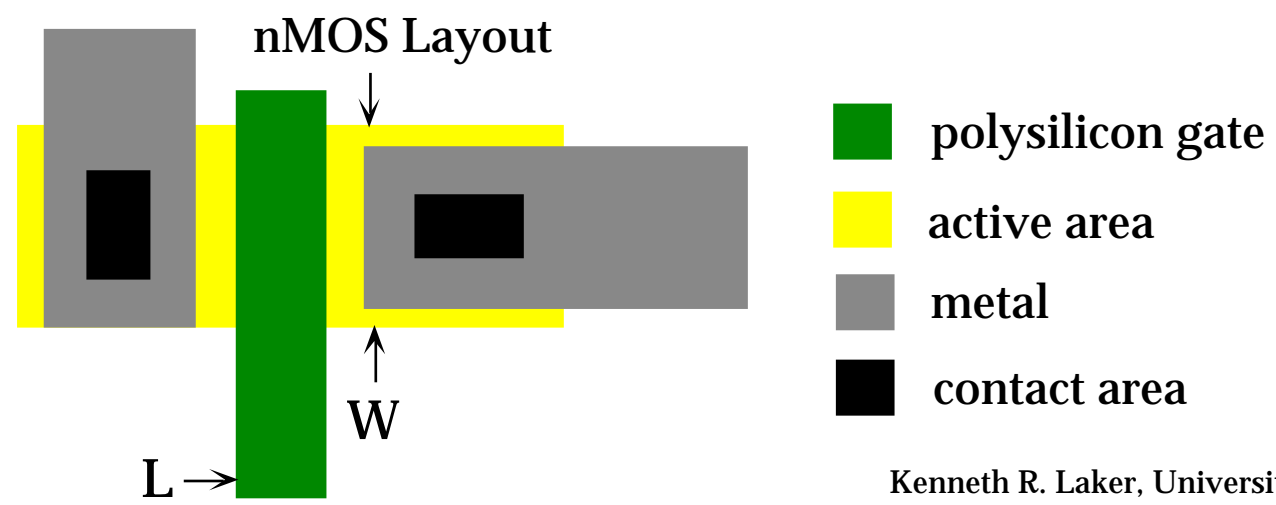


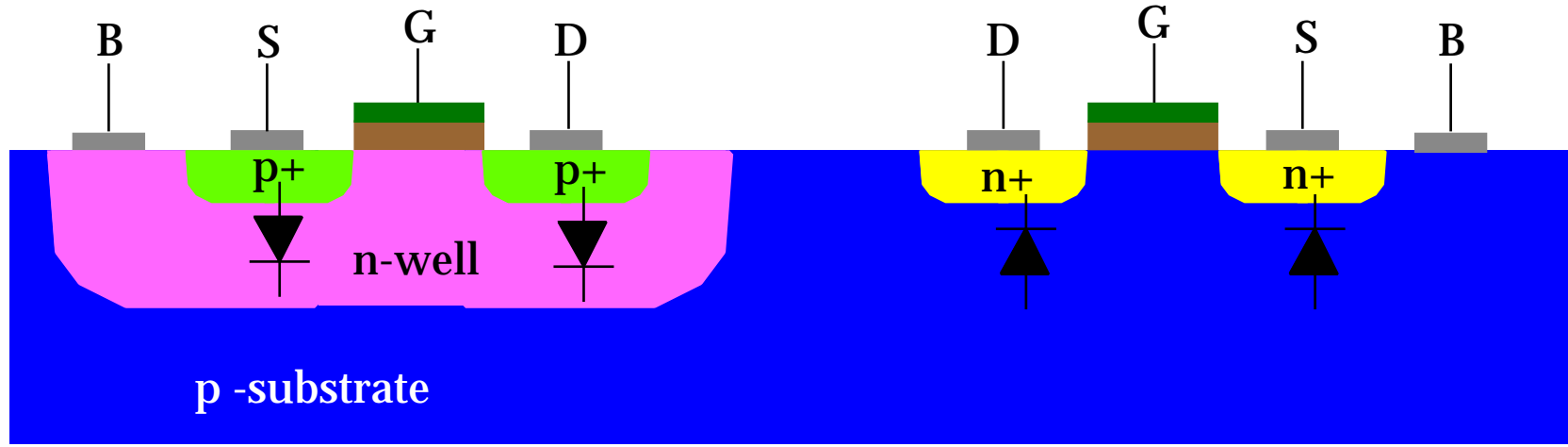
n-channel depletion





N-CHANNEL ENHANCEMENT-TYPE MOSFET

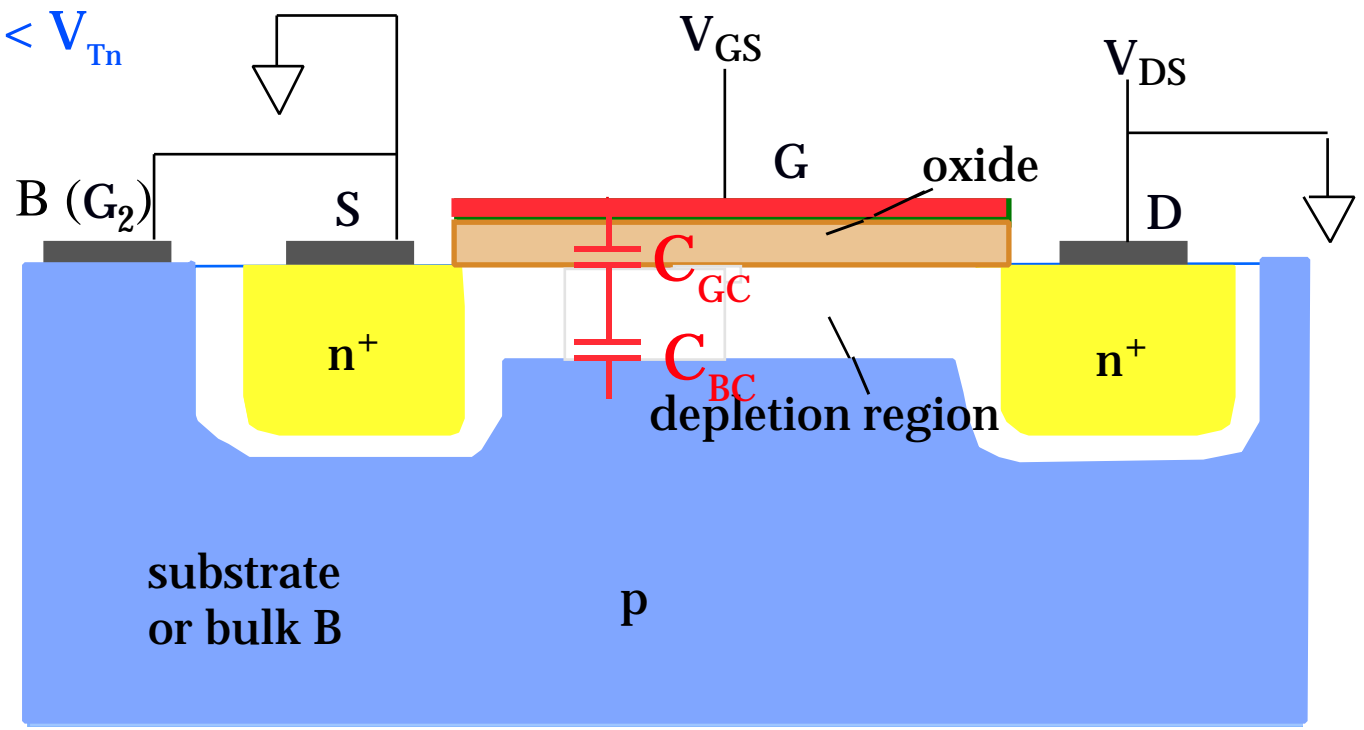




$V_{GS} < V_{Tn}$ → CUT-OFF REGION

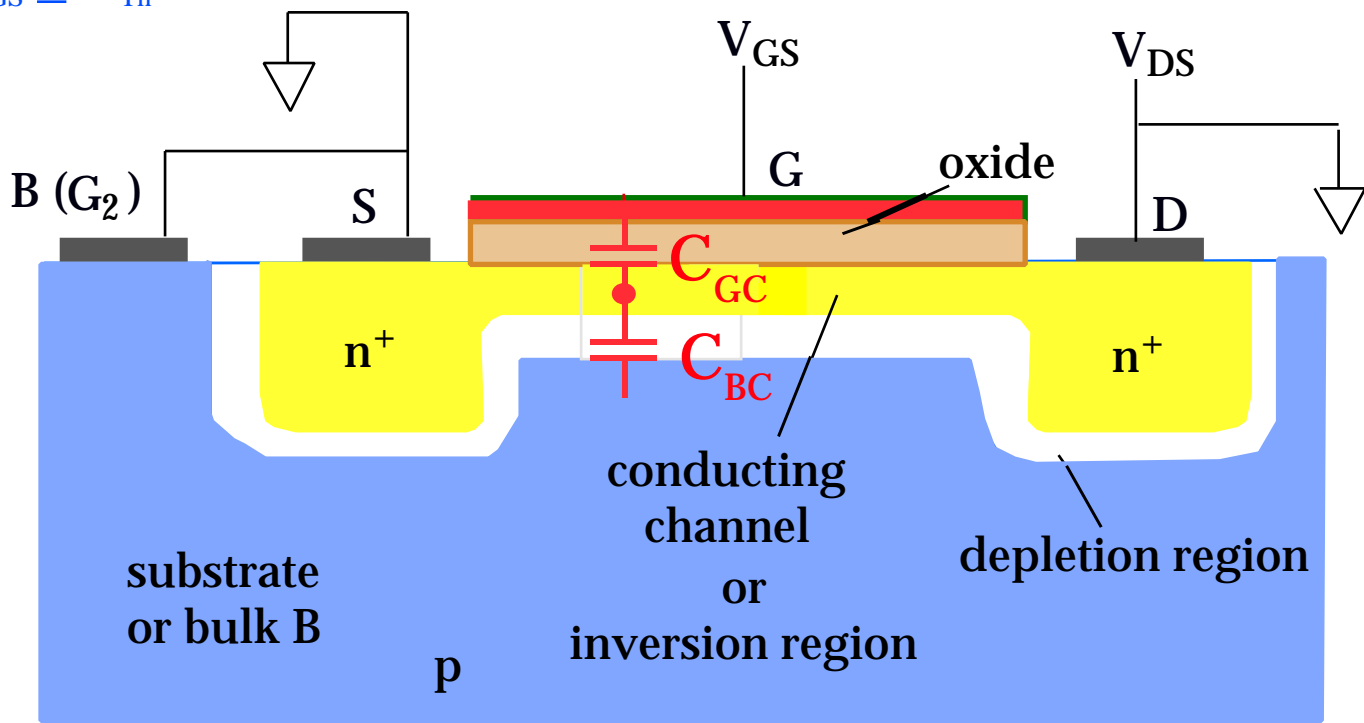
DEPLETION REGION

$0 < V_{GS} < V_{Tn}$



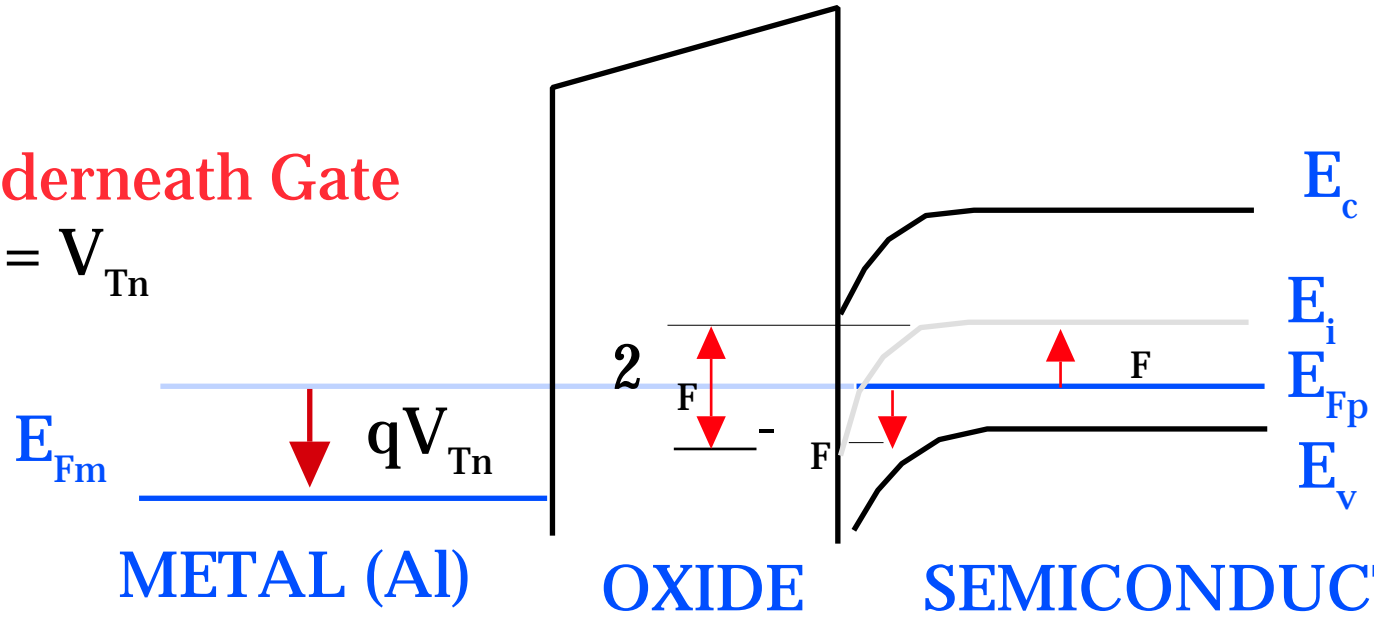
$$V_{GS} \geq V_{Tn}$$

INVERSION REGION



Underneath Gate

$$V_G = V_{Tn}$$



METAL (Al)

OXIDE

SEMICONDUCTOR (Si)

MOS Capacitance $C_{GC} = WLC_{ox}$, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ [t_{ox} -> TOX in SPICE]
[C_{ox} -> COX in SPICE]

$$t_{ox} = 50 \text{ nm}, \quad \epsilon_{ox} = 0.34 \text{ pF/cm} \Rightarrow C_{ox} = 6.8 \times 10^{-8} \text{ F/cm}^2$$

$$W \times L = 50 \text{ } \mu\text{m} \times 50 \text{ } \mu\text{m} \Rightarrow C_{GC} = 170 \text{ fF}$$

Depletion Capacitance $C_{BC} = WLC_j$, $C_j = \frac{\epsilon_{Si}}{x_d}$

$$x_d = \sqrt{\frac{2\epsilon_{Si}|\phi_F - V_{SB}|}{qN_A}} \quad [N_{SUB} \rightarrow NSUB \text{ in SPICE}]$$

N_{SUB} (p - substrate)

$$\phi_F = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

$$N_A = 3 \times 10^{17} \text{ cm}^{-3}, \quad n_i = 1.45 \times 10^{10} \text{ cm}^{-3} \Rightarrow \phi_F = -0.438 \text{ V}$$

(recall that at room temp or 27°C $kT/q = 26 \text{ mV}$)

$$V_{SB} = 0 \text{ V}, \quad \epsilon_{Si} = 1.06 \text{ pF/cm}, \quad q = 1.6 \times 10^{-19} \text{ C}, \quad N_A, \quad \phi_F \Rightarrow x_d = 6.22 \text{ } \mu\text{m}$$

$$\epsilon_{Si}, x_d \Rightarrow C_j = 0.17 \times 10^{-8} \text{ F/cm}^2$$

$$W \times L = 50 \text{ } \mu\text{m} \times 50 \text{ } \mu\text{m} \Rightarrow C_{BC} = 42.5 \text{ fF}$$

Threshold Voltage for MOS Transistors

n-channel enhancement

For $V_{SB} = 0$, the threshold voltage is denoted as V_{T0} or $V_{T0n,p}$ [$V_{T0} \rightarrow VT0$ in SPICE]

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

(+ for nMOS and - for pMOS)

[$2\phi_F = PHI$ in SPICE]

$$Q_{B0} = -\sqrt{2qN_A\epsilon_{Si}|2\phi_F|}$$

[$N_A = NSUB$ in SPICE]

Threshold Voltage factors:

-> Gate conductor material;

-> Gate oxide material & thickness;

-> Channel doping;

-> Impurities in Si-oxide interface;

-> Source-bulk voltage V_{sb} ;

-> Temperature.

$$\phi_{GC} = \phi_F(\text{substrate}) - \phi_M$$

$$\phi_{GC} = \phi_F(\text{substrate}) - \phi_F(\text{gate})$$

metal gate
polysilicon gate

[$Q_{ox} = qNSS$ in SPICE]

Threshold Voltage for MOS Transistors

n-channel enhancement

For $V_{SB} \neq 0$: the threshold voltage is denoted as V_T or $V_{Tn,p}$

$$Q_B = -\sqrt{2qN_A\epsilon_{Si}|2\phi_F - V_{SB}|}$$

$$V_T = V_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$= \underbrace{V_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}}_{V_{T0}} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

where

$$\frac{Q_B - Q_{B0}}{C_{ox}} = \underbrace{\sqrt{\frac{2qN_A\epsilon_{Si}}{C_{ox}}}}_{\gamma} \left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

(γ = Body-effect coefficient) [γ = GAMMA in SPICE]

$$V_{Tn} = V_{T0n} + \gamma \left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

Threshold Voltage for MOS Transistors

n-channel -> p-channel

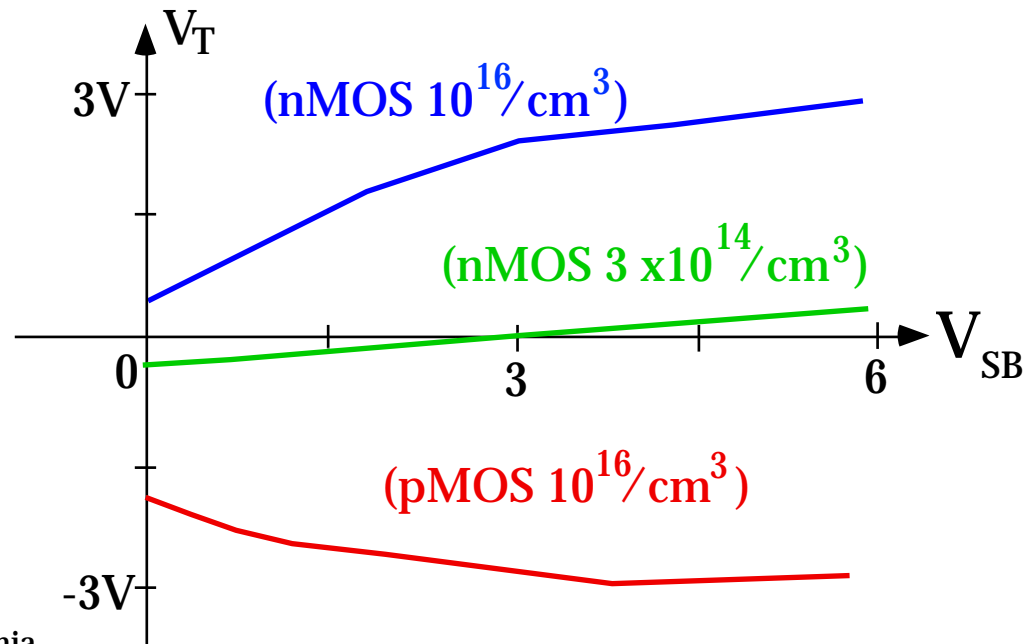
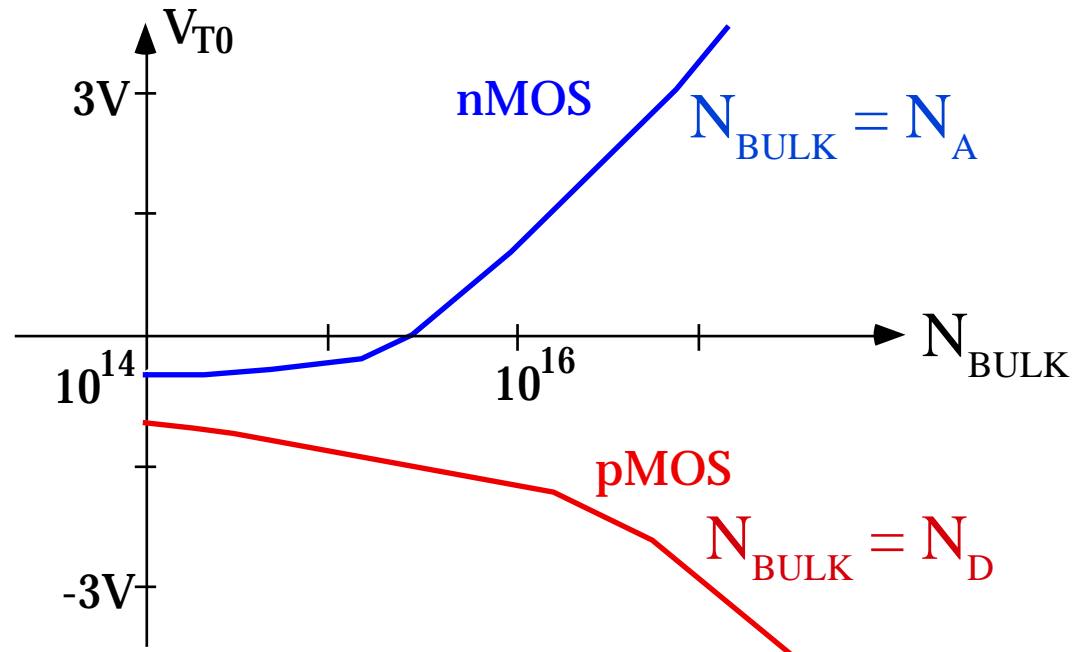
*****BE CAREFULL*** WITH SIGNS**

- V_F is negative in nMOS, positive in pMOS
- Q_{B0} , Q_B are negative in nMOS, positive in pMOS
- V_{GS} is positive in nMOS, negative in pMOS
- V_{SB} is negative in nMOS, positive in pMOS

NOTE:

$$\frac{C_{BC}}{C_{GC}}$$

Threshold Voltage for MOS Transistors



EXAMPLE 3.2 Calculate the threshold voltage V_{T0} at $V_{BS} = 0$, for a polysilicon gate n-channel MOS transistor with the following parameters:

substrate doping density $N_A = 10^{16} \text{ cm}^{-3}$,
 polysilicon doping density $N_D = 2 \times 10^{20} \text{ cm}^{-3}$,
 gate oxide thickness $t_{ox} = 500 \text{ Angstroms}$,
 oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10} \text{ cm}^{-2}$.

$$\longrightarrow V_{T0} = \underbrace{GC}_{F(\text{sub})} - 2 \underbrace{F(\text{sub})}_{GC} - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \longleftarrow$$

$F(\text{sub})$, GC

$$GC = F(\text{sub}) - F(\text{gate})$$

$$F(\text{sub}) = \frac{kT}{q} \ln \frac{n_i}{N_A} = 0.026 \text{ V} \ln \frac{1.45 \times 10^{10}}{10^{16}} = -0.35 \text{ V}$$

$$F(\text{gate}) = \frac{kT}{q} \ln \frac{N_D}{n_i} = 0.026 \text{ V} \ln \frac{2 \times 10^{20}}{1.45 \times 10^{10}} = 0.60 \text{ V}$$

$$GC = F(\text{sub}) - F(\text{gate}) = -0.35 \text{ V} - 0.60 \text{ V} = -0.95 \text{ V}$$

EXAMPLE 3-2 CONT.

$$V_{T0} = V_{GC} - 2 \phi_{F(\text{sub})} - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

 Q_{B0} :

$$\begin{aligned} Q_{B0} &= -\sqrt{2qN_A \epsilon_{Si} |2\phi_{F(\text{sub})}|} \\ &= -\sqrt{2(1.6 \times 10^{-19} \text{ C})(10^{16} \text{ cm}^{-3})(1.06 \times 10^{-12} \text{ Fcm}^{-1}) |2 \times 0.35 \text{ V}|} \\ &= -4.87 \times 10^{-8} \text{ C/cm}^2 \end{aligned}$$

$F = C/V$

 C_{ox} :

$$C_{ox} = \frac{Q_{ox}}{t_{ox}} = \frac{0.34 \times 10^{-12} \text{ Fcm}^{-1}}{500 \times 10^{-8} \text{ cm}} = 6.8 \times 10^8 \text{ F/cm}^2$$

 Q_{ox} :

$$Q_{ox} = qN_{ox} = (1.6 \times 10^{-19} \text{ C})(4 \times 10^{10} \text{ cm}^{-2}) = 6.4 \times 10^{-9} \text{ C/cm}^2$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-4.87 \times 10^{-8} \text{ C/cm}^2}{6.8 \times 10^8 \text{ F/cm}^2} = -0.716 \text{ V} \quad \frac{Q_{ox}}{C_{ox}} = \frac{6.4 \times 10^{-9} \text{ C/cm}^2}{6.8 \times 10^8 \text{ F/cm}^2} = 0.094 \text{ V}$$

$$V_{T0} = -0.95 \text{ V} - (-0.70 \text{ V}) - (-0.72 \text{ V}) - (0.09 \text{ V}) = 0.38 \text{ V}$$

EXAMPLE 3.3 Consider the n-channel MOS transistor with the following process parameters:

substrate doping density $N_A = 10^{16} \text{ cm}^{-3}$,

polysilicon doping density $N_D = 2 \times 10^{20} \text{ cm}^{-3}$,

gate oxide thickness $t_{\text{ox}} = 500 \text{ Angstroms}$,

oxide-interface fixed charge density $N_{\text{ox}} = 4 \times 10^{10} \text{ cm}^{-2}$.

In digital circuit design, the condition $V_{\text{SB}} = 0$ can not always be quaranteed for all transistors. Plot the threshold voltage V_T as a function of V_{SB} .

$$\longrightarrow \quad V_T = V_{T0} + \gamma \left(\sqrt{|2\phi_F - V_{\text{SB}}|} - \sqrt{|2\phi_F|} \right) \quad \longleftarrow$$

- Body-effect coefficient:

$$F = C/V$$

$$= \frac{\sqrt{2qN_A e_{\text{Si}}}}{C_{\text{ox}}} = \frac{\sqrt{2(1.6 \times 10^{-19} \text{ C})(10^{16} \text{ cm}^{-3})(1.06 \times 10^{-12} \text{ Fcm}^{-1})}}{6.8 \times 10^8 \text{ F/cm}^2}$$

$$= \frac{5.824 \times 10^{-8} \text{ C/V}^{-1/2} \text{ cm}^2}{6.8 \times 10^8 \text{ C/Vcm}^2} = 0.85 \text{ V}^{1/2}$$

EXAMPLE 3-3 CONT.

$$V_T = V_{T0} + \gamma \left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

where

$$\begin{aligned} V_{T0} &= 0.38 \text{ V} \quad (\text{from EX 3-2}) \\ &= 0.85 \text{ V}^{1/2} \end{aligned}$$

