MT-027: ADC Architectures VIII: Integrating ADCs

by Walt Kester and James Bryant
Rev. 0, 02-13-06

INTRODUCTION

Soon after the discovery of the basic counting ADC architectures (see Tutorial MT-026) it was realized that much greater accuracy could be obtained using a combination of integrating and counting techniques. This led to the development of high accuracy dual-slope, triple-slope, and quad-slope ADCs. Although the proliferation of high resolution sigma-delta ADCs has made integrating architectures somewhat less popular, they are still used in a variety of precision applications such as digital voltmeters, etc.

MULTI-SLOPE ADCs

Introduced in the 1950s, the "dual-slope" ADC architecture was truly a breakthrough in ADCs for high resolution applications such as digital voltmeters, etc. (see References 1-4). A simplified diagram is shown in Figure 1, and the integrator output waveforms are shown in Figure 2.

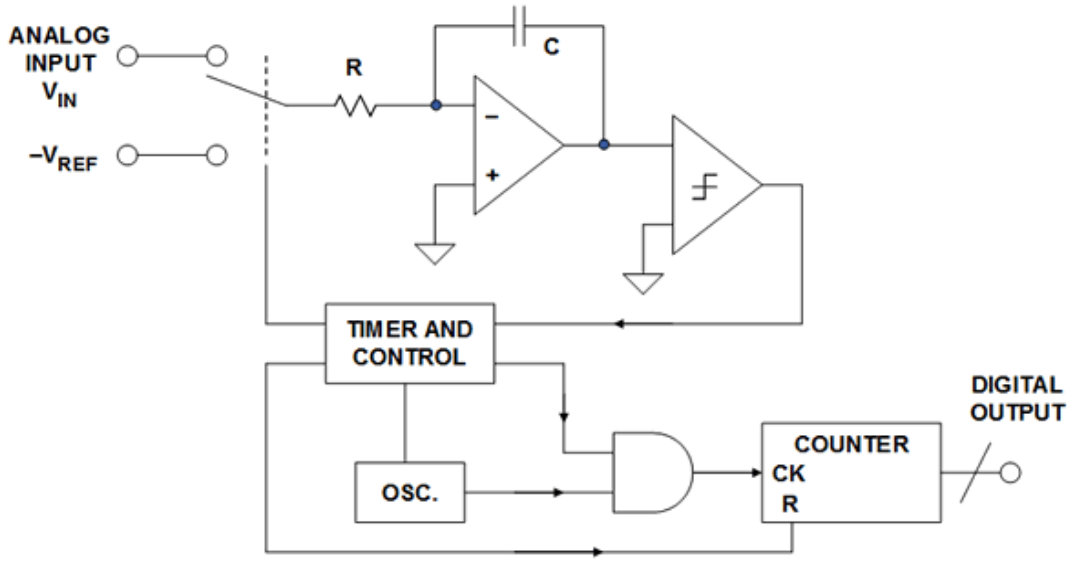

Figure 1: Dual Slope Integrating ADC

The input signal is applied to an integrator; at the same time a counter is started, counting clock pulses. After a pre-determined amount of time (T), a reference voltage having opposite polarity is applied to the integrator. At that instant, the accumulated charge on the integrating capacitor is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having a slope of V_{REF}/RC. At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to $V_{IN} \times T$, and the equal amount of charge lost is proportional to $V_{REF} \times t_x$, then the number of counts relative to the full scale count is proportional to t_x/T, or V_{IN}/V_{REF}. If the output of the counter is a binary number, it will therefore be a binary representation of the input voltage.

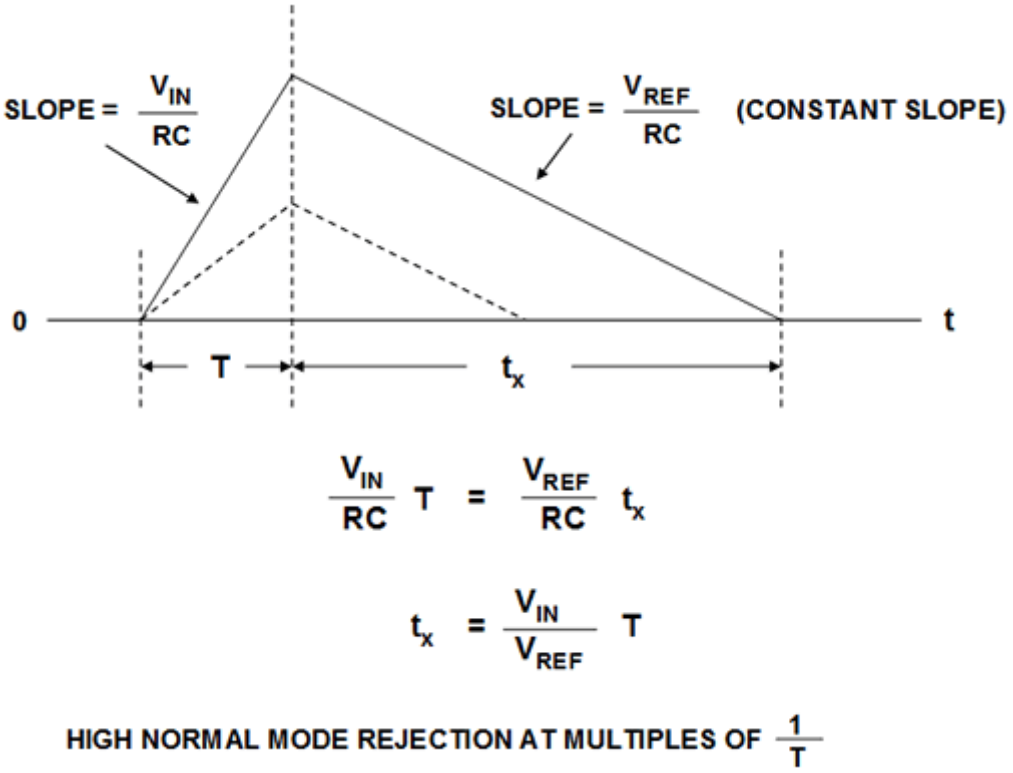

Figure 2: Dual Slope ADC Integrator Output Waveforms

Dual-slope integration has many advantages. Conversion accuracy is independent of both the capacitance and the clock frequency, because they affect both the up-slope and the down-slope by the same ratio.

The fixed input signal integration period results in rejection of noise frequencies on the analog input that have periods that are equal to or a sub-multiple of the integration time T. Proper choice of T can therefore result in excellent rejection of 50-Hz and 60-Hz line ripple as shown in Figure 3.

Errors caused by bias currents and the offset voltages of the integrating amplifier and the comparator as well as gain errors can be cancelled by using additional charge/discharge cycles to measure "zero" and "full-scale" and using the results to digitally correct the initial measurement, as in the *quad-slope* architecture discussed in Reference 5.

The *triple-slope* architecture (see References 6-8) retains the advantages of the dual-slope, but greatly increases the conversion speed at the cost of added complexity. The increase in conversion speed is achieved by accomplishing the reference integration (ramp-down) at two distinct rates: a high-speed rate, and a "vernier" lower speed rate. The counter is likewise divided into two sections, one for the MSBs and one for the LSBs. In a properly designed triple-slope converter, a significant increase in speed can be achieved while retaining the inherent linearity, differential linearity, and stability characteristics associated with dual-slope ADCs.

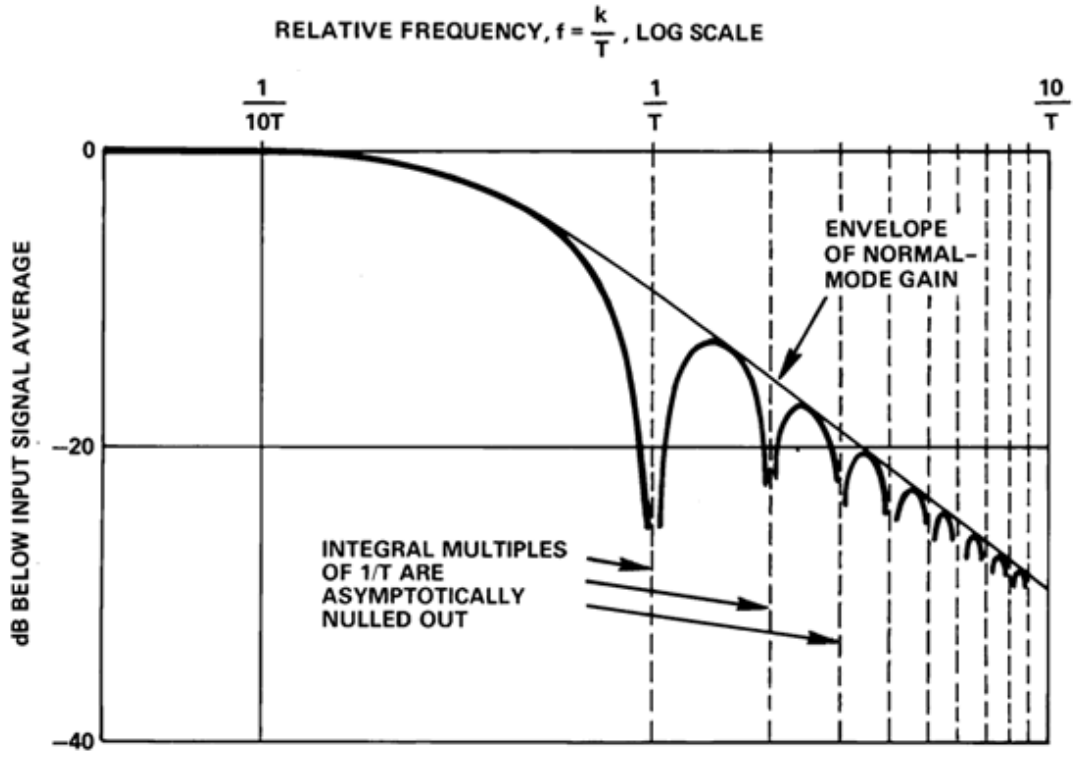

Figure 3: Frequency Response of Integrating ADC

REFERENCES

1. Robin N. Anderson and Howard A. Dorey, "Digital Voltmeters," **U.S. Patent 3,267,458,** filed August 20, 1962, issued August 16, 1966. *(charge balance dual slope voltmeter ADC).*

2. Richard Olshausen, "Analog-to-Digital Converter," **U.S. Patent 3,281,827,** filed June 27, 1963, issued October 25, 1966. *(charge balance dual slope ADC).*

3. Roswell W. Gilbert, "Analog-to-Digital Converter," **U.S. Patent 3,051,939,** filed May 8, 1957, issued August 28, 1962. *(dual-slope ADC).*

4. Stephan K. Ammann, "Integrating Analog-to-Digital Converter," **U.S. Patent 3,316,547,** filed July 15, 1964, issued April 25, 1967. *(dual-slope ADC).*

5. Ivar Wold, "Integrating Analog-to-Digital Converter Having Digitally-Derived Offset Error Compensation and Bipolar Operation without Zero Discontinuity," **U.S. Patent 3,872,466,** filed July 19, 1973, issued March 18, 1975. *(quad-slope ADC).*

6. Hans Bent Aasnaes, "Triple Integrating Ramp Analog-to-Digital Converter," **U.S. Patent 3,577,140,** filed June 27, 1967, issued May 4,

1971. *(triple-slope ADC).*

7. Frederick Bondzeit, Lewis J. Neelands, "Multiple Slope Analog-to-Digital Converter," **U.S. Patent 3,564,538,** filed January 29, 1968, issued February 16, 1971. *(triple-slope ADC).*

8. Desmond Wheable, "Triple-Slope Analog-to-Digital Converters," **U.S. Patent 3,678,506,** filed October 2, 1968, issued July 18, 1972. *(triple-slope ADC).*