University of Illinois at Urbana-Champaign
Digital Electronics Laboratory

Physics Department
Physics 405 Laboratory

Experiment 3: CMOS Digital Logic

1. Introduction

The purpose of this lab is to continue our investigation of various types (i.e. families) and kinds of logic circuits, and moving further towards highly-integrated circuit chips that carry out several functions.

2. Special Handling Requirements For CMOS Logic Circuits:

Examples of Complementary Metal Oxide Semiconductor (CMOS) logic circuits are the CD 4007 dual complementary pair, the CD 4011 quadruple 2–input NAND gate and the CD 4016 quad bilateral switch, as shown below in Figures 1a –1c.

When using CMOS IC's, it is very important to keep in mind that MOSFET's have extremely high input impedance (typically 10^{12} Ω), and because of this, they can be very easily destroyed by the application of excessive voltages to the gate and/or discharges of static electricity! Please read the precautions listed under "Operating considerations" in the manufacturer's specifications and follow the rules carefully.

The input voltage requirement: $V_{SS} \leq V_I \leq V_{DD}$ ***must*** be strictly adhered to at **ALL** times - i.e. V_{DD} = +5 Volts must ***never*** be turned off while a (positive) input voltage, V_I is applied to any input. You ***must*** connect **all unused inputs** either to V_{DD} = +5V, or to V_{SS} = 0V (i.e. ground). In order to minimize capacitive pick–up, it is wise/good practice to also connect the *ground plate* of the breadboard to V_{SS} = 0 volts.

For more information on CMOS logic, refer e.g. to the RCA Solid State Data Book SSD–203C, COS/MOS Digital Integrated Circuits; CMOS Integrated Circuits, National; Section 4–CMOS of Fairchild MOS/CCD Data Book; Motorola Semiconductor Library Vol. 5 CMOS, etc.

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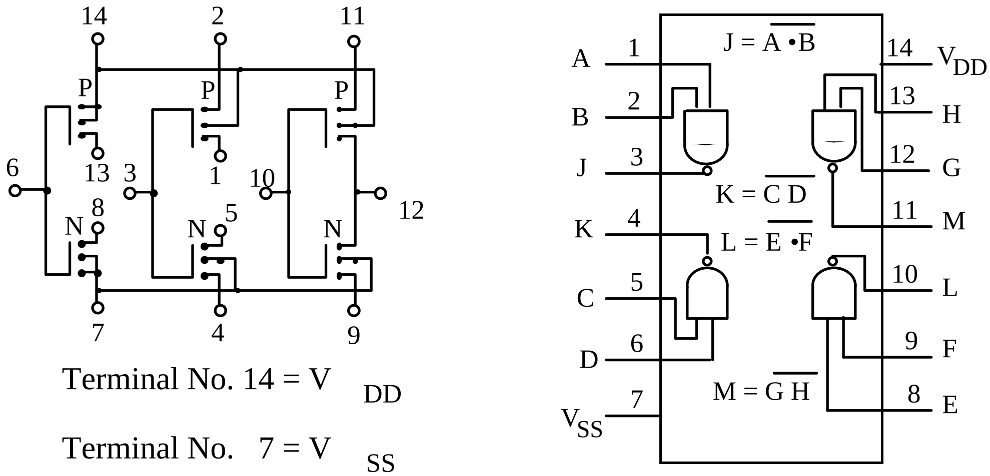
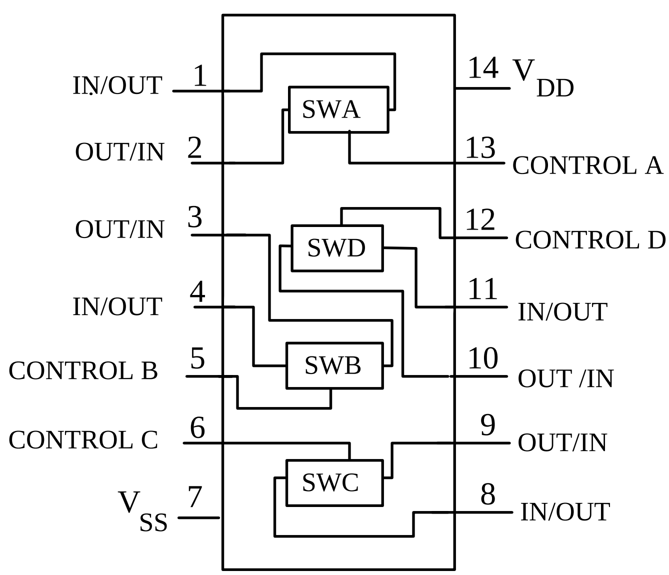


CD 4007 CD 4011A

(a) (b)

Figure 1a & 1b. Pin-out information for the CMOS CD 4007 and CD 4011A IC's.

(c)



CD 4016B

Fig. 1c. Pin-out information for the CMOS CD 4016B/CD 4066 Analog Switch IC.

3. <u>Exercises with CMOS Integrated Circuits:</u>

<u>Part A</u>: a.) Measure the voltage transfer characteristics, V_0 versus V_I associated with a CMOS CD 4011A NAND gate for V_{DD} = 3, 5, 10 and 15 volts. Plot out your V_0 versus V_I measurements on a graph in your lab book, similar to those shown below in Figure 2 (Note that graph paper is available in one of the filing cabinets in the Physics 405 lab and also online, on the Physics 405 web page).
b) What are the “0” and “1” logic levels for each of the four values of V_{DD}?

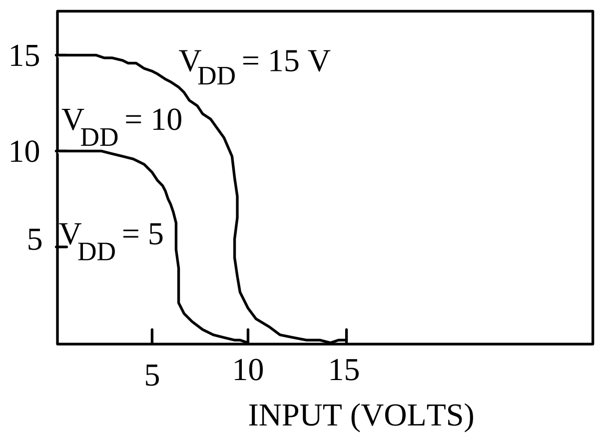


Figure 2: Voltage Transfer Characteristics, V_0 versus V_I of a CMOS CD 4011A NAND gate for V_{DD} = 5, 10 and 15 volts.

<u>Part B</u>: a.) Measure the switching speed of a CMOS CD 4011A NAND gate for V_{DD} = 5 volts. Apply a square wave to one input and observe the output signals if the gates are connected in series. How does the capacitance of your scope probe affect your measurement of the rise and fall times?*
b.) Connect five CMOS inverters (CD4069) in a loop like in the previous lab and measure the frequency of oscillation as a function of V_{DD}.

<u>Part C</u>: **<u>Interfaces Between TTL and CMOS Gates:</u>** (Note: V_{DD} = +5 volts)

a.) Are the TTL logic levels and/or currents adequate to drive a CMOS gate?
b.) Are the CMOS logic levels and/or currents adequate to drive a TTL gate?
c.) What kind of interface circuit(s) between TTL ⇔ CMOS logic are required in order for them to communicate properly with each other?

* Did you use a *<u>compensated</u>* 10X scope probe? Explain.

4. CMOS Three Digit Counter and Display:

CMOS circuits are particularly desirable for use in large-scale systems. The Motorola MC 14553B and MC 14543B are examples of several logic functions integrated into a single IC. The MC 14553B is a three-digit BCD (Binary Coded Decimal) counter with overflow (for cascading purposes). Refer to the MC14553B data sheet for details of the following: Three separate counters (with 4-bit BCD output data) are driven by a common clock input. Three individual 4-bit latches store BCD information associated with each counter. The content of each of the three 4-bit latches is multiplexed and output serially, digit-by-digit. Three output lines (DS1, DS2 and DS3) indicate which digit (1'^{s}, 10'^{s} or 100'^{s}) the BCD data (Q0, Q1, Q2 and Q3) is being displayed at the output. An internal oscillator can be used to determine the 3-digit multiplexing frequency, using C1A & C1B lines. The BCD data output from the MC 14553B IC can then be subsequently decoded by a BCD-to-seven–segment latch/decoder/display driver IC, the MC 14543B (n.b. the CD4056B is equivalent to the Motorola MC 14543B).

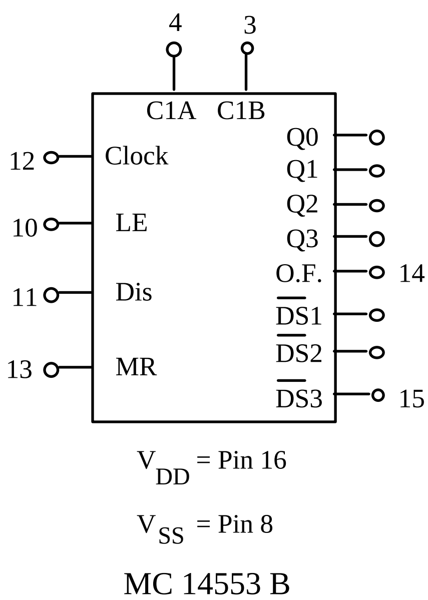


Figure 3. The MC 14553B 3-Digit BCD Counter IC.

Details of the MC14553B 3-Digit BCD Counter IC:

$\overline{DS1}$, $\overline{DS2}$, $\overline{DS3}$ – (outputs) indicate which digit (1’^{s}, 10’^{s} or 100’^{s}) is associated with the BCD data (Q0, Q1, Q2 and Q3). Level is low for the digit being displayed.

Q0, Q1, Q2, Q3 – (outputs) BCD data associated with the particular digit (1’^{s}, 10’^{s} or 100’^{s}) being displayed.

LE – (input) Latches BCD data from the counter into the output(s). Raising this line will latch the current count into the output display register(s). This is function is analogous to the elapsed time on a stop watch. The displayed count at the instant the LE line was initially raised (thus latching the count data) will remain at this count while the counter is still counting. To update the displayed number, simply momentarily drop the LE line low. If the LE line is continuously held low, the displayed number will always equal the current count.

MR – (input) {Master} Reset of the counter. Raising this line resets the counter to 0. To start counting again, drop this line low.

DIS – (input) Disables counting. When this line is high the counter stops counting. When the line is again dropped low, the counter begins counting again, continuing on from its previous count value.

OF – (output) Overflow. This line goes high when the (0:999) counter overflows, i.e. when the count =1000 (and higher).

CIA, CIB – These lines control the 3-digit MUX display rate – i.e. the rate at which the BCD data (outputs Q0, Q1, Q2 and Q3) changes between the three digits (1’^{s}, 10’^{s} or 100’^{s}). The 3-digit MUX display rate can be directly controlled by supplying a clock pulse-train to pin 4, or by placing a capacitor (e.g. 0.001 μF) between C1A & C1B (pins 3 and 4) to cycle through the digits.

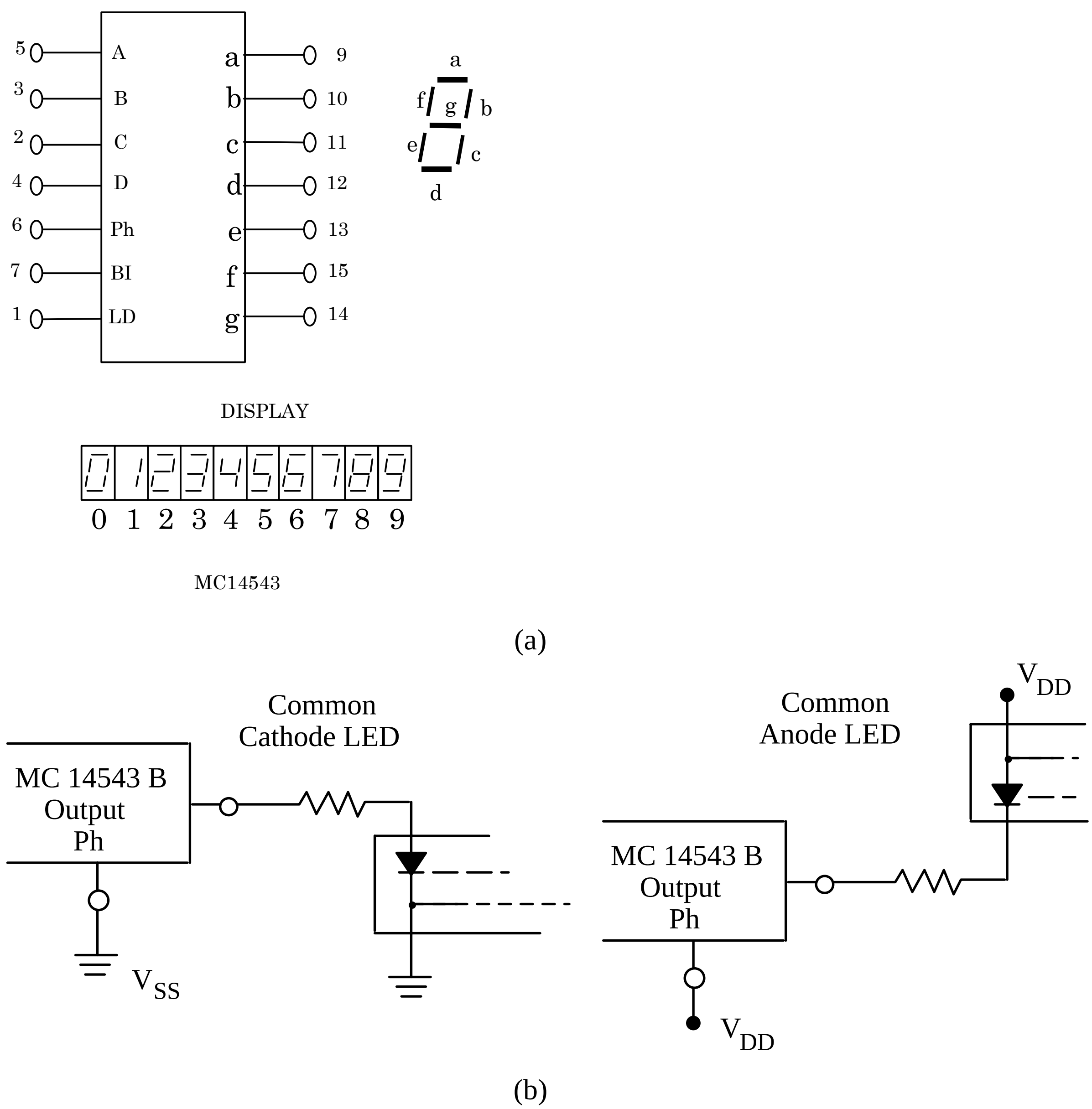


Fig. 4. (a) MC14543 BCD-to-Seven Segment Latch/Decoder/Driver IC and LED readout. Note that for MC14543, V_{DD} is Pin 16 and V_{SS} is Pin 8.

(b) LED connection with MC 14543. [Bipolar transistors may be added for gain (for $V_{DD} \leq 10$ V or $I_{out} \geq 10$ mA)]

Details of the MC14543B BCD-to-Seven Segment Latch/Decoder/Driver IC:

For a given digit (1's, 10's or 100's), the MC14543 IC takes the 4-bit BCD code and outputs data for which of the 7 segments of the LED display are to be on, for that particular number. The MC14543 IC is capable of driving either 7-segment common anode or common cathode displays. For common anode (common cathode) mode, the segments that are to be on will have a low (high) level, respectively.

LD – (input) Latch Disable. Set high (low) to enable (disable) the display numbers, respectively.

A,B,C,D – (input) 4-bit BCD number.

a,b,c,d,e,f,g – outputs to drive the seven-segment display.

Ph – (input) Internally configures the MC14543B for driving common anode or common cathode displays. Set Ph=0 (=1) for use with common cathode (common anode) 7-segment LED displays, respectively.

BI – (input) Setting this line high (low) blanks (enables) the display, respectively.

Multiplexed 7-Segment LED Displays:

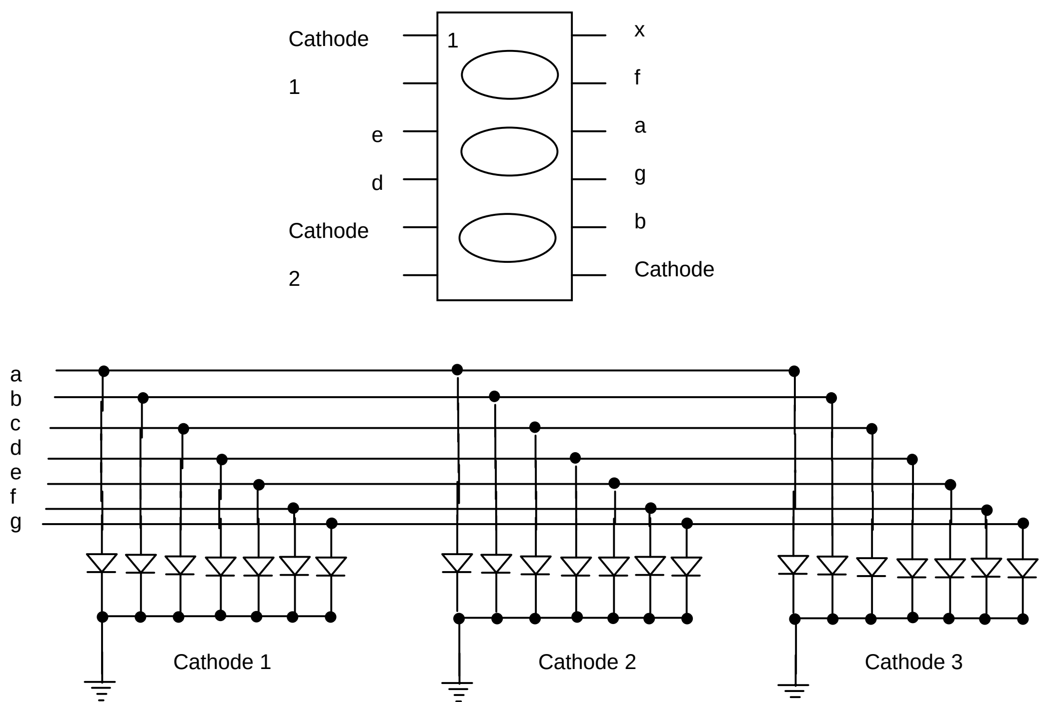


Figure 5. HP 5082-7433 schematic and connections.

Two different types of multiplexed 7-segment LED displays are available in the lab: the HP5082-7433 3-digit bubble displays and the Lumex 4-digit displays [LDQ-N516RI (common cathode) and LDQ-M516RI (common anode)]. The HP5082-7433 is a common cathode 7-segment LED display and its use is shown as an example in our circuit. Note that the line for each segment of HP 5082-7433 is the same for each digit. Therefore applying a voltage to a pin will light the segment on each digit whose cathode is connected to ground. See Figure 5.

During the construction of the 3-digit counter & diplay circuit (using e.g. the common-cathode 7-segment LED display), it is important to understand the details of how the MC14453 3-digit BCD counter acutally outputs the data used for displaying numbers on the 3-digit LED display. MC14453 outputs 7-segment data associated with a number for a given digit (1's, 10's or 100's) one number at a time, and which digit's data that is being output at that time is indicated by a low level on one of the three DS# pins. The MC14453 3digit BCD counter IC begins by outputting the 7-segment data for the 1's digit, with DS1 going low. Then it outputs the 7-segment data for the 10's digit with DS2 going low. Then it outputs the 7-segment data for the 100's digit with DS3 going low. Then it goes back to outputting the 7-segment data for the 1's digit and so on. Thus, if all three of your LED display's common cathodes of are hooked **directly** to ground, then the same number will be simultaneously displayed on all three digits – which is not what we want! In order to properly (i.e. separately, sequentially) display the 7-segment data for the 1's, 10's and 100's digits, the common cathode associated with each LED display digit must be grounded **only** during the time its 7-segment data is supposed to be displayed. A simple way to accomplish this task is to use each of the DS# lines to drive an NPN transistor to control the current flow in the common cathodes associated with each LED display digit.

a.) Design and assemble this circuit on your breadboard using the MC 14553 3-digit BCD counter IC to count pulses and check out its operation at low frequencies using e.g. a 3-digit, 7-segment common cathode LED display.

b.) Investigate (i.e. determine) the maximum frequency of operation of your 3-digit counter and display circuit. Using 50 Ohm impedance RG-58/RG-174 coax cables and BNC Tees, "breeze-by" the output of your function generator (50 Ohm output impedance) first to the channel 1 input of your oscilloscope input (1 Meg-Ohm input impedance), then to the input of your HP 34401 DMM (which also has a 1 Meg-Ohm input impedance) and finally to the input of your circuit. Use a 51 Ohm resistor at the input of your circuit to properly impedance-match the input impedance of your circuit to the 50 Ohm transmission-line/coax cable. Note also that you will need to re-adjust the output level of the function generator with the 51 Ohm coax cable termination resistor installed on the input of your circuit.

Run the frequency of your function generator up from low frequencies continuously through the KHz, 10's of KHz, 100's of KHz bands, simultaneously observing the behavior of your circuit, the function generator signal on the scope and measuring the frequency on the HP 34401 DMM. Verify that the function generator frequency agrees with that measured by the HP34401 DMM and with the frequency as measured from waveform observed on your oscilloscope. Then slowly raise the frequency of your function generator up into the MHz region. Is your HP 34401 DMM capable of measuring frequencies above 1 MHz? Refer to the HP 34401 DMM User Manual for specifications on this device. Raise the frequency of your function generator past 2 MHz, simultaneously monitoring the signal on your scope and your circuit. What happens? From the waveform displayed on your oscilloscope, determine the maximum frequency of operation of your 3-digit counter and display circuit. Explain in your lab report why impedance matching from the output of the function generator to the input of your circuit is important. Is impedance matching important/necessary at **all** frequencies – low and high? If not, what are the criteria for which impedance-matching between function generator output and circuit input becomes important?

c.) What additional components would be necessary for your 3-digit counter and display circuit in order to build a frequency meter? (see e.g. *Horowitz and Hill* 2nd ed., section 15.10)

d.) What additional components would be necessary for your 3-digit counter and display circuit in order to enable it to measure higher frequencies?