Lab 5: FET circuits

Reading:
"The Art of Electronics (TAOE)"
Section 3.01 –3.10, FET's, followers, and current sources. Specifically look at information relevant to today's lab: follower, current source, and variable resistor

5.1 FET Characteristics

a) Pinch off voltage V_p (called V_T for a JFET) and I_{DSS}

Recall that there are two types of FET- a normally on (Depletion Mode) and normally off (Enhancement Mode). The JFET is a normally on device, which means that it can be turned off with an applied voltage. The voltage that turns it completely off is called the "pinch off voltage". The aim of this section is to verify the "transfer characteristics" presented on the data sheet by measuring I_{DSS} (the current flowing when $V_{GS} = 0$) and V_T (the voltage for which I_D is reduced to zero). Plot a graph to verify the relation between I_D and V_{GS} shown in the data sheet.

Once you have obtained these values, look at some results from other groups and note the spread in values across a single batch. Check that your values fall within the manufacturers maximum range.

$$8.0 \text{ mA} < I_{DSS} < 20 \text{ mA}$$
$$-6 \text{ V} < V_T < -2 \text{ V}$$

Your specific value of V_T will be useful to know for some of the following circuits. What role does the 0.01uF capacitor play?

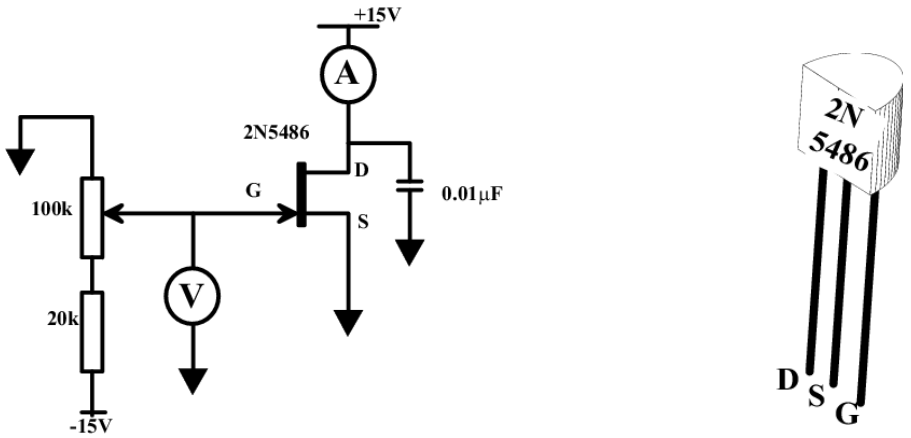

Figure 5.1: FET test circuit. Plot I_D vs V_{GS}.

5.2 Common Drain Source Characteristics (I_D vs V_{DS})

Construct the following circuit. This will allow you to examine the "common drain source characteristics" of a JFET. A sample plot is shown on the transistor data sheet in which the operation of the transistor is presented as a series of lines for constant V_{GS}. In the following you will attempt to reproduce these graphs.

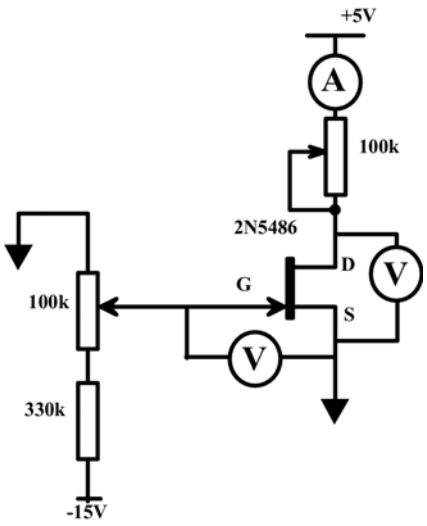

Figure 5.2: Circuit to measure V_{DS} vs I_D

We want to trace out a line of constant V_{GS}, so the first step is to set V_{GS} to a test value. Then measure I_D for a wide range of voltages V_{DS}. Then try a new value of V_{GS} (use a total of four values of constant V_{GS} = -3, -2, -1, 0V). Plot these on a graph and compare them to the figure in the data sheet. How well do they compare?

5.3 Transconductance and the "Load Line" (Optional)

Transconductance, g, of a FET is the equivalent parameter to h_{FE} for a BJT. It is given by the ratio $I_D/(V_{GS}-V_T)$ that has units of "Mhos" or "Seimens" (S). Why is this parameter important rather than the equivalent construction (I_D/I_G) that we used for the BJT? Construct the following circuit and determine the value of the transconductance of the 2N5486 for a wide range of values of the drain current I_D.

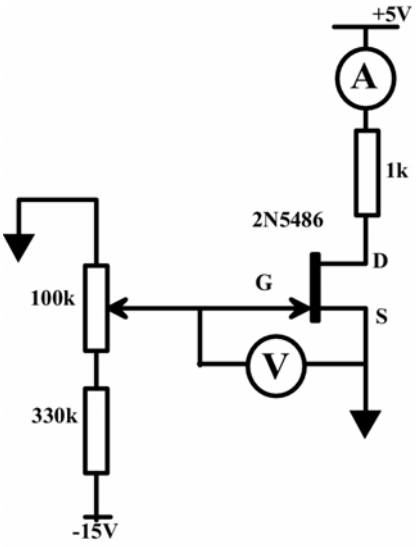

Figure 5.3. Circuit to measure transconductance.

Try to explain the results that you get from this circuit using the results of section 5.2.

5.4 FET Current Sources (Optional)

a) Discreet Transistor Current Source

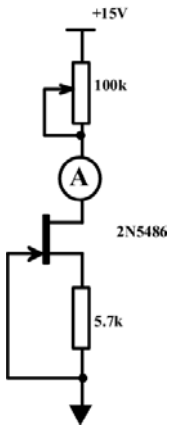

Figure 5.3: FET current source

Wire up the circuit above. How good a current source is this? Vary the load and watch V_{DS} with your digital voltmeter as you monitor the current I_{OUT} with the ammeter.

What is V_{DS} when the constant current behaviour starts to breakdown? This V_{DS} value marks the boundary of the linear region and should occur when V_{DS} is near V_{GS}-V_T. Does your FET's linear region begin around this value of V_{DS}?

What you have just constructed is a *two terminal* current source (a current source that requires no external bias)! This device is almost as easy to use as a resistor as it can be simply slotted into a circuit to provide constant current. Why is it only *almost* as versatile as a resistor? FET manufacturers have constructed exactly this type of device that is now sold as a current source.

b) Integrated Two Terminal Current Source

The J510 is a JFET with the source shorted to the gate, but available in a two terminal package (sometimes this package looks just like a diode and is called a current regulator diode). The current sources are sorted by I_{DSS}; the J510 passes 3.6mA.

First try the FET in the test circuit above (replacing the 2N5486 and 5.6k resistor with the J510). Does the current source perform as well as the circuit you built with the '5486? Would you expect it to?

Now to get a feel for how easy it is to design a circuit with this device, try the circuit below – which at a glance will look slightly foolish.

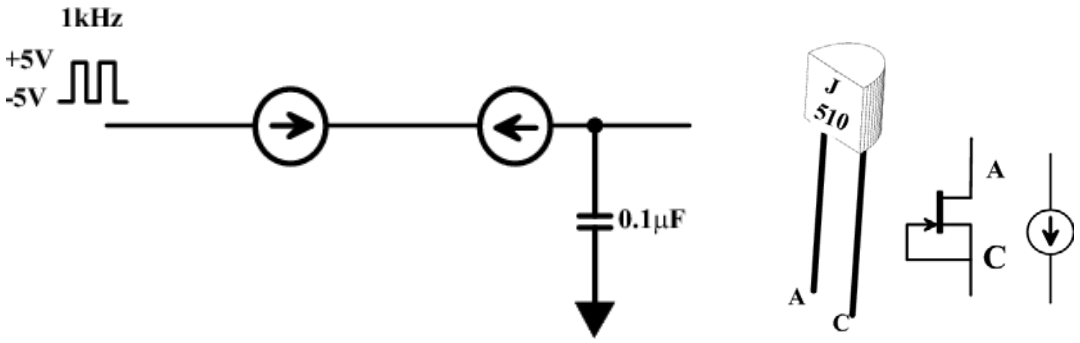

Figure 5.3: Application for a two terminal current source: square wave to (?) circuit.

What output waveform do you expect? In this circuit a JFET's gate *conducts* if it is forward biased with respect to either the source or the drain, that is why this circuit will operate.

Drive the circuit with a 1kHz square wave of about 5 volts' amplitude. Centre the input waveform on zero volts and note whether the output is centred. If it is not, why is it not?

Now gradually lower the input amplitude until you notice distortion in the output (some curvature near the points). Why does this occur? (*Hint:* At the point where you notice curvature beginning, note the voltage across the FET: V_{DS}).

5.5 FET as a Variable Resistor

When you tested the FET as a *current source*, you found that the circuit failed when V_{DS} shrank so far that the device fell into its linear region. Here you will build a circuit intended to operate always within that region: it will fail if V_{DS} gets large enough to carry the FET into the current source region.

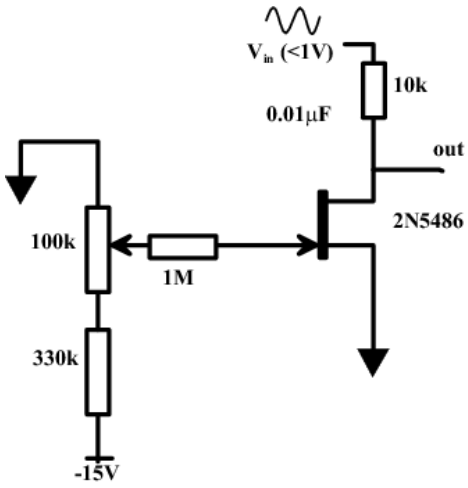

Figure 5.7: FET as a voltage controlled resistor/attenuator circuit

a) Uncompensated Attenuator

Drive the circuit above with a small sine wave **(around 0.2V)** at around **1kHz**. Adjust the potentiometer and note the results, not only in variable attenuation but also in varying the amounts of distortion. (To see the distortion clearly, drive the circuit with a *triangle* waveform.) Would you predict such a distortion from what you have seen so far? How does the circuit treat a larger input waveform?

b) Compensated attenuator

Adding ½ V_{DS} to the gate signal straightens the curves of figure 3.30 considerably. The above amendment to the circuit performs this addition. Take a look at its effect in the shape of V_{out} as you drive the circuit with a triangle waveform of about 0.2V amplitude.

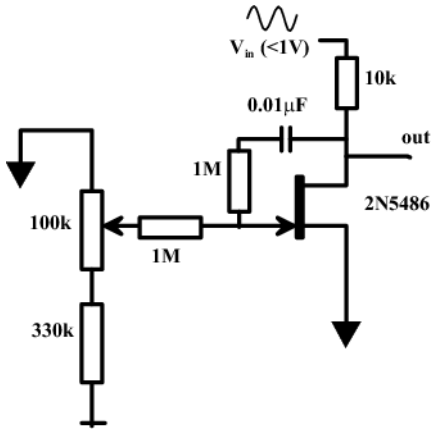

Figure 5.7: FET as a voltage controlled resistor/attenuator circuit

c) Amplitude modulation

The circuits above are not very impressive, because it is just as easy to vary the amplitude of the signal using a variable resistor that you turn by hand as it is to use the FET. However with the FET, a *voltage* controls the amount of attenuation this circuit, thus it is

much more flexible (not to mention faster) than a simple hand turned pot. Using this circuit we can control the size of a signal using a second signal as a control.

To put this ability of the FET to work, we shall use a second function generator to drive the gate voltage, so that this second signal replaces the potentiometer and modulates the amplitude of the input signal. Let the frequency of modulation be small, try $f_{modulation}$ of around 50Hz and keep the modulation amplitude small (**around 0.2 V**). For a stable display of the output waveform trigger the scope on the modulation signal not on the modulated output.

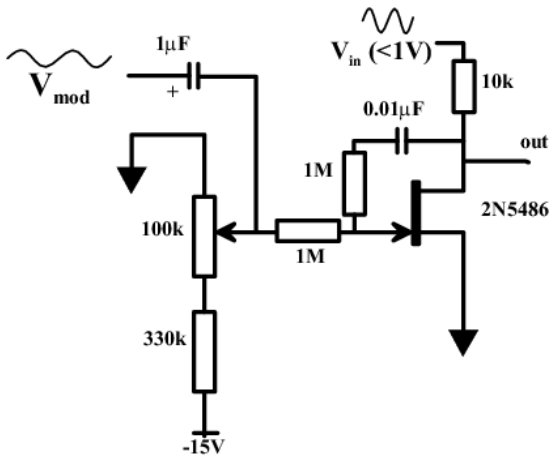

Figure 5.8: Amplitude modulation, or multiplication of one signal by another

d) AM Radio (optional)

This circuit can be easily turned into an AM Radio transmitter. Drive the point called V_{in} with a sine wave of about **1MHz** (this is the carrier frequency, $f_{carrier}$). Attach a few cms of wire to the output point to act as an aerial then tune an AM radio located nearby to a quite place on the dial and adjust $f_{carrier}$ until you can hear the modulating signal (a single tone). (To make it easier you might want to use the sweep function of the function generator).