MC14046B

PhaseLockedLoop

The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC_{1, out}, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, PC_{2, out} and LD, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins C1_{A}, C1_{B}, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

Features
- Buffered Outputs Compatible with Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin–for–Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive OR Gate and is Duty Cycle Limited
- Phase Comparator 2 Switches on Rising Edges and is not Duty Cycle Limited
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD}</td>
<td>DC Supply Voltage Range</td>
<td>–0.5 to +18.0</td>
<td>V</td>
</tr>
<tr>
<td>V_{in}</td>
<td>Input Voltage Range (All Inputs)</td>
<td>–0.5 to V_{DD} + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>I_{in}</td>
<td>DC Input Current, per Pin</td>
<td>± 10</td>
<td>mA</td>
</tr>
<tr>
<td>P_{D}</td>
<td>Power Dissipation, per Package (Note 1)</td>
<td>500</td>
<td>mW</td>
</tr>
<tr>
<td>T_{A}</td>
<td>Operating Temperature Range</td>
<td>–55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>Storage Temperature Range</td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
- Plastic “P” and D/DW Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
### ELECTRICAL CHARACTERISTICS (Voltages Referenced to \( V_{SS} \))

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>( V_{DD} )</th>
<th>(-55^\circ C)</th>
<th>( 25^\circ C)</th>
<th>( 125^\circ C)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage 0 Level</td>
<td>( V_{OL} )</td>
<td>5.0</td>
<td>–</td>
<td>–</td>
<td>0</td>
<td>0.05</td>
</tr>
<tr>
<td>( V_{in} = V_{DD} ) or 0</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>0</td>
<td>0.05</td>
<td>–</td>
</tr>
<tr>
<td>( V_{in} = 0 ) or ( V_{DD} )</td>
<td>15</td>
<td>–</td>
<td>–</td>
<td>0</td>
<td>0.05</td>
<td>–</td>
</tr>
<tr>
<td>Input Voltage (Note 2) 0 Level</td>
<td>( V_{IL} )</td>
<td>5.0</td>
<td>–</td>
<td>1.5</td>
<td>2.25</td>
<td>1.5</td>
</tr>
<tr>
<td>(( V_{O} = 4.5 ) or 0.5 Vdc)</td>
<td>10</td>
<td>–</td>
<td>3.0</td>
<td>4.50</td>
<td>3.0</td>
<td>–</td>
</tr>
<tr>
<td>(( V_{O} = 9.0 ) or 1.0 Vdc)</td>
<td>15</td>
<td>–</td>
<td>4.0</td>
<td>6.75</td>
<td>4.0</td>
<td>–</td>
</tr>
<tr>
<td>1 Level</td>
<td>( V_{IH} )</td>
<td>5.0</td>
<td>3.5</td>
<td>–</td>
<td>3.5</td>
<td>2.75</td>
</tr>
<tr>
<td>(( V_{O} = 0.5 ) or 4.5 Vdc)</td>
<td>10</td>
<td>7.0</td>
<td>–</td>
<td>7.0</td>
<td>5.50</td>
<td>–</td>
</tr>
<tr>
<td>(( V_{O} = 1.0 ) or 9.0 Vdc)</td>
<td>15</td>
<td>11</td>
<td>–</td>
<td>11</td>
<td>8.25</td>
<td>–</td>
</tr>
<tr>
<td>Output Drive Current Source</td>
<td>( I_{OH} )</td>
<td>5.0</td>
<td>–</td>
<td>1.2</td>
<td>–</td>
<td>1.0</td>
</tr>
<tr>
<td>(( V_{OH} = 2.5 ) Vdc)</td>
<td>5.0</td>
<td>–</td>
<td>0.25</td>
<td>–</td>
<td>0.2</td>
<td>–</td>
</tr>
<tr>
<td>(( V_{OH} = 9.5 ) Vdc)</td>
<td>10</td>
<td>–</td>
<td>0.62</td>
<td>–</td>
<td>0.5</td>
<td>–</td>
</tr>
<tr>
<td>(( V_{OH} = 13.5 ) Vdc)</td>
<td>15</td>
<td>–</td>
<td>1.8</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
</tr>
<tr>
<td>(( V_{OL} = 0.4 ) Vdc)</td>
<td>( I_{OL} )</td>
<td>5.0</td>
<td>0.64</td>
<td>–</td>
<td>0.51</td>
<td>0.88</td>
</tr>
<tr>
<td>(( V_{OL} = 0.5 ) Vdc)</td>
<td>10</td>
<td>1.6</td>
<td>–</td>
<td>1.3</td>
<td>2.25</td>
<td>–</td>
</tr>
<tr>
<td>(( V_{OL} = 1.5 ) Vdc)</td>
<td>15</td>
<td>4.2</td>
<td>–</td>
<td>3.4</td>
<td>8.8</td>
<td>–</td>
</tr>
<tr>
<td>Input Current</td>
<td>( I_{in} )</td>
<td>15</td>
<td>–</td>
<td>± 0.1</td>
<td>–</td>
<td>±0.00001</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{in} )</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>5.0</td>
<td>7.5</td>
</tr>
<tr>
<td>Quiescent Current (Per Package)</td>
<td>( I_{DD} )</td>
<td>5.0</td>
<td>–</td>
<td>5.0</td>
<td>–</td>
<td>0.005</td>
</tr>
<tr>
<td>(Inh = “0”, ( f_{in} = 10 ) kHz, ( C_{in} = 50 ) pF, ( R_{in} = 1.0 ) M( \Omega ), ( R_{out} = \infty ), and 50% Duty Cycle)</td>
<td>10</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>0.010</td>
<td>10</td>
</tr>
<tr>
<td>15</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>0.015</td>
<td>20</td>
<td>–</td>
</tr>
<tr>
<td>Total Supply Current (Note 3)</td>
<td>( I_{T} )</td>
<td>5.0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>(Inh = “0”, ( f_{in} = 10 ) kHz, ( C_{in} = 50 ) pF, ( R_{in} = 1.0 ) M( \Omega ), ( R_{out} = \infty ), and 50% Duty Cycle)</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>15</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>


Noise Margin for both “1” and “0” level =

\[
1.0 \text{ Vdc min } @ V_{DD} = 5.0 \text{ Vdc} \\
2.0 \text{ Vdc min } @ V_{DD} = 10 \text{ Vdc} \\
2.5 \text{ Vdc min } @ V_{DD} = 15 \text{ Vdc}
\]

3. To Calculate Total Current in General:

\[
I_{T} = 2.2 \times V_{DD} \left( V_{CO_{in}} - 1.65 \right) + V_{DD} - 1.35 \left\{ R_{1} \right\}^{3/4} + 1.6 \times V_{CO_{in}} - 1.65 \left\{ R_{SF} \right\}^{3/4} + 1 \times 10^{-3} \left( C_{L} + 9 \right) V_{DD} f + 1 \times 10^{-3} V_{DD}^{2} \left( \frac{100 \text{ Duty Cycle of } PCA_{in}}{100} \right) + I_{0}
\]

where: \( I_{T} \) in \( mA \), \( C_{L} \) in pF, VCOin, VDD in Vdc, f in kHz, and R1, R2, R_{SF} in M\( \Omega \), C_{L} on VCO_{out}.

http://onsemi.com
**ELECTRICAL CHARACTERISTICS** (Note 4) (CL = 50 pF, TA = 25°C)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>VDD Vdc</th>
<th>Minimum Device</th>
<th>Typical</th>
<th>Maximum Device</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Rise Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tTLH = (3.0 ns/pF) CL + 30 ns</td>
<td>tTLH</td>
<td>5.0</td>
<td>–</td>
<td>180</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>tTLH = (1.5 ns/pF) CL + 15 ns</td>
<td></td>
<td>10</td>
<td>–</td>
<td>90</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>tTLH = (1.1 ns/pF) CL + 10 ns</td>
<td></td>
<td>15</td>
<td>–</td>
<td>65</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>Output Fall Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tTHL = (1.5 ns/pF) CL + 25 ns</td>
<td>tTHL</td>
<td>5.0</td>
<td>–</td>
<td>100</td>
<td>175</td>
<td></td>
</tr>
<tr>
<td>tTHL = (0.75 ns/pF) CL + 12.5 ns</td>
<td></td>
<td>10</td>
<td>–</td>
<td>50</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td>tTHL = (0.55 ns/pF) CL + 9.5 ns</td>
<td></td>
<td>15</td>
<td>–</td>
<td>37</td>
<td>55</td>
<td></td>
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</tbody>
</table>

**PHASE COMPARATORS 1 and 2**

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Resistance – PCAin</td>
<td>Rin</td>
<td>5.0</td>
<td>1.0</td>
<td>2.0</td>
<td>–</td>
<td>MΩ</td>
</tr>
<tr>
<td>– PCBin</td>
<td>Rin</td>
<td>15</td>
<td>150</td>
<td>1500</td>
<td>–</td>
<td>MΩ</td>
</tr>
<tr>
<td>Minimum Input Sensitivity</td>
<td>VIn</td>
<td>5.0</td>
<td>–</td>
<td>200</td>
<td>300</td>
<td>mV p–p</td>
</tr>
<tr>
<td>AC Coupled — PCAin</td>
<td>R1</td>
<td>10</td>
<td>–</td>
<td>400</td>
<td>600</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>1500</td>
<td>–</td>
<td>1050</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>DC Coupled – PCAin, PCBin</td>
<td>–</td>
<td>5 to 15</td>
<td>–</td>
<td>See Noise Immunity</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VOLTAGE CONTROLLED OSCILLATOR (VCO)**

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Frequency</td>
<td>fmax</td>
<td>5.0</td>
<td>0.5</td>
<td>0.7</td>
<td>–</td>
<td>MHz</td>
</tr>
<tr>
<td>(VCOin = VDD, C1 = 50 pF)</td>
<td></td>
<td>10</td>
<td>1.0</td>
<td>1.4</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>1.4</td>
<td>1.9</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Temperature – Frequency Stability (R2 = ∞)</td>
<td>–</td>
<td>5.0</td>
<td>–</td>
<td>0.12</td>
<td>–</td>
<td>%/°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>–</td>
<td>0.04</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>–</td>
<td>0.015</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Linearity (R2 = ∞)</td>
<td>–</td>
<td>5.0</td>
<td>–</td>
<td>1.0</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>(VCOin = 2.5 V ± 0.3 V, R1 &gt; 10 kΩ)</td>
<td></td>
<td>10</td>
<td>–</td>
<td>1.0</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>(VCOin = 5.0 V ± 2.5 V, R1 &gt; 400 kΩ)</td>
<td></td>
<td>15</td>
<td>–</td>
<td>1.0</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>(VCOin = 7.5 V ± 5.0 V, R1 ≥ 1000 kΩ)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Duty Cycle</td>
<td>–</td>
<td>5 to 15</td>
<td>–</td>
<td>50</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Input Resistance – VCOin</td>
<td>Rin</td>
<td>15</td>
<td>150</td>
<td>1500</td>
<td>–</td>
<td>MΩ</td>
</tr>
</tbody>
</table>

**SOURCE–FOLLOWER**

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Voltage</td>
<td>–</td>
<td>5.0</td>
<td>–</td>
<td>1.65</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>(VCOin minus SFout, RSF &gt; 500 kΩ)</td>
<td></td>
<td>10</td>
<td>–</td>
<td>1.65</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>–</td>
<td>1.65</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td>Linearity</td>
<td>–</td>
<td>5.0</td>
<td>–</td>
<td>0.1</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>(VCOin = 2.5 V ± 0.3 V, RSF &gt; 50 kΩ)</td>
<td></td>
<td>10</td>
<td>–</td>
<td>0.6</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>(VCOin = 5.0 V ± 2.5 V, RSF &gt; 50 kΩ)</td>
<td></td>
<td>15</td>
<td>–</td>
<td>0.8</td>
<td>–</td>
<td></td>
</tr>
</tbody>
</table>

**ZENER DIODE**

|                     |        |         |                |         |                |       |
| Zener Voltage (Iz = 50 μA) | VZ    | –       | 6.7            | 7.0     | 7.3            | V     |
| Dynamic Resistance (Iz = 1.0 mA) | RZ    | –       | –              | 100     | –              | Ω     |

4. The formula given is for the typical characteristics only.
# ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC14046BCP</td>
<td>PDIP−16</td>
<td>500 Units / Rail</td>
</tr>
<tr>
<td>MC14046BCPG</td>
<td>PDIP−16 (Pb−Free)</td>
<td>500 Units / Rail</td>
</tr>
<tr>
<td>MC14046BDW</td>
<td>SOIC−16 WB</td>
<td>47 Units / Rail</td>
</tr>
<tr>
<td>MC14046BDWG</td>
<td>SOIC−16 WB (Pb−Free)</td>
<td>47 Units / Rail</td>
</tr>
<tr>
<td>MC14046BDWR2</td>
<td>SOIC−16 WB</td>
<td>1000 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC14046BDWR2G</td>
<td>SOIC−16 WB (Pb−Free)</td>
<td>1000 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC14046BF</td>
<td>SOEIAJ−16</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>MC14046BFEL</td>
<td>SOEIAJ−16</td>
<td>2000 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC14046BFELG</td>
<td>SOEIAJ−16 (Pb−Free)</td>
<td>2000 Units / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
Figure 1. Phase Comparators State Diagrams

<table>
<thead>
<tr>
<th>PHASE COMPARATOR 1</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Stage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCAin</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCBin</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC1out</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PHASE COMPARATOR 2</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Stage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCAin</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCBin</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC2out</td>
<td>0</td>
<td>3–State Output Disconnected</td>
</tr>
<tr>
<td>LD (Lock Detect)</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Refer to Waveforms in Figure 3.

### Figure 2. Design Information

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Using Phase Comparator 1</th>
<th>Using Phase Comparator 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>No signal on input PCAin.</td>
<td>VCO in PLL system adjusts to center frequency ( f_0 ).</td>
<td>VCO in PLL system adjusts to minimum frequency ( f_{\text{min}} ).</td>
</tr>
<tr>
<td>Phase angle between PCAin and PCBin.</td>
<td>90° at center frequency ( f_0 ), approaching 0° and 180° at ends of lock range (2( f_L ))</td>
<td>Always 0° in lock (positive rising edges).</td>
</tr>
<tr>
<td>Locks on harmonics of center frequency.</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Signal input noise rejection.</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Lock frequency range (2( f_L )).</td>
<td>The frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2( f_L ) = full VCO frequency range = ( f_{\text{max}} - f_{\text{min}} ).</td>
<td></td>
</tr>
<tr>
<td>Capture frequency range (2( f_C )).</td>
<td>The frequency range of the input signal on which the loop will lock if it was initially out of lock.</td>
<td>Depends on low-pass filter characteristics (see Figure 3). ( f_C \leq f_L )</td>
</tr>
<tr>
<td>Center frequency ( f_0 ).</td>
<td>The frequency of VCOout, when VCOin = 1/2 ( V_{DD} )</td>
<td>( f_C = f_L )</td>
</tr>
<tr>
<td>VCO output frequency ( f ).</td>
<td>( f_{\text{min}} = \frac{1}{R_2(C_1 + 32 \text{ pF})} ) ( (V_{CO \text{ input}} = V_{SS}) )</td>
<td>( f_{\text{max}} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{\text{min}} ) ( (V_{CO \text{ input}} = V_{DD}) )</td>
</tr>
</tbody>
</table>

Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ±20%.

\( f_{\text{min}} \) = minimum VCO frequency

\( f_{\text{max}} \) = maximum VCO frequency

\( f_C \) = capture frequency

\( f_L \) = lock frequency

\( f_0 \) = center frequency

\( R_1 \) and \( R_2 \) = resistors

\( C_1 \) = capacitor

\( V_{DD} \) = supply voltage

\( V_{SS} \) = ground

\( f_{\text{min}} \) = 1/2 \( V_{DD} \)

\( f_{\text{max}} \) = 1/2 \( V_{DD} \)
Typical Low-Pass Filters

![Typical Low-Pass Filters Diagram]

NOTE: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor Cc is then placed from the midpoint to ground. The value for Cc should be such that the corner frequency of this network does not significantly affect \( \omega_n \). In Figure B, the ratio of R3 to R4 sets the damping, \( R4 \cdot C2 = \frac{6N}{f_{max}^2} - \frac{N}{2\pi \Delta f} \) for optimum results.

Definitions:

\[ N = \text{Total division ratio in feedback loop} \]
\[ K_\phi = \frac{V_{DD}}{\pi} \text{ for Phase Comparator 1} \]
\[ K_\phi = \frac{V_{DD}}{4\pi} \text{ for Phase Comparator 2} \]
\[ K_{VCO} = \frac{V_{DD} - 2V}{V_{DD}} \]
for a typical design \( \Omega_n = \frac{2\pi f_r}{10} \) (at phase detector input)
\[ \zeta = 0.707 \]

LOW-PASS FILTER

<table>
<thead>
<tr>
<th>Filter A</th>
<th>Filter B</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ \omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_3 C_2}} ]</td>
<td>[ \omega_n = \sqrt{\frac{K_\phi K_{VCO}}{R_2 (R_3 + R_4)}} ]</td>
</tr>
<tr>
<td>[ \zeta = \frac{N \omega_n}{2K_\phi K_{VCO}} ]</td>
<td>[ \zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K_\phi K_{VCO}}) ]</td>
</tr>
<tr>
<td>[ F(s) = \frac{1}{R_3 C_2 S + 1} ]</td>
<td>[ F(s) = \frac{R_3 C_2 S + 1}{S (R_3 C_2 + R_4 C_2) + 1} ]</td>
</tr>
</tbody>
</table>

Waveforms

**Phase Comparator 1**

- \( \text{PCA}_\text{in} \)
- \( \text{PCB}_\text{in} \)
- \( \text{PC1}_\text{out} \)
- \( \text{VCO}_\text{in} \)

**Phase Comparator 2**

- \( \text{PCA}_\text{in} \)
- \( \text{PCB}_\text{in} \)
- \( \text{PC2}_\text{out} \)
- \( \text{VCO}_\text{in} \)

Note: for further information, see:


Figure 3. General Phase–Locked Loop Connections and Waveforms
NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MILLIMETERS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>7.40, 7.70</td>
<td>0.29, 0.30</td>
</tr>
<tr>
<td>B</td>
<td>2.50, 2.70</td>
<td>0.09, 0.10</td>
</tr>
<tr>
<td>C</td>
<td>0.145, 0.175</td>
<td>0.06, 0.07</td>
</tr>
<tr>
<td>D</td>
<td>0.015, 0.021</td>
<td>0.0006, 0.0008</td>
</tr>
<tr>
<td>F</td>
<td>0.040, 0.070</td>
<td>0.0016, 0.0028</td>
</tr>
<tr>
<td>G</td>
<td>0.100 BSC, 2.54 ↑5SC</td>
<td>0.039, 0.10</td>
</tr>
<tr>
<td>H</td>
<td>0.050 BSC, 1.27 BSC</td>
<td>0.020, 0.049</td>
</tr>
<tr>
<td>J</td>
<td>0.008, 0.015</td>
<td>0.0003, 0.0006</td>
</tr>
<tr>
<td>K</td>
<td>0.110, 0.120</td>
<td>0.043, 0.047</td>
</tr>
<tr>
<td>L</td>
<td>0.296, 0.305</td>
<td>0.0116, 0.0120</td>
</tr>
<tr>
<td>M</td>
<td>0°, 0°</td>
<td>0°, 0°</td>
</tr>
<tr>
<td>S</td>
<td>0.020, 0.040</td>
<td>0.0008, 0.0016</td>
</tr>
</tbody>
</table>

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.
MC14046B

PACKAGE DIMENSIONS

SOEIAJ−16
F SUFFIX
CASE 966−01
ISSUE A

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION [b] DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.25</td>
<td>0.26</td>
<td>0.002</td>
<td>0.008</td>
</tr>
<tr>
<td>b</td>
<td>0.35</td>
<td>0.50</td>
<td>0.014</td>
<td>0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.10</td>
<td>0.20</td>
<td>0.007</td>
<td>0.011</td>
</tr>
<tr>
<td>D</td>
<td>0.90</td>
<td>10.50</td>
<td>0.390</td>
<td>0.413</td>
</tr>
<tr>
<td>E</td>
<td>4.10</td>
<td>4.50</td>
<td>0.201</td>
<td>0.215</td>
</tr>
<tr>
<td>t</td>
<td>1.27</td>
<td>0.05</td>
<td>0.090</td>
<td>0.050</td>
</tr>
<tr>
<td>M</td>
<td>0.50</td>
<td>0.85</td>
<td>0.020</td>
<td>0.033</td>
</tr>
<tr>
<td>L</td>
<td>1.19</td>
<td>1.50</td>
<td>0.040</td>
<td>0.059</td>
</tr>
<tr>
<td>e</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>d</td>
<td>0.70</td>
<td>0.90</td>
<td>0.028</td>
<td>0.035</td>
</tr>
<tr>
<td>Z</td>
<td>0.76</td>
<td>0.83</td>
<td>0.001</td>
<td>0.001</td>
</tr>
</tbody>
</table>

0.13 (0.005)
0.10 (0.004)

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