Lecture 12

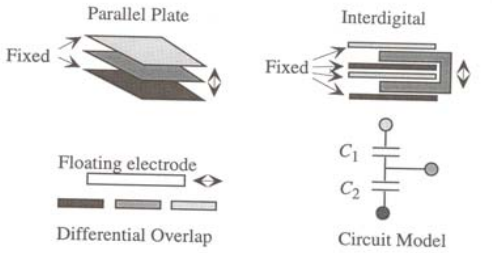
- Agenda:
  - Capacitive Interface Circuits

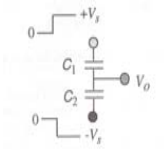
Capacitive Sensing

- Capacitive Sensing

MEMS Capacitive Sensors:
- High impedance
- Small sensing capacitance
- Very small signal
- Parasitic capacitance
- Noise

Capacitive Sensing



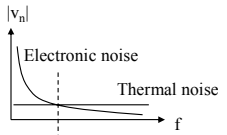


$$V_0 = -V_s + \frac{C_1}{C_1 + C_2}(2V_s) = \frac{C_1 - C_2}{C_1 + C_2}V_s$$

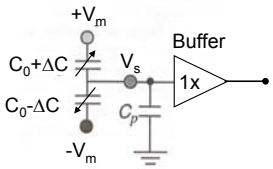
- Differential Capacitive Sensing
  - First order cancellation of many effects
    - Temperature variations
  - Common mode rejection

Capacitive Sensing

- **Challenges**
  - Small sensing capacitance
  - High output impedance
  - Parasitics
  - Noises
    - 1/f noise
  - Offset
  - DC bias



Parasitic Capacitance

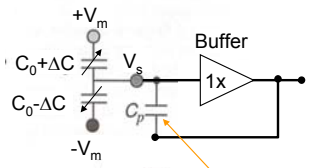


$$V_s = \frac{2\Delta C}{2C_0 + C_P} V_m$$

If C_0=100fF, C_P =200fF,

The signal will be attenuated by half

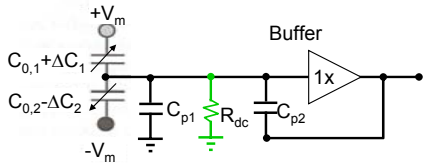
Bootstrapping



Zero voltage across C_p

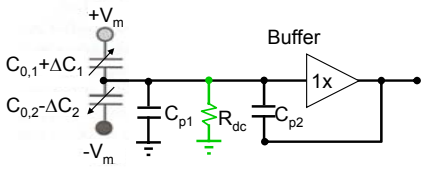
- Increased fabrication complexity
- Difficult to cancel all parasitics

DC Bias at Sensing Node



- Charging on the small sensing capacitors causes drifting, instability and uncertain electrostatic force
- R_{dc} provides DC bias, charging path
- Typical R_{dc} > 1MΩ

DC Bias at Sensing Node



Typical R_{dc} > 1MΩ

- Polysilicon resistor:
  - Large silicon area
  - Large parasitics: capacitance; inductance
- Switched-capacitor circuits
- Diodes
- Sub-threshold transistors
- Long-channel transistors

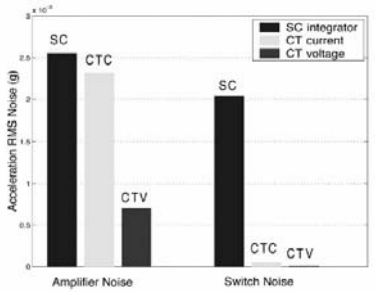
Capacitive Interface Circuits

- ❑ **Noise Analysis**
- ❑ **Input transistor optimization**
- ❑ **Chopper Stabilization (CHS)**
  - ➢ **Continuous-time amplifiers**
- ❑ **Correlated Double Sampling (CDS)**
- ❑ **CHS vs CDS Comparison**
- ❑ **Design Example**

Capacitive Interface Circuits

Continuous-time (CT)
- **CT Voltage Sensing (CTV)**
  - Impedance-conversion buffer
  - Charge integration
- **CT Current Sensing (CTC)**
  - Transimpedance amplifier

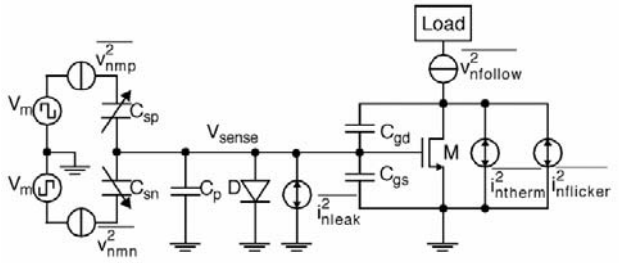
Discrete-time (DT)
- **Switched Capacitor (SC) Sensing: Correlated Double Sampling (CDS)**



- Flicker noise
- Offset
- kT/C noise (CDS)
- Noise folding
- Charge injection
- Quantization noise

J. Wu et al., IEEE J. SSC, 2004

Noise Analysis



$$\frac{\overline{v_n^2}}{\Delta f}(f) = \frac{\overline{v_{ntherm}^2}}{\Delta f}(f) + \frac{\overline{v_{nflicker}^2}}{\Delta f}(f) + \frac{\overline{v_{nleak}^2}}{\Delta f}(f)$$
$$= \frac{K_t T}{W^\beta L^{\beta-1}} + \frac{K_f}{WLf} + \frac{K_s I_{leak}}{(2C_s + C_P + C_{gs} + C_{gd})^2 f^2}$$

J. Wu et al., IEEE J. SSC, 2004

Input Transistor Optimization

But, $$V_{sense} = \frac{2\Delta C}{2C_0 + C_P + C_{gs} + C_{gd}} V_m$$

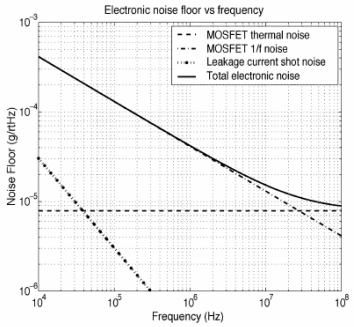
and $$C_{gs} + C_{gd} = (\frac{2}{3}L + 2L_{overlap})W$$

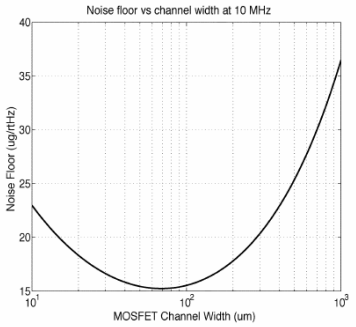
Increase W $\Longrightarrow$ Reduce 1/f noise and thermal noise
But reduce sensitivity.

Maximize SNR given by $\frac{V_{sense}^2}{\overline{v}_n^2}$

$\Longrightarrow$ Optimal input-transistor width

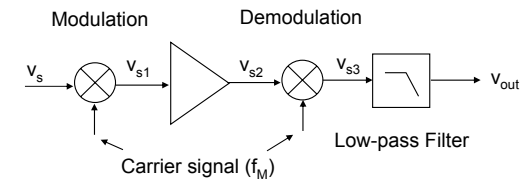
Input Transistor Optimization

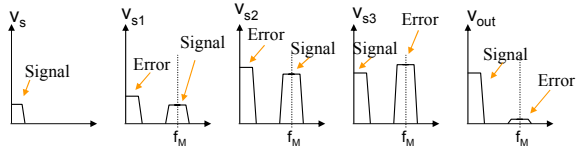




J. Wu et al., IEEE J. SSC, 2004

Chopper Stabilization

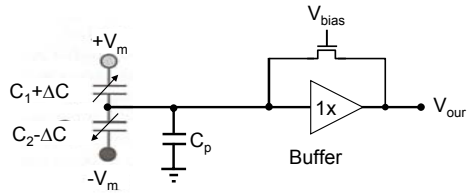




• Cancel amplifier offset and *1/f* noise

Continuous-Time Amplifiers

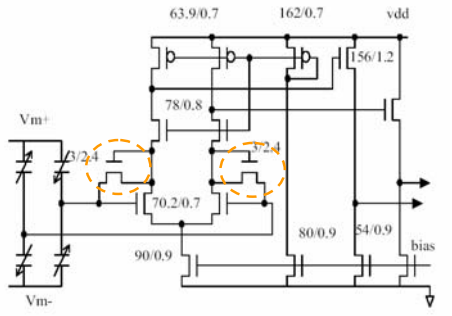
■ **Unity-gain Buffer With a Sub-threshold Biasing**



- **Use a feedback transistor operating at its subthreshold**
- **Bias voltage must be carefully set**

Continuous-Time Amplifiers

■ **Unity-gain Buffer With a Sub-threshold Biasing**

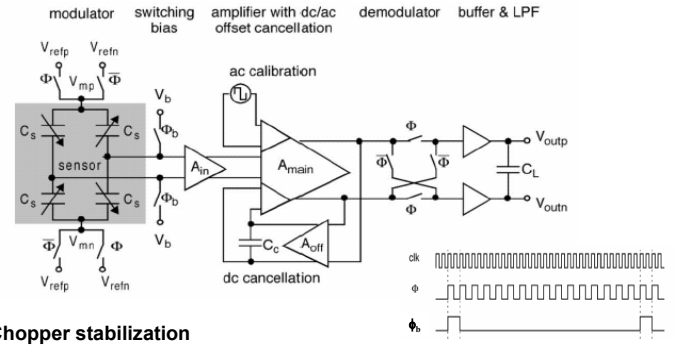


Luo, ISSCC 2003

- **Noise floor: 110 nV/rtHz**
- **Gain: 23 dB**
- **Switched-capacitor demodulator: Insensitive to dc offset**

Continuous-Time Amplifiers

■ **Chopper Stabilization with Periodic Reset**

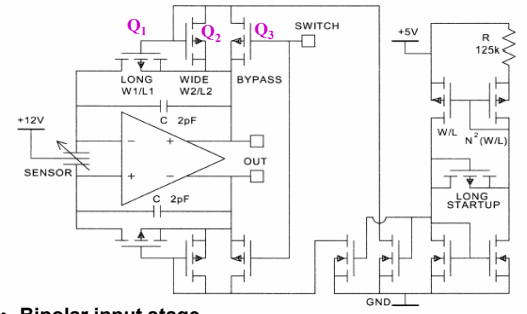


- **Chopper stabilization**
- **Optimal transistor sizing to minimize SNR**
- **DC offset cancellation**
- **Low-duty-cycle periodic reset for dc biasing**
- **Noise floor: ~50 nV/rtHz**

J. Wu et al., IEEE J. SSC, 2004

Continuous-Time Amplifiers

- **Transcapacitance Amplifier**

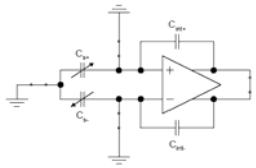


- **Bipolar input stage**
- **Controlled-impedance FET for biasing**
- **Q1 in triode-mode and Q2 saturated: 50MΩ**
- **Q3, 1/50 duty cycle: 2.5GΩ**
- **Temperature compensation: PTAT**
- **Noise floor: 12 zF/rtHz**

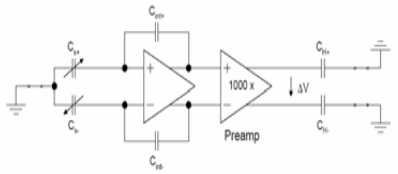
Geen et al., IEEE J. SSC, 2002

Discrete-Time

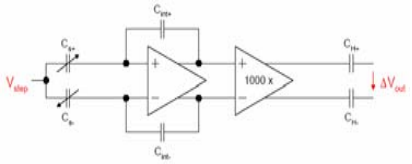
- **Correlated Double Sampling (CDS)**



Step 1: Set DC level



Step 2: Offset and 1/f noise cancellation

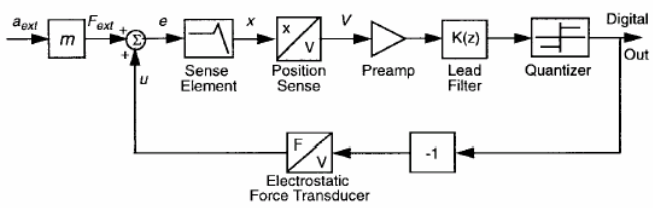


Step 3: Sensing ΔC_s

- Offset cancellation
- 1/f noise cancellation
- kT/C noise reduction
- but noise aliasing, switch noise still problematic
- Atialiasing needed

Boser, Transducers 1997

Force-balanced Feedback



- One-bit feedback
- Increased dynamic range
- Good linearity
- Digital output

- Higher cost
- Higher power consumption
- Not suitable for applications with high-g shock

Lemkin and Boser, IEEE J. SSC, 1999

CHS vs. SC

Interface type	Advantages	Disadvantages
Chopper-Stabilization	• Low noise: no aliasing, minimal number of noise sources • Low front-end power – SNR not limited by capacitor size • Suitable for discrete-component implementation	• Requires additional filtering and ADC for digital output • Requires large biasing resistors
Switch-Capacitor	• Robust DC biasing Good Linearity and accurate gain • Easy to integrate more functions (ADC, force-feedback) • Output can be digitized directly • No low-pass filter needed	• Higher noise – Noise folding, charge injection • Large capacitors needed for low kT/C noise

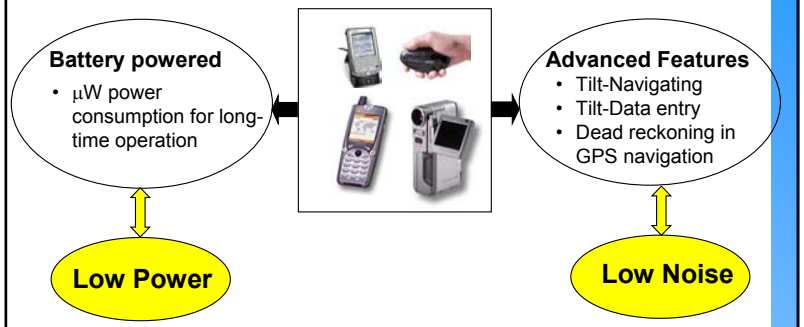
Other Groups: U-Mich, GA Tech, UF, …

Design Example:

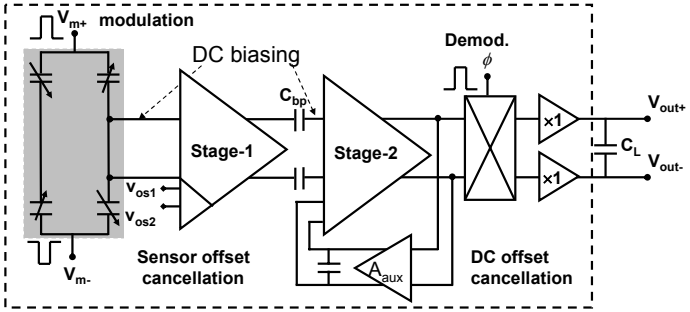
Low-power low-noise interface circuit for accelerometers (by D. Fang)

Example: Low-power Low-noise Accelerometer

- Low-Power and Low-Noise Operation are Critical in Emerging Applications

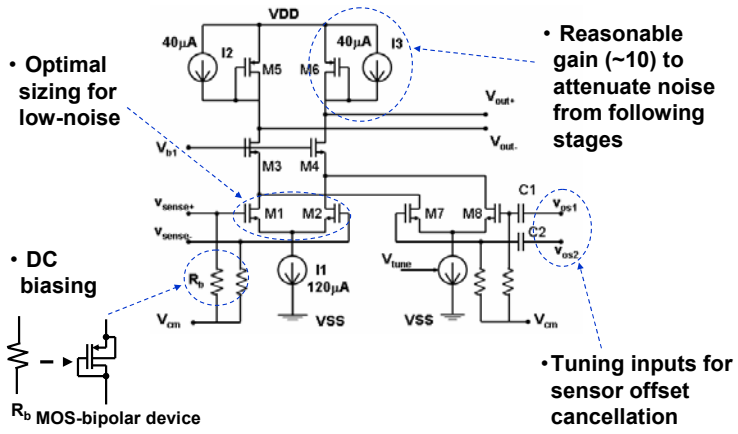


Low-Power Low-Noise Architecture



- **Low Noise**
  - Noise Matching
  - High chopping frequency (0.1~2 MHz)
- **Low Power**
  - 2-stage, open-loop
  - Stage-1 optimized for noise
  - Staeg-2 optimized for signal swing and linearity

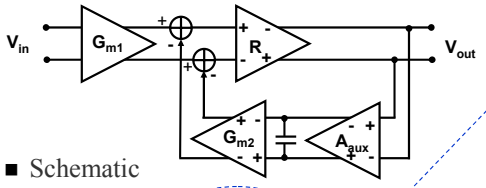
Interface Circuit Design: Stage-1



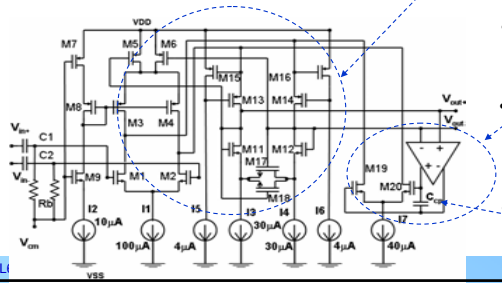
- **Optimal sizing for low-noise**
- **Reasonable gain (~10) to attenuate noise from following stages**
- **DC biasing**
- **Tuning inputs for sensor offset cancellation**

Interface Circuit Design: Stage-2

- Block Diagram



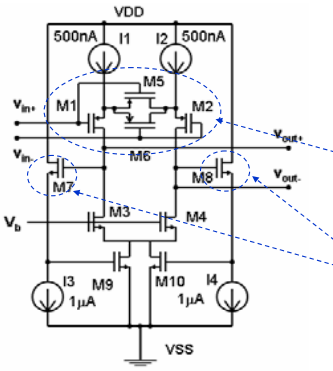
- Schematic



- Folded-cascode with linearized trans-conductance load
- Optimized for linearity and signal swing
- Medium gain (10~20)
- DC feedback to cancel offset
- On-chip low-pass capacitor (20pF)

Interface Circuit Design: Auxiliary Amplifier

- Used in DC feedback loop within stage-2



- Form a low-pass g_m-c filter ($f_{cut-off}$ is about 50 kHz) with on-chip capacitor C_{cp}
- Low sink current and source degeneration are used to get very low g_m (a few μA/V)
- M7 and M8 are used as level-shifter to keep common-mode level of outputs of the auxiliary amplifier in the right range

Experimental Results

Chopping freq.	50 kHz ~ 1 MHz
Gain	40 dB
DC offset	<1 mV
Sensor offset attenuation	>26 dB
noise	24 nv/√Hz, chopping at 1 MHz (simulation)
Power	330 μA × 3.3 V

Fang and Xie, IASTED CSS 2004

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