DATA SHEET

NE567/SE567
Tone decoder/phase-locked loop

Product data
Supersedes data of 1992 Apr 15

2002 Sep 25
DESCRIPTION
The NE567/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

FEATURES
• Wide frequency range (0.01 Hz to 500 kHz)
• High stability of center frequency
• Independently controllable bandwidth (up to 14%)
• High out-band signal and noise rejection
• Logic-compatible output with 100 mA current sinking capability
• Inherent immunity to false signals
• Frequency adjustment over a 20-to-1 range with an external resistor

APPLICATIONS
• Touch-Tone® decoding
• Carrier current remote controls
• Ultrasonic controls (remote TV, etc.)
• Communications paging
• Frequency monitoring and control
• Wireless intercom
• Precision oscillator

BLOCK DIAGRAM

![Block Diagram](image)

Figure 1. Pin configuration

Figure 2. Block Diagram

Touch-Tone is a registered trademark of AT&T.
EQUIVALENT SCHEMATIC

Figure 3. Equivalent schematic
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>ORDER CODE</th>
<th>DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
<th>DWG #</th>
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<tbody>
<tr>
<td>NE567D</td>
<td>SO8: plastic small outline package; 8 leads; body width 3.9 mm</td>
<td>0 °C to +70 °C</td>
<td>SOT96-1</td>
</tr>
<tr>
<td>NE567N</td>
<td>DIP8: plastic dual in-line package; 8 leads (300 mil)</td>
<td>0 °C to +70 °C</td>
<td>SOT97-1</td>
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<tr>
<td>SE567D</td>
<td>SO8: plastic small outline package; 8 leads; body width 3.9 mm</td>
<td>−55 °C to +125 °C</td>
<td>SOT96-1</td>
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<tr>
<td>SE567N</td>
<td>DIP8: plastic dual in-line package; 8 leads (300 mil)</td>
<td>−55 °C to +125 °C</td>
<td>SOT97-1</td>
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</table>

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATING</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>T_{amb}</td>
<td>Operating temperature</td>
<td>0 to +70</td>
<td>°C</td>
</tr>
<tr>
<td>NE567</td>
<td></td>
<td>−55 to +125</td>
<td>°C</td>
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<tr>
<td>SE567</td>
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<td></td>
<td></td>
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<tr>
<td>V_{CC}</td>
<td>Operating voltage</td>
<td>10</td>
<td>V</td>
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<tr>
<td>V+</td>
<td>Positive voltage at input</td>
<td>0.5 +V_S</td>
<td>V</td>
</tr>
<tr>
<td>V−</td>
<td>Negative voltage at input</td>
<td>−10</td>
<td>V_{DC}</td>
</tr>
<tr>
<td>V_{OUT}</td>
<td>Output voltage (collector of output transistor)</td>
<td>15</td>
<td>V_{DC}</td>
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<tr>
<td>T_{slg}</td>
<td>Storage temperature range</td>
<td>−65 to +150</td>
<td>°C</td>
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<td>P_D</td>
<td>Power dissipation</td>
<td>300</td>
<td>mW</td>
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## DC ELECTRICAL CHARACTERISTICS

V+ = 5.0 V, T\textsubscript{amb} = 25 °C, unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SE567</th>
<th>NE567</th>
<th>UNIT</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
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<tr>
<td>fO</td>
<td>Highest center frequency</td>
<td></td>
<td>500</td>
<td>500</td>
<td>kHz</td>
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<td>fO</td>
<td>Center frequency stability(^2)</td>
<td>–55 °C to +125 °C</td>
<td>35 ±140</td>
<td>35 ±140</td>
<td>ppm/°C</td>
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<td></td>
<td></td>
<td>0 °C to +70 °C</td>
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<td>35 ±60</td>
<td>ppm/°C</td>
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<tr>
<td>fO</td>
<td>Center frequency distribution</td>
<td>(f_{0} = 100\text{kHz} = \frac{1}{1.1R_{1}C_{1}})</td>
<td>–10</td>
<td>0</td>
<td>+10</td>
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<tr>
<td>fO</td>
<td>Center frequency shift with supply voltage</td>
<td>(f_{0} = 100\text{kHz} = \frac{1}{1.1R_{1}C_{1}})</td>
<td>0.5</td>
<td>1</td>
<td>0.7</td>
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### Detection bandwidth

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<thead>
<tr>
<th>BW</th>
<th>Largest detection bandwidth fO = 100kHz = \frac{1}{1.1R_{1}C_{1}}</th>
<th>12</th>
<th>14</th>
<th>16</th>
<th>10</th>
<th>14</th>
<th>18</th>
<th>% of fO</th>
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<td>Largest detection bandwidth skew</td>
<td>2</td>
<td>4</td>
<td></td>
<td>3</td>
<td>6</td>
<td></td>
<td>% of fO</td>
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<tr>
<td>BW</td>
<td>Largest detection bandwidth—variation with temperature V\textsubscript{l} = 300 mV\textsubscript{RMS}</td>
<td>±0.1</td>
<td>±0.1</td>
<td>%/°C</td>
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<td>BW</td>
<td>Largest detection bandwidth—variation with supply voltage V\textsubscript{l} = 300 mV\textsubscript{RMS}</td>
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<td>±2</td>
<td>%/V</td>
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### Input

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<thead>
<tr>
<th>R\textsubscript{IN}</th>
<th>Input resistance</th>
<th>15</th>
<th>20</th>
<th>25</th>
<th>15</th>
<th>20</th>
<th>25</th>
<th>kΩ</th>
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<tr>
<td>V\textsubscript{l}</td>
<td>Smallest detectable input voltage(^4)</td>
<td>10</td>
<td>15</td>
<td>10</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>mV\textsubscript{RMS}</td>
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<tr>
<td></td>
<td>Largest no-output input voltage(^4)</td>
<td>20</td>
<td>25</td>
<td>20</td>
<td>25</td>
<td>mV\textsubscript{RMS}</td>
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<tr>
<td></td>
<td>Greatest simultaneous out-band signal-to-in-band signal ratio</td>
<td>+6</td>
<td>+6</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Minimum input signal to wide-band noise ratio</td>
<td>B\textsubscript{n} = 140 kHz</td>
<td>–6</td>
<td>–6</td>
<td>dB</td>
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### Output

<table>
<thead>
<tr>
<th>fO/20</th>
<th>Fastest on-off cycling rate</th>
<th></th>
<th>fO/20</th>
<th></th>
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<tr>
<td></td>
<td>“1” output leakage current</td>
<td>V\textsubscript{B} = 15 V</td>
<td>0.01</td>
<td>25</td>
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<tr>
<td></td>
<td>“0” output voltage</td>
<td>I\textsubscript{L} = 30 mA</td>
<td>0.2</td>
<td>0.4</td>
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<tr>
<td></td>
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<td>I\textsubscript{L} = 100 mA</td>
<td>0.6</td>
<td>1.0</td>
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<td></td>
<td>Output fall time(^3)</td>
<td>R\textsubscript{L} = 50 Ω</td>
<td>30</td>
<td>30</td>
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<tr>
<td></td>
<td>Output rise time(^3)</td>
<td>R\textsubscript{L} = 50 Ω</td>
<td>150</td>
<td>150</td>
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### General

<table>
<thead>
<tr>
<th>(V\textsubscript{CC})</th>
<th>Operating voltage range</th>
<th>4.75</th>
<th>9.0</th>
<th>4.75</th>
<th>9.0</th>
<th>V</th>
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<tr>
<td>Supply current quiescent</td>
<td>R\textsubscript{L} = 20 kΩ</td>
<td>6</td>
<td>8</td>
<td>7</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Supply current—activated</td>
<td>R\textsubscript{L} = 20 kΩ</td>
<td>11</td>
<td>13</td>
<td>12</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>Q0</td>
<td>Quiescent power dissipation</td>
<td>30</td>
<td>35</td>
<td>mW</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Frequency determining resistor R\textsubscript{1} should be between 2 and 20 kΩ.
2. Applicable over 4.75 V to 5.75 V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R\textsubscript{L} network selected to eliminate pulsing during turn-on and turn-off.
4. With R\textsubscript{2} = 130 kΩ from Pin 1 to V+ See Figure 16.
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. Bandwidth vs. input signal amplitude

Figure 5. Largest detection bandwidth vs. operating frequency

Figure 6. Detection bandwidth as a function of $C_2$ and $C_3$

Figure 7. Typical supply current vs. supply voltage

Figure 8. Greatest number of cycles before output

Figure 9. Typical output voltage vs. temperature
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 10. Typical frequency drift with temperature (Mean and SD)

Figure 11. Typical frequency drift with temperature (Mean and SD)

Figure 12. Typical frequency drift with temperature (Mean and SD)

Figure 13. Center frequency temperature coefficient (Mean and SD)

Figure 14. Center frequency shift with supply voltage change vs. operating frequency

Figure 15. Typical bandwidth variation temperature
DESIGN FORMULAS

\[ f_O = \frac{1}{TR_1C_1} \]

\[ BW = 1070 \sqrt{\frac{V_I}{f_OC_2}} \text{ in } \% \text{ of } f_O \]

\[ V_I \leq 200mV_{RMS} \]

Where

\[ V_I = \text{Input voltage (V RMS)} \]

\[ C_2 = \text{Low-pass filter capacitor (} \mu \text{F)} \]

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f₀)
The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection bandwidth (BW)
The frequency range, centered about f₀, within which an input signal above the threshold voltage (typically 20 mV RMS) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock range
The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection band skew
A measure of how well the detection band is centered about the center frequency, f₀. The skew is defined as:

\[ \frac{(f_{\text{MAX}} + f_{\text{MIN}} - 2f_O)}{2f_O} \]

where fMAX and fMIN are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS
Figure 16 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R₁, C₁, C₂, and C₃.

1. Select R₁ and C₁ for the desired center frequency. For best temperature stability, R₁ should be between 2 kΩ and 20 kΩ, and the combined temperature coefficient of the R₁C₁ product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low-pass capacitor, C₂, by referring to Figure 4, ‘Bandwidth vs. input signal amplitude’. If the input amplitude variation is known, the appropriate value of f₀ ⋅ C₂ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C₂ may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mV RMS. The bandwidth, as noted on the graph, is then controlled solely by the f₀ ⋅ C₂ product (f₀ (Hz), C₂ (µF)).

3. The value of C₃ is generally non-critical. C₃ sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C₃ is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C₃ is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C₃ passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C₃ is 2C₂.

4. Optional resistor R₂ sets the threshold for the largest “no output” input voltage. A value of 130 kΩ is used to assure the tested limit of 10 mV RMS min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the “optional controls” section which follows.

TYPICAL RESPONSE
Figure 17. Typical response

Response to 100mV RMS Tone Burst

Response to Same Input Tone Burst With Wideband Noise

NOTE:

RL = 100Ω

S/N = –6dB

Noise Bandwidth = 140Hz
AVAILABLE OUTPUTS (Figure 18)
The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 \( f_0 \) with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude \((+V - 2V_{BE}) \approx (+V - 1.4V)\) having a DC average of \(+V/2\). A 1k\( \Omega \) load may be driven from pin 5. Pin 6 is an exponential triangle of 1V P-P with an average DC level of \(+V/2\). Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS
A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200 mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at \(f_0/3\), \(f_0/5\), etc.

2. The 567 will lock onto signals near \((2n+1) f_0\), and will give an output for signals near \((4n+1) f_0\) where \(n = 0, 1, 2,\) etc. Thus, signals at \(5f_0\) and \(9f_0\) can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200 mV RMS) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20 ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01\( \mu \)F or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.
**SPEED OF OPERATION**

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when $C_2$ is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of $C_2$ and $C_3$ which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O} \mu F$$

$$C_3 = \frac{260}{f_O} \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent $C_3$ voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

**OPTIONAL CONTROLS** (Figure 19)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

**SENSITIVITY ADJUSTMENT** (Figure 19)

When operated as a very narrow-band detector (less than 8%), both $C_2$ and $C_3$ are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10 mV or lower).

![Sensitivity Adjustment Diagram](SL00556)

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, $C_2$ and $C_3$ are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.
CHATTER PREVENTION (Figure 20)
Chatter occurs in the output stage when C₃ is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 20. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C₃ large, the feedback circuit will enable faster operation of the 567 by allowing C₃ to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 21)
When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since Rᵥ also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.
**ALTERNATE METHOD OF BANDWIDTH REDUCTION** (Figure 22)

Although a large value of $C_2$ will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of $C_2$ be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of $R_B$ and $R_C$ can be eliminated and the $R_A$ resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

![Figure 22. BW reduction](image)

**NOTE:**

1. $\frac{10 \cdot k}{10 \cdot k + R}$ < $C_2$ < $\frac{1300 \cdot (10 \cdot k + R)}{10 \cdot k + R}$

Adjust control for symmetry of detection band edges about $f_0$.

---

**OUTPUT LATCHING** (Figure 23)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled-up to unlatch the output stage.

![Figure 23. Output latching](image)

**NOTE:**

$C_A$ prevents latch-up when power supply is turned on.

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**REDUCTION OF C1 VALUE**

For precision very low-frequency applications, where the value of $C_1$ becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the $R_1$ $C_1$ junction and Pin 6, so as to allow a higher value of $R_1$ and a lower value of $C_1$ for a given frequency.

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**PROGRAMMING**

To change the center frequency, the value of $R_1$ can be changed with a mechanical or solid state switch, or additional $C_1$ capacitors may be added by grounding them through saturating NPN transistors.
TYPICAL APPLICATIONS

NOTES:
Component values (Typical)
R₁ = 26.8 to 15kΩ
R₂ = 24.7kΩ
R₃ = 20kΩ
C₁ = 0.10mF
C₂ = 1.0mF 5V
C₃ = 2.2mF 6V
C₄ = 250µF 6V

Figure 24. Typical applications
TYPICAL APPLICATIONS  (continued)

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C3 is made large so as to delay turn-on of the top 567, decoding of sequential (f1 f2) tones is possible.

NOTES:
R2 = R1/5
Adjust R1 so that φ = 90° with control midway.

Figure 25. Typical applications (cont.)
TYPICAL APPLICATIONS (continued)

- Oscillator With Quadrature Output
- Oscillator With Double Frequency Output
- Precision Oscillator With 20ns Switching
- Pulse Generator With 25% Duty Cycle
- Precision Oscillator to Switch 100mA Loads
- Pulse Generator

Figure 26. Typical applications (cont.)
SO8: plastic small outline package; 8 leads; body width 3.9 mm

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

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<th>UNIT</th>
<th>A_{max}</th>
<th>A_1</th>
<th>A_2</th>
<th>A_3</th>
<th>b_p</th>
<th>c</th>
<th>D^{(1)}</th>
<th>E^{(2)}</th>
<th>e</th>
<th>H_E</th>
<th>L</th>
<th>L_P</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
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<tr>
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<td>0.069</td>
<td>0.010</td>
<td>0.057</td>
<td>0.01</td>
<td>0.019</td>
<td>0.010</td>
<td>0.0075</td>
<td>0.019</td>
<td>0.16</td>
<td>0.244</td>
<td>0.228</td>
<td>0.041</td>
<td>0.039</td>
<td>0.028</td>
<td>0.01</td>
<td>0.01</td>
<td>0.004</td>
</tr>
</tbody>
</table>

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

<table>
<thead>
<tr>
<th>OUTLINE VERSION</th>
<th>REFERENCES</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT96-1</td>
<td>IEC 078E03</td>
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</table>

2002 Sep 25

16
DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A max.</th>
<th>A 1 min.</th>
<th>A 2 max.</th>
<th>b</th>
<th>b 1</th>
<th>b 2</th>
<th>c</th>
<th>D (1)</th>
<th>E (1)</th>
<th>e</th>
<th>e 1</th>
<th>L</th>
<th>M  E</th>
<th>M  H</th>
<th>w</th>
<th>Z (1) max.</th>
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</thead>
<tbody>
<tr>
<td>mm</td>
<td>4.2</td>
<td>0.51</td>
<td>3.2</td>
<td>1.73</td>
<td>0.53</td>
<td>1.07</td>
<td>0.36</td>
<td>9.8</td>
<td>6.48</td>
<td>2.54</td>
<td>7.62</td>
<td>3.60</td>
<td>8.25</td>
<td>10.0</td>
<td>0.254</td>
<td>1.15</td>
</tr>
<tr>
<td>inches</td>
<td>0.17</td>
<td>0.020</td>
<td>0.13</td>
<td>0.068</td>
<td>0.021</td>
<td>0.042</td>
<td>0.014</td>
<td>0.39</td>
<td>0.26</td>
<td>0.10</td>
<td>0.30</td>
<td>0.14</td>
<td>0.32</td>
<td>0.39</td>
<td>0.01</td>
<td>0.045</td>
</tr>
</tbody>
</table>

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

<table>
<thead>
<tr>
<th>OUTLINE VERSION</th>
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<th>EUROPEAN PROJECTION</th>
<th>ISSUE DATE</th>
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<tbody>
<tr>
<td>SOT97-1</td>
<td>IEC 0503G01</td>
<td>JEDEC MO-001</td>
<td>SC-504-8</td>
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Tone decoder/phase-locked loop

Data sheet status

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Objective data</td>
<td>Development</td>
<td>This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary data</td>
<td>Qualification</td>
<td>This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.</td>
</tr>
<tr>
<td>Product data</td>
<td>Production</td>
<td>This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPON) procedure SNW-SQ-650A.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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