Layer Stack Guidelines

Layer stack defines:

- The ordering of the signal, power and GND layers
- The dielectric constant of the substrate
- The spacing between layers
- Optionally, the trace dimensions and minimum spacing.

Bear in mind, unlike VLSI, the greater the wiring density, the greater the production costs per square inch.

Start by designing the power and GND layers first.

This requires knowledge of signal rise times, the # of signals, the board dimensions and a guess on the trace width.

Estimate the *self-inductance* and *mutual inductance* using solid, hatched and fingers GND plane models.

- Fingers model: all traces interact.
- Hatched model: parallel traces interact.
- Plane model: only adjacent traces interact.

Layer Stack Guidelines

Try to use power and GND planes in pairs.

Single planes offset to one side or the other can cause warping.

Power planes can be used as *low-inductance* signal-current paths (just like GND planes) assuming **adequate *by-pass* capacitors** are installed.

In this case, transmission lines work as well as they do over a GND plane.

Transmission striplines routed between one power and GND layer or two power layers also work.

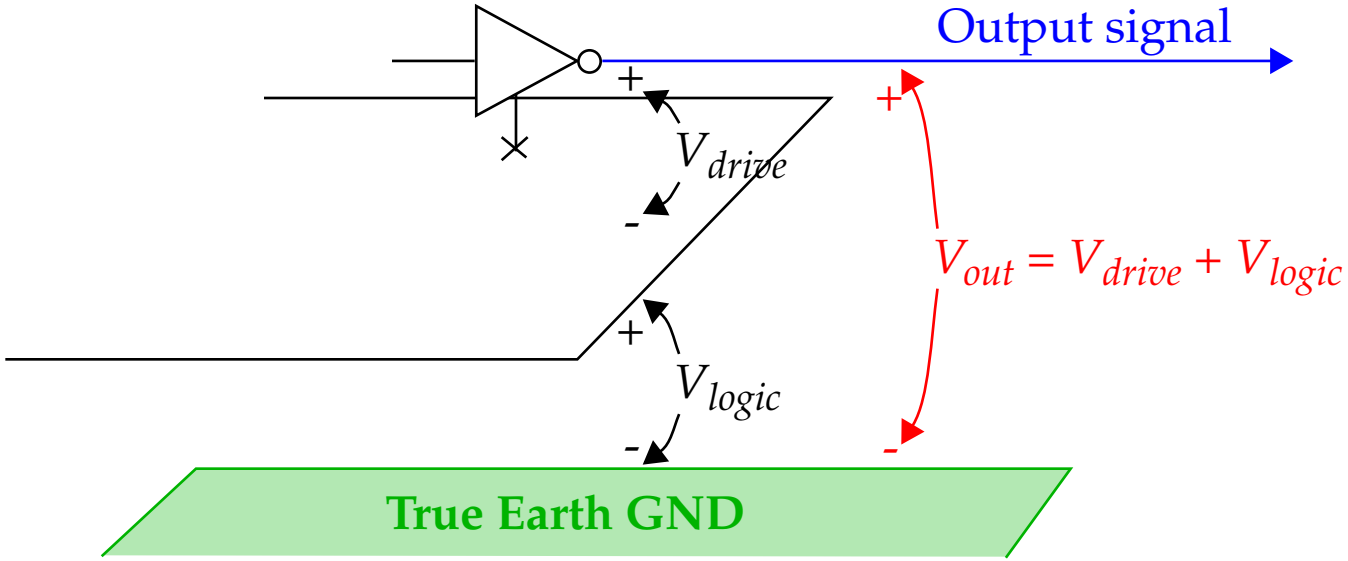
A **Chassis Layer** may be needed for driving signals off the board, otherwise external radiation will cause FCC problems.

Start by choosing a *low-speed* or *controlled rise time* driver.

Connecting the driver to the ordinary digital logic ground on board is probably not a good idea.

Chassis Layer

Consider the following:



Digital logic GNDs (on board) are notorious for *high-frequency* noise voltages.

These GNDs carry many returning currents acting across their self-inductance.

The high-frequency fluctuations are too small to cause trouble for digital logic on board.

However, the driver acts to broadcast the ground noise outside the cabinet, and the level will almost always exceed FCC limits.

Chassis Layer

One solution is to add a *chassis* plane adjacent to the GND plane on the board. This provides a high level of capacitance coupling between the planes.

The *chassis* layer is then screwed, soldered or welded to the external chassis along one **continuous** axis near the controlled rise-time driver.

This effectively shorts the digital GND plane to the chassis.

Ordinary capacitors will not function as a short between the digital logic GND and the *chassis* GND (lead inductance is too high).

The separate plane approach ensure the electrical separation of these two GNDs.

If separation is not important, short the digital GND directly to the chassis (no separate *chassis* GND plane is needed).

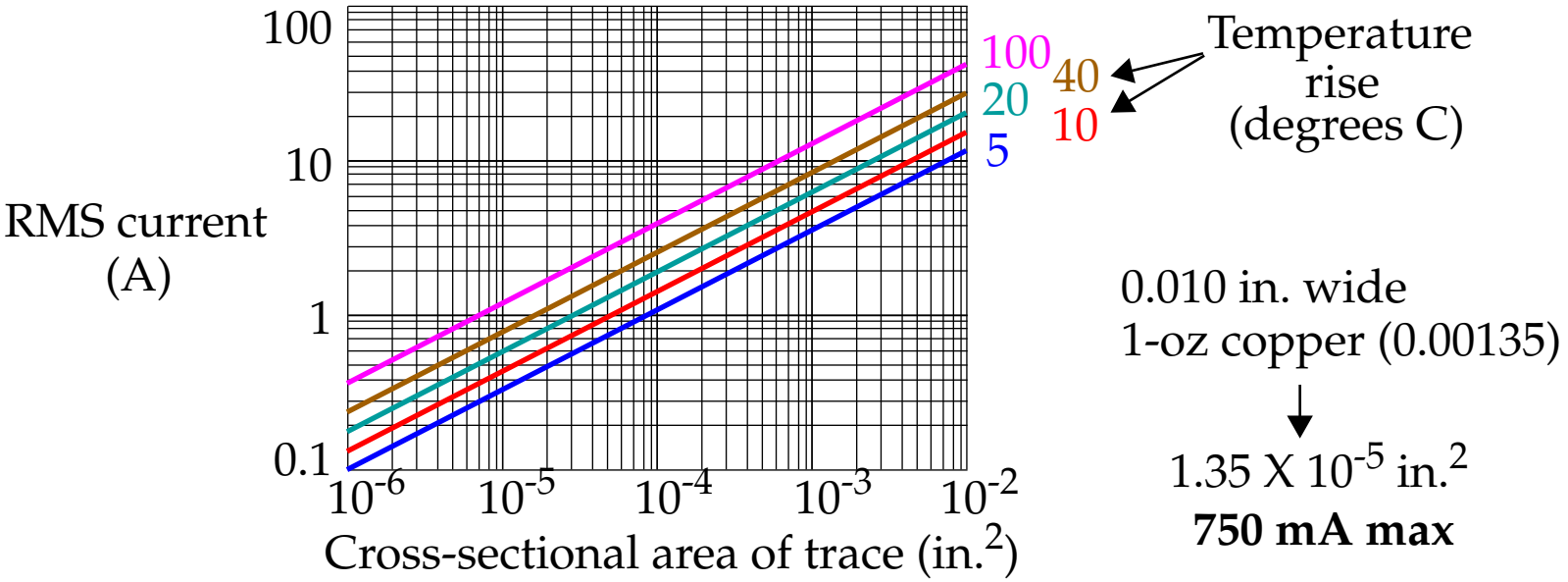
Selecting Trace Dimensions

Since board cost is proportional to the number of layers and its surface area, we tend to squeeze traces tightly together.

This increases *crosstalk* and reduces *routing area* available for power/GND.

Therefore, crosstalk, routing density and power are traded off to reduce cost.

The *power-handling* capacity of a PCB trace depends on its cross-sectional area and allowable temperature increase (typically 10 degrees).



Selecting Trace Dimensions

Power is rarely a serious constraint except for large power buses.

However, as *thin-film* technology becomes more widely available, this may become an issue.

Other than power, manufacturing tolerances also **lower bound** trace width.

Process	Min line width (in.)
Gold screened onto thick film substrate	0.010
Etched copper on epoxy board with plating	0.004
Etched copper on epoxy board with no plating	0.003
Gold evaporated onto thin film substrate and etched	0.001

Most designers won't use the min-width since **yield** goes down (cost up).

Also, *line width variations* and *variations in the electrical permittivity* of the substrate make it difficult to keep impedance within tolerance at min widths.

Trace width: Set by power, cost (yield) and impedance constraints.
Trace height: Set by impedance once trace width is established.

Selecting Trace Dimensions

Trace spacing is determined using our crosstalk formula:

$$\text{Crosstalk} = \frac{K}{1 + (D/H)^2}$$

Trace spacing is measured center-to-center and is called **trace pitch**.

The unused space between traces is called **trace separation**.

Therefore, trace width + trace separation = trace pitch.

Of course, using more layers allows larger pitches but higher cost.

So a trade-off between cost and crosstalk determines acceptable pitch.

The optimization problem is "route *N* connections of average wire length *X* using *M* layers".

Average wire length can be approximated from *Rent's rule.*

"Half the wires in a quadrant cross the quadrant boundary."

Selecting Trace Dimensions

From this, we can estimate the average *pitch* to route N connections:

$$p_{ave} = \frac{\sqrt{XY}}{N} 2.7M$$

Here, N is assumed distributed according to Rent's rule, X and Y are the dimensions of the board (in.), and M is the # of board layers.

For example, an 8X12 in. board having 800 connections routed on 4 layers yields a trace pitch of 0.132 in.

If the board has a lot of DIP *through-holes*, this requires traces to be run between the pins.

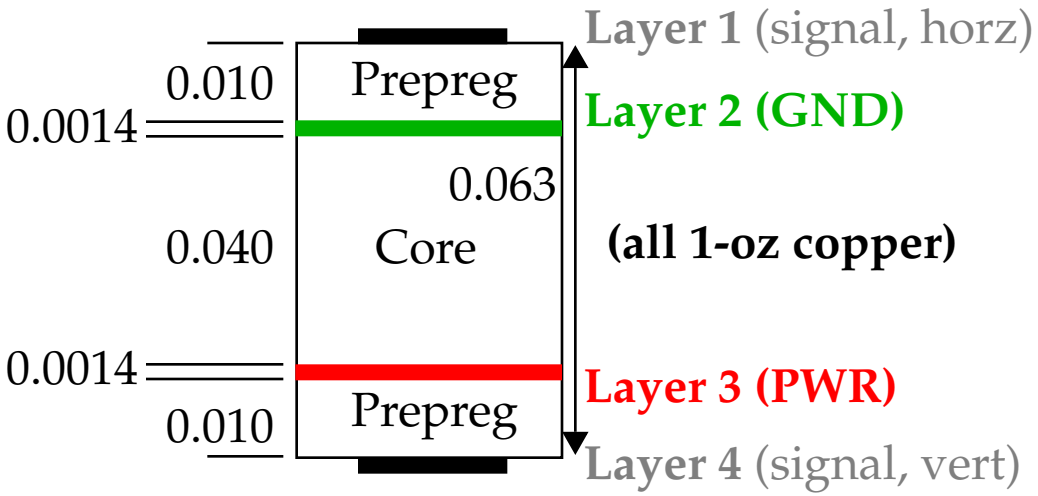
On average, no more than half of the space between pins can be filled.

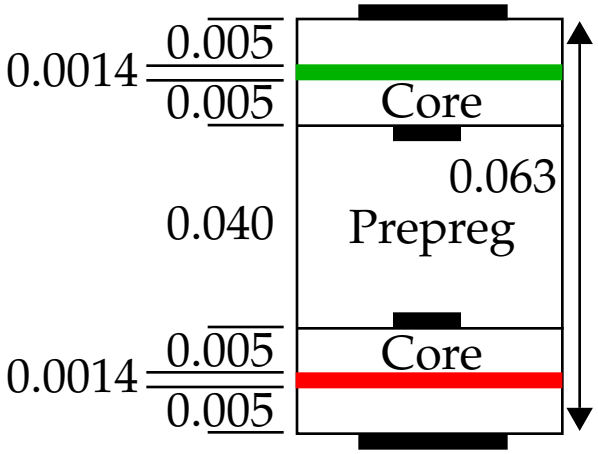
However, for *through-hole* boards, the average pitch (above eq) and the minimum pitch (from *crosstalk* considerations) can be very different.

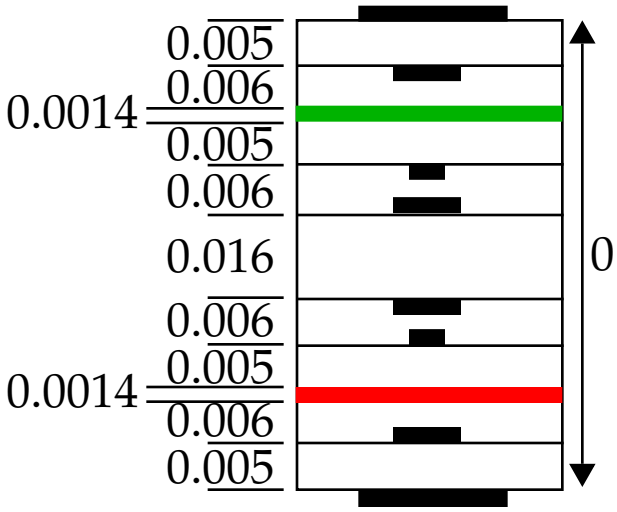
For *surface mount* boards, the average pitch and the minimum pitch may be similar for the inner layers.

Layer Stacks

4, 6 and 10 layer stacks are commonly used in the ordinary epoxy multilayer fabrication process.







microstrip

embedded microstrip

offset stripline

Alternating core and prepreg layers from top to bottom.

Layer Stacks

These layer stacks are designed for high-speed computer products embedded in well-shielded card cages.

Traces on successive layers traditionally run perpendicular with each other.

Core and *prepreg* are materials used in the substrate lamination process.

The fabrication process involves etching (for inner layers) two sided "cores" and then stacking the "cores" separated with "prepreg".

Prepreg melts into an epoxy glue when heated and pressed, and then hardens with the same dielectric constant as the core material.

Drilling is then performed exposing the inner metal layers and the *plating* step covers the inside surfaces of the drill holes.

For very high-speed boards, make the power and GND planes adjacent and add extra GND planes to isolate routing layers.

Use plenty of vias to tie the multiple GND planes together.