Basic Principle of
Plasma Display Panel

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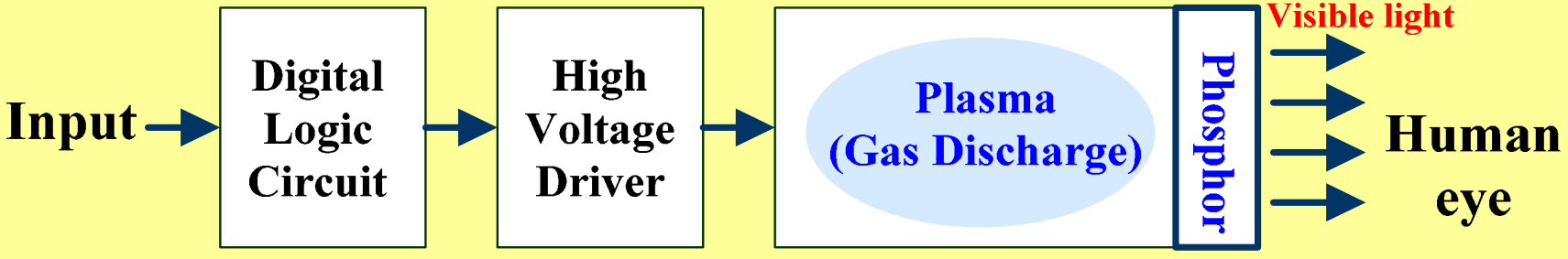
- **What is the ‘Plasma Display Panel’?**
- **Principle of AC-PDP**
- **Driving Mechanism**
- **Image in PDP**

Section 1: What is the ‘PDP’?

- **Definition of PDP**
- **What is ‘plasma’?**
- **Plasma 의 특징**
- **Applications of PDP**
- **Advantages of PDP**

What is the 'PDP'?

Definition



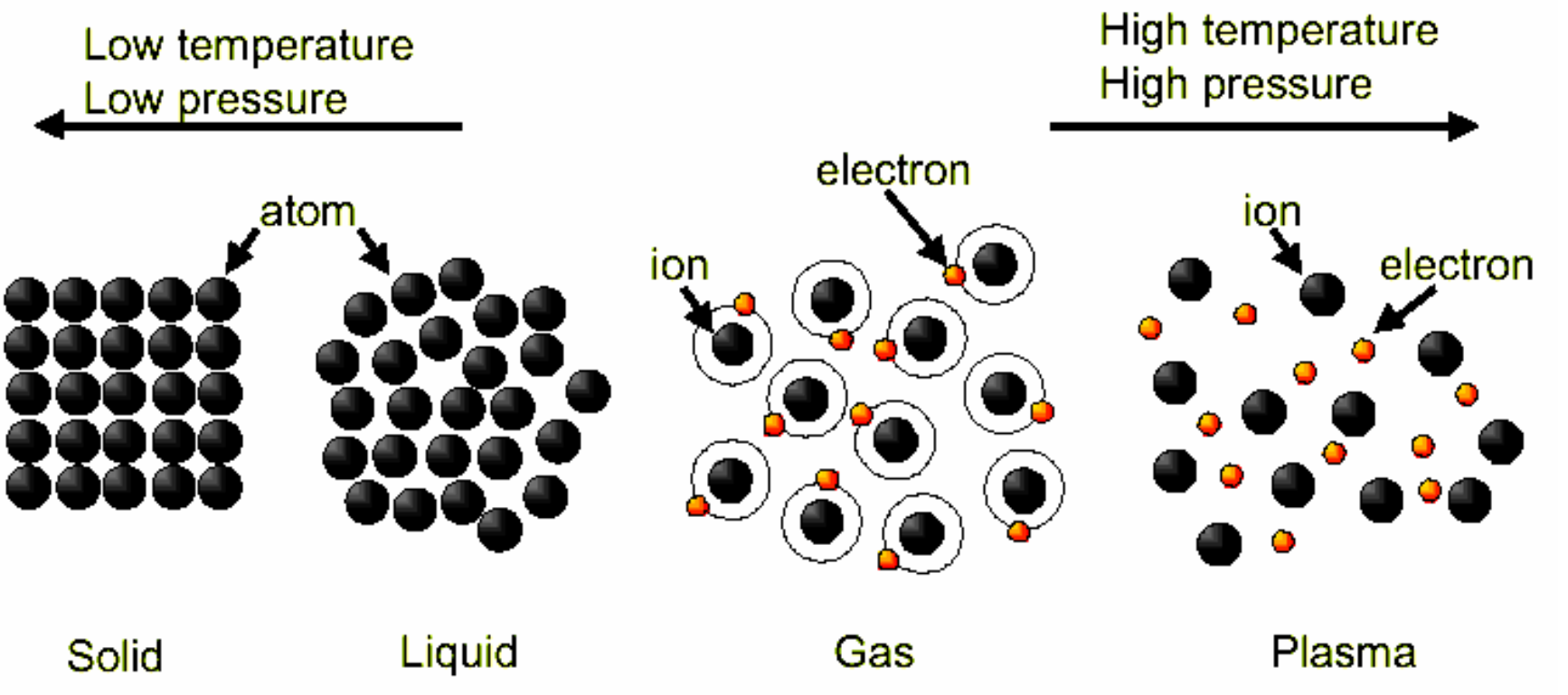
Plasma: 플라즈마 현상이용

Display: 문자 및 영상표시

Panel : 플라즈마 생성환경조성 및 픽셀형성

What is the ‘PDP’?

- What is ‘Plasma’?



What is the ‘PDP’?

- Plasma의 특징

I. 제 4의 물질상태

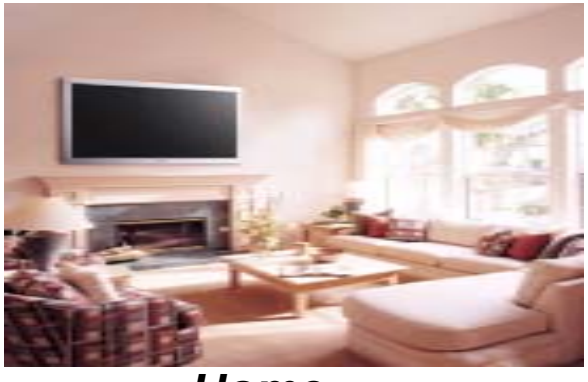
II. 전기적으로 준 중성상태를 유지

III. 다수의 전자(-)와 이온(+)들의 집합체

IV. 집단운동(collective behavior)

What is the ‘PDP’?

- Applications of PDP



Home

Public

Commercial

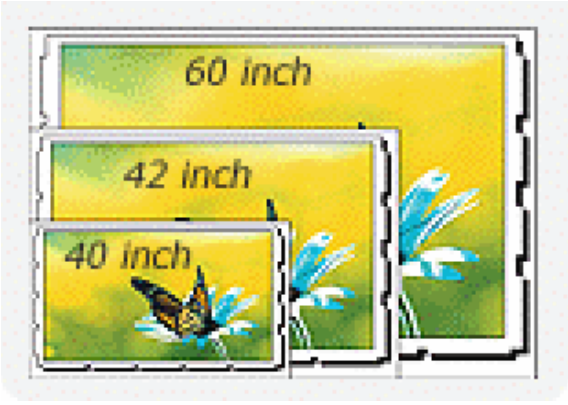
Entertainment

Industrial

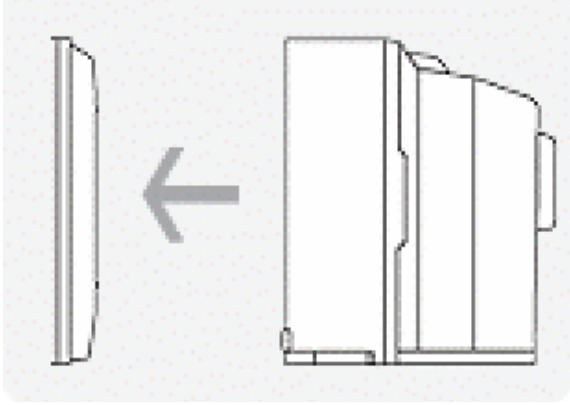
Business

What is the ‘PDP’?

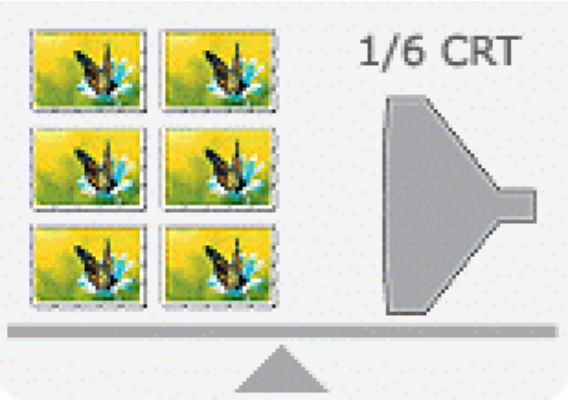
- Advantages of PDP



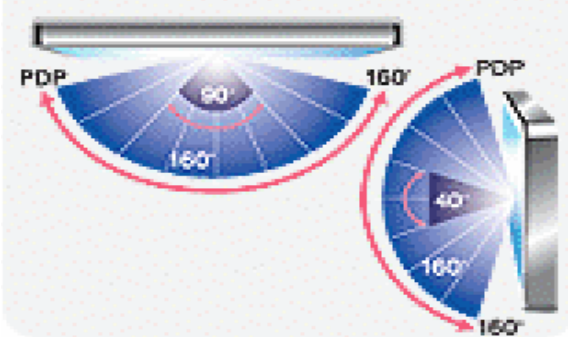
Large screen



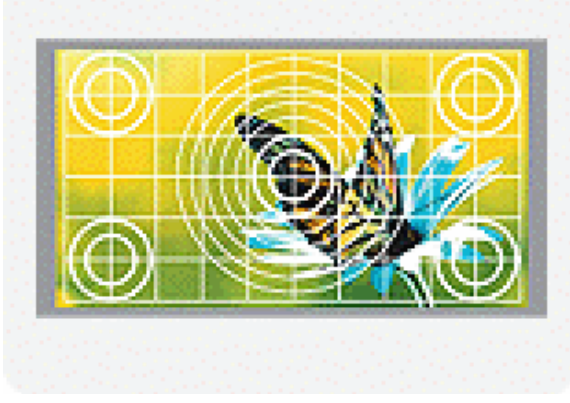
Thin



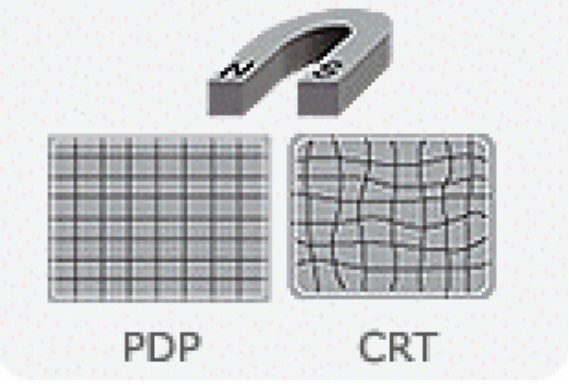
Lightweight



Wide viewing angle



Good Uniformity



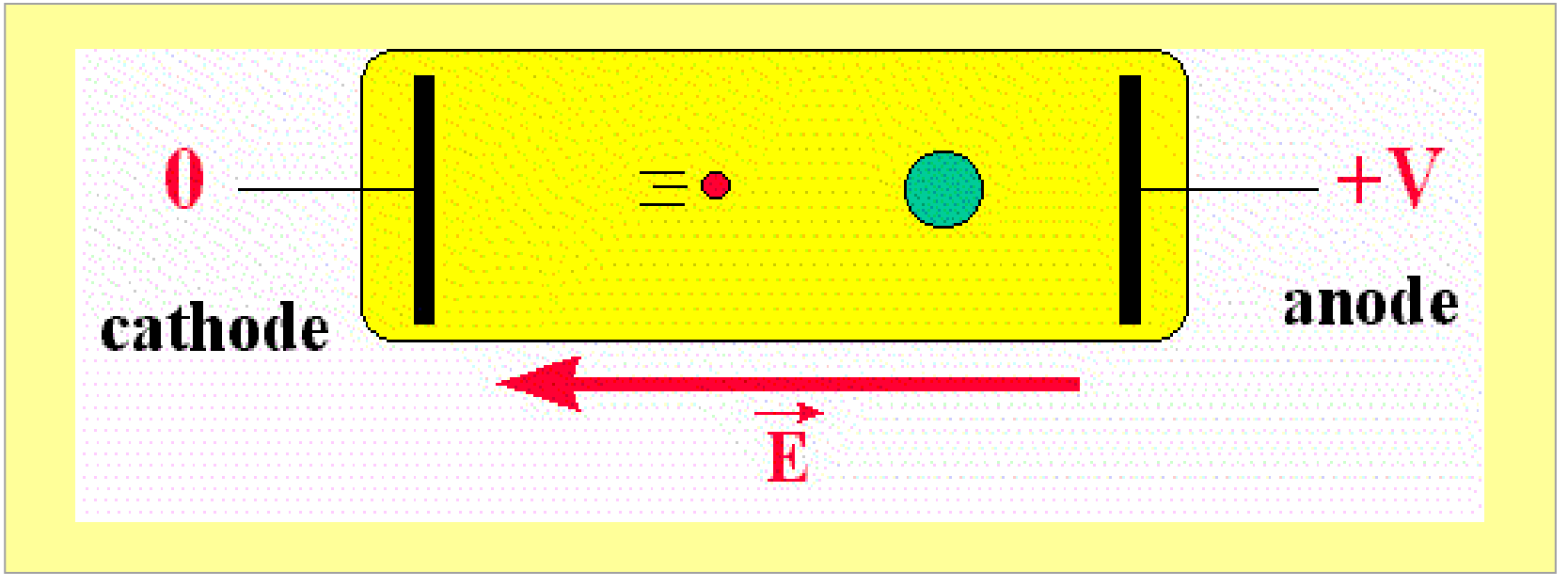
Distortion-Free with M.F.

Section 2: Principles of PDP

- Gas Discharge
- Structure of AC-PDP
- Gas in PDP
- Basic of AC discharge
- Emission of VUV
- Definition of Phosphor
- Spectrum of Visible light

Principles of PDP

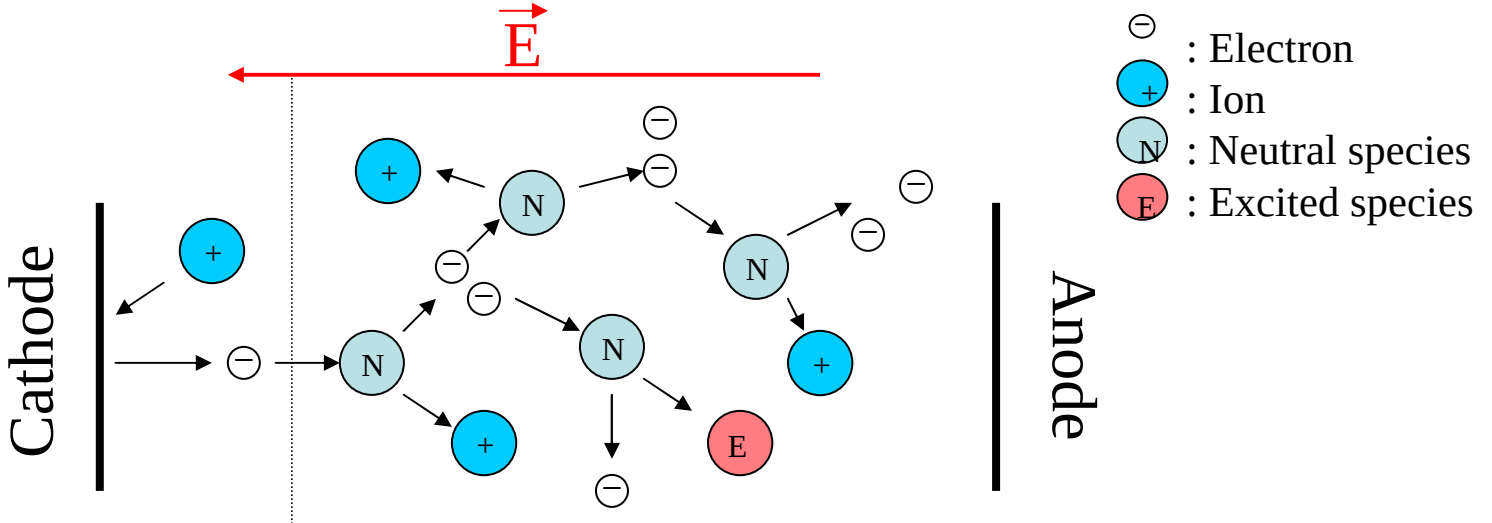
- 기체 방전(애니메이션)



●:전자 ●:중성자 ●:이온

Principles of PDP

기체 방전

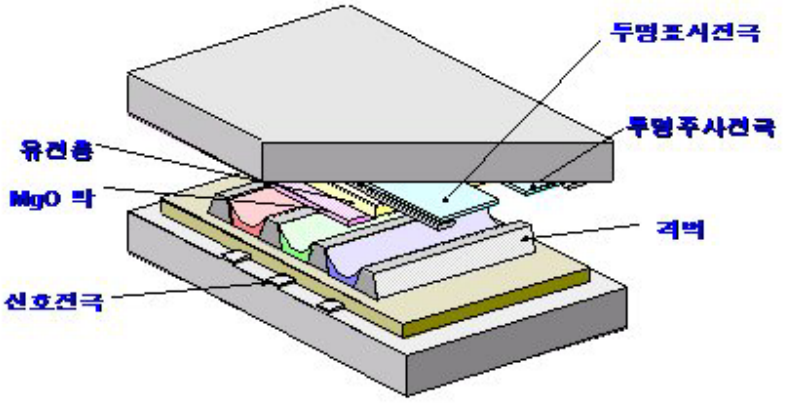


γ-process
(ion, excited species)

α-process
(electron)

Principles of PDP

AC Type PDP



➢방전공간에 형성되는 전계의 방향이 계속 바뀐다.

➢구조가 간단하다.

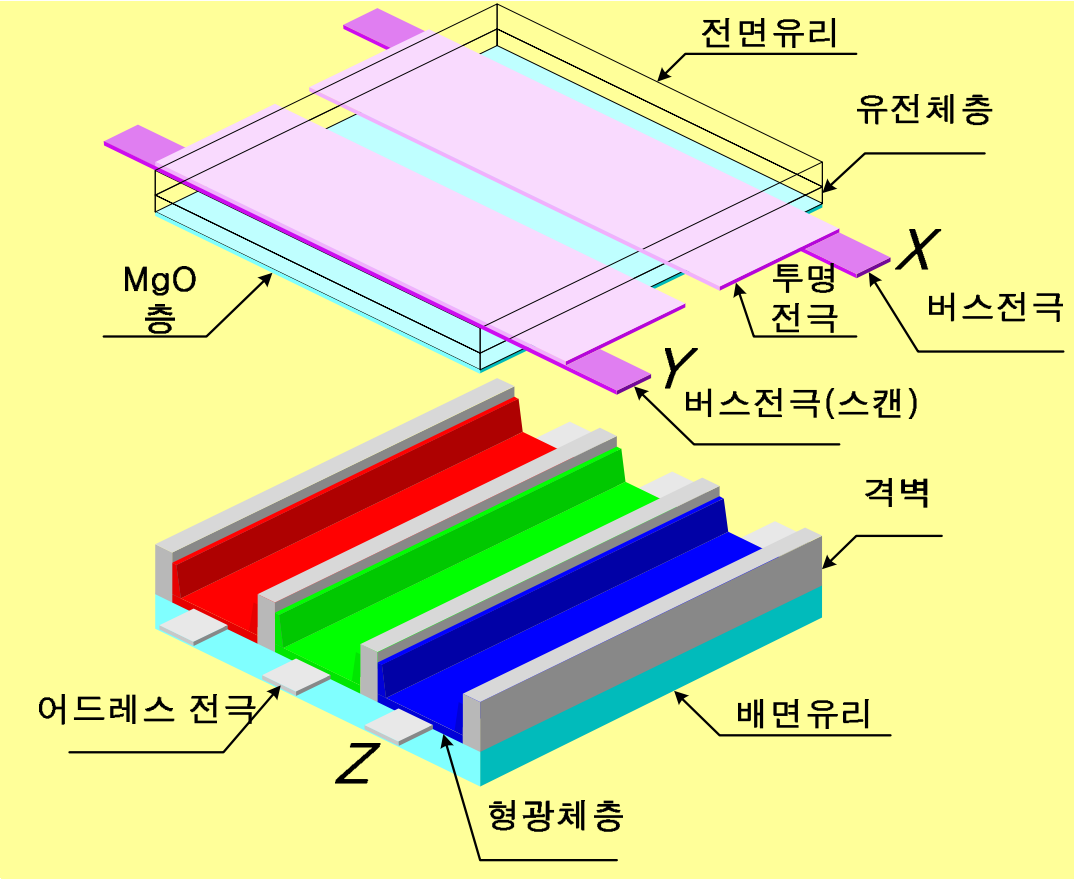
➢전극이 방전공간으로부터 보호되어 있다.

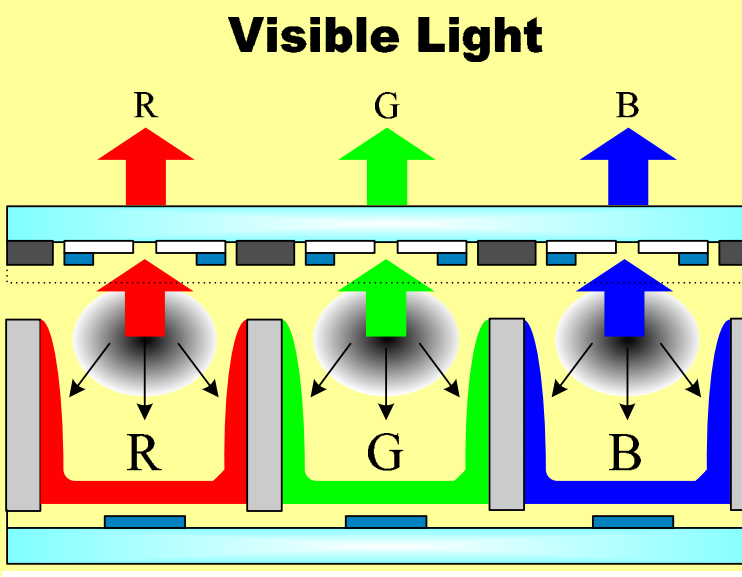
=>전극재료의 선택폭이 넓고 수명이 길다.

➢현재 상용화 되어있는 구조.

Principles of PDP

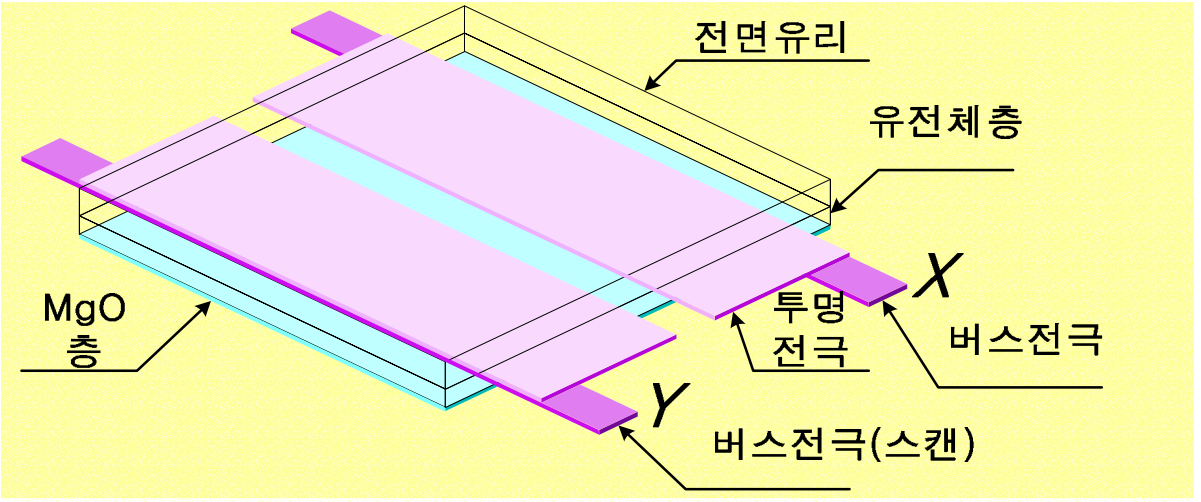
Structure of AC PDP





Principles of PDP

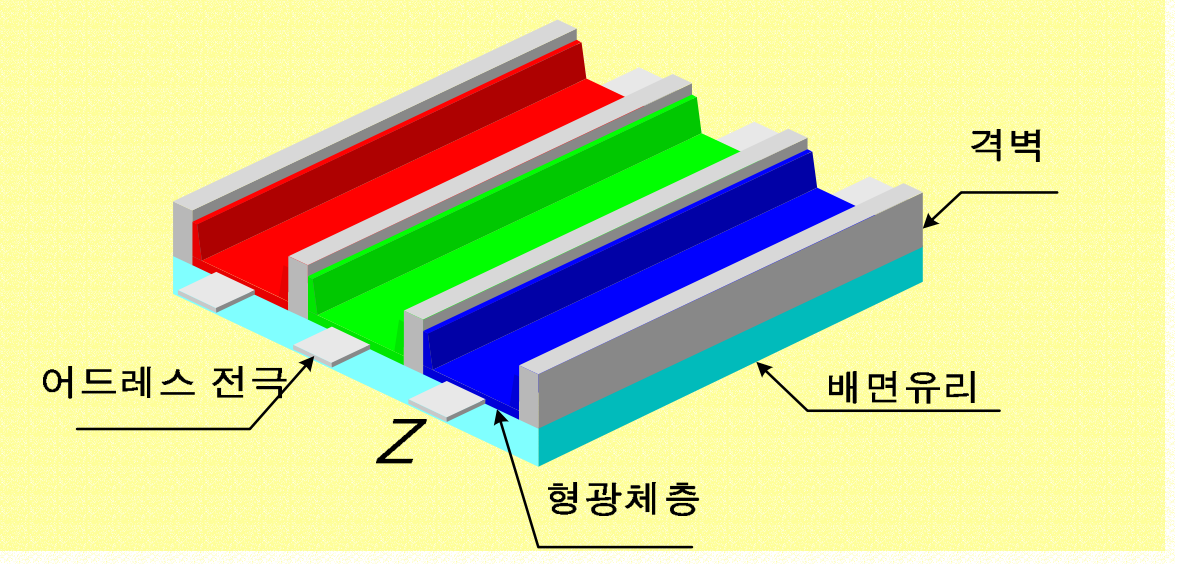
Structure of AC PDP(상판부분)



- 투명전극:방전공간에 전계를 형성시켜주는 역할
- 버스전극:투명전극의 저항을 줄여주는 역할
- 유전체층:메모리 기능을 가능하게 해준다.
- MgO층:이온충돌로부터 유전체를 보호한다.

Principles of PDP

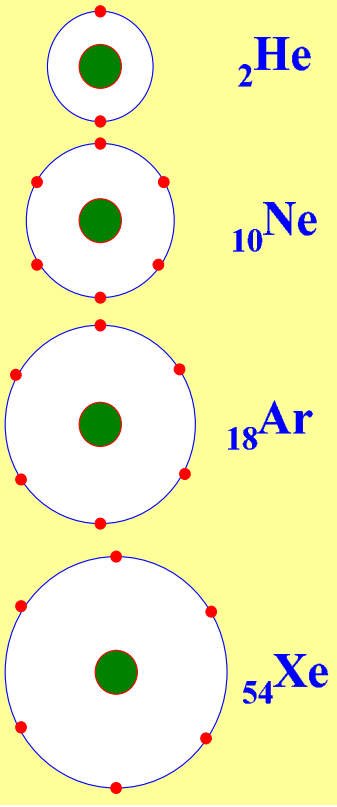
Structure of AC PDP(하판부분)



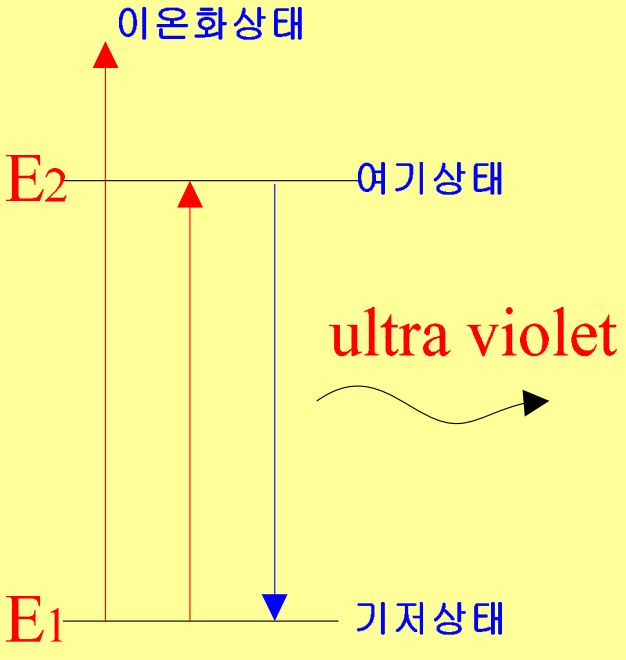
- 격벽:방전공간을 형성시켜주며 상호혼신을 방지한다.
- 형광체:VUV로부터 가시광 생성시킨다.
- 어드레스전극:각각의 픽셀에 영상데이타를 기입하는 역할

Principles of PDP

PDP에 사용되는 Gas



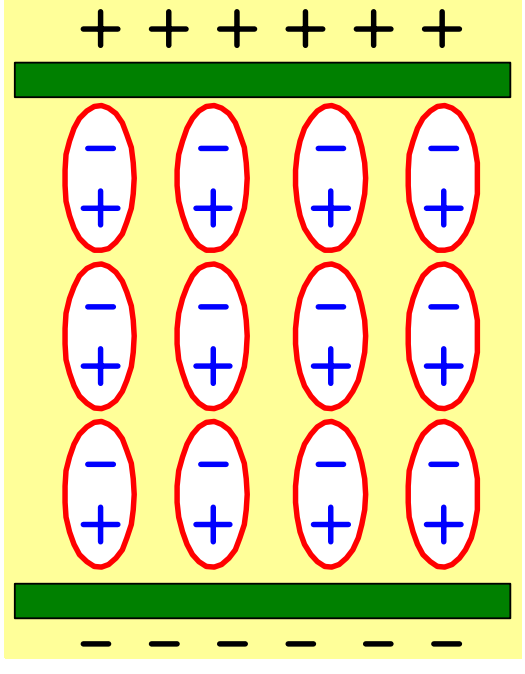
	여기전압	파장	전리전압
$_{2}He$	21.2eV	58.4nm	24.59eV
$_{10}Ne$	16.54eV	74.4nm	21.57eV
$_{18}Ar$	11.61eV	107nm	15.76eV
$_{54}Xe$	8.45eV	147nm	12.13eV

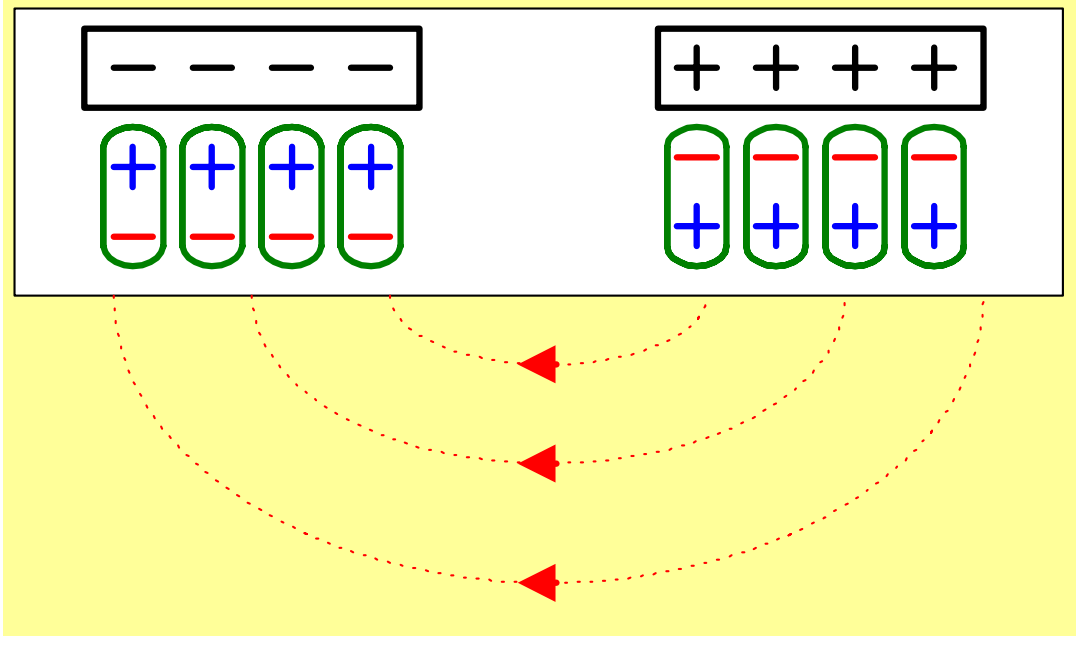


Principles of PDP

- AC 방전의 기초

Wall charge
Polarization of dielectric (유전체의 분극)

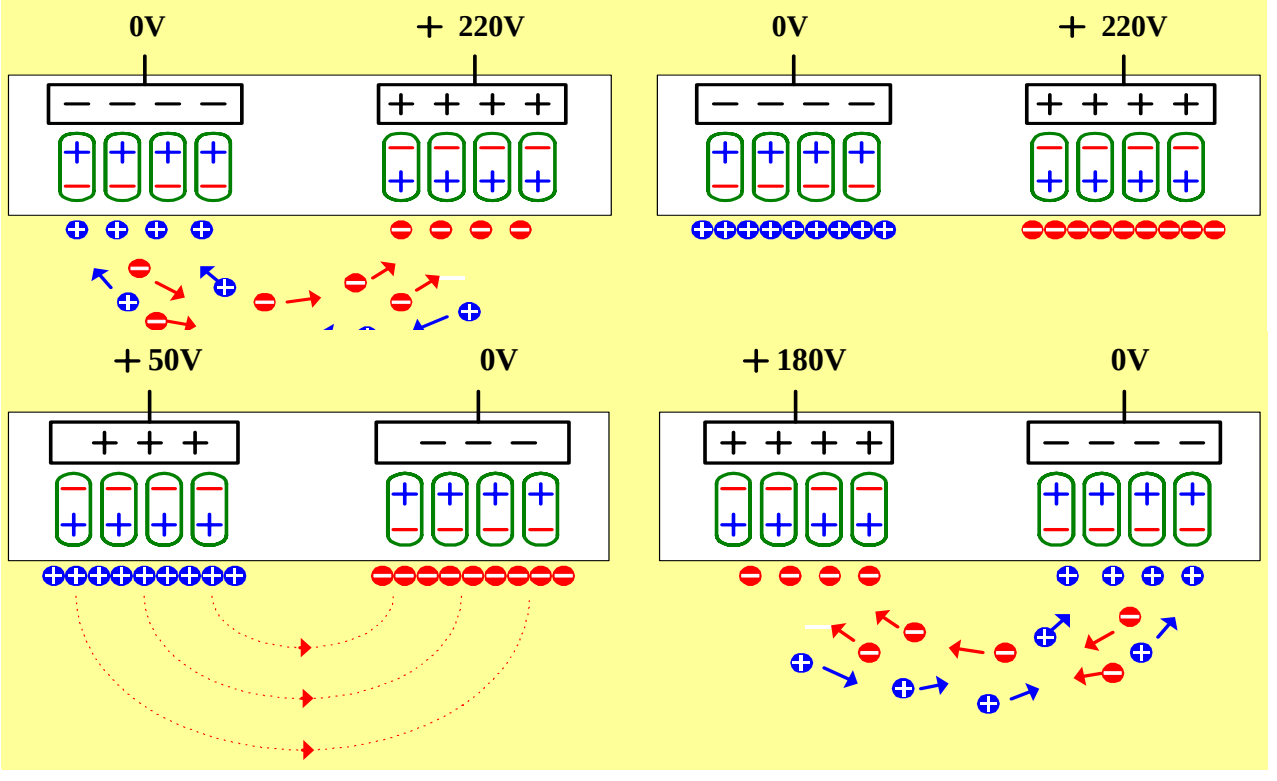




Principles of PDP

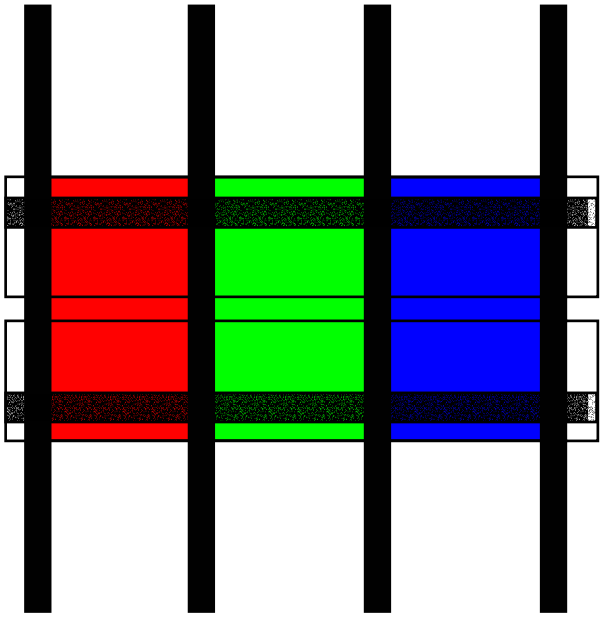
AC 방전의 기초

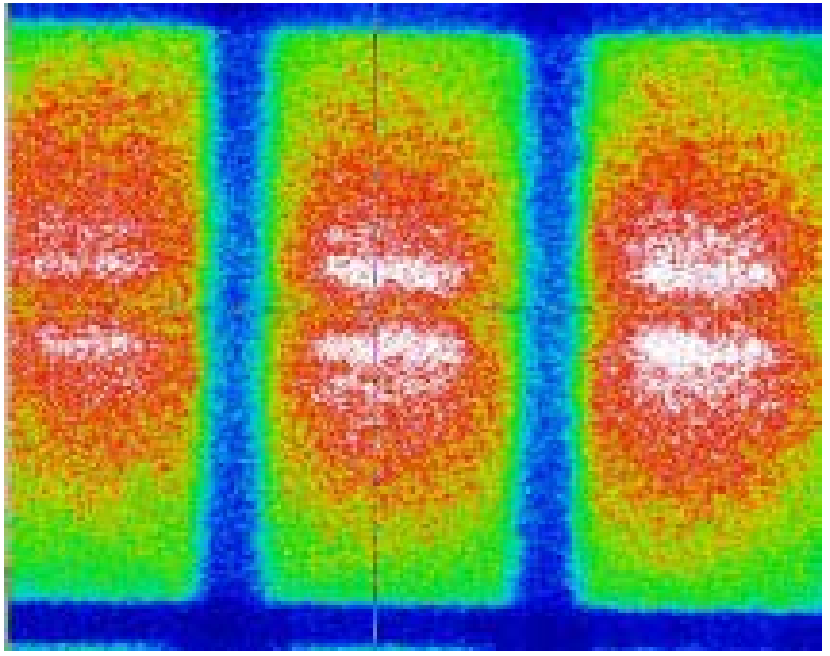
- **Wall charge**



Principles of PDP

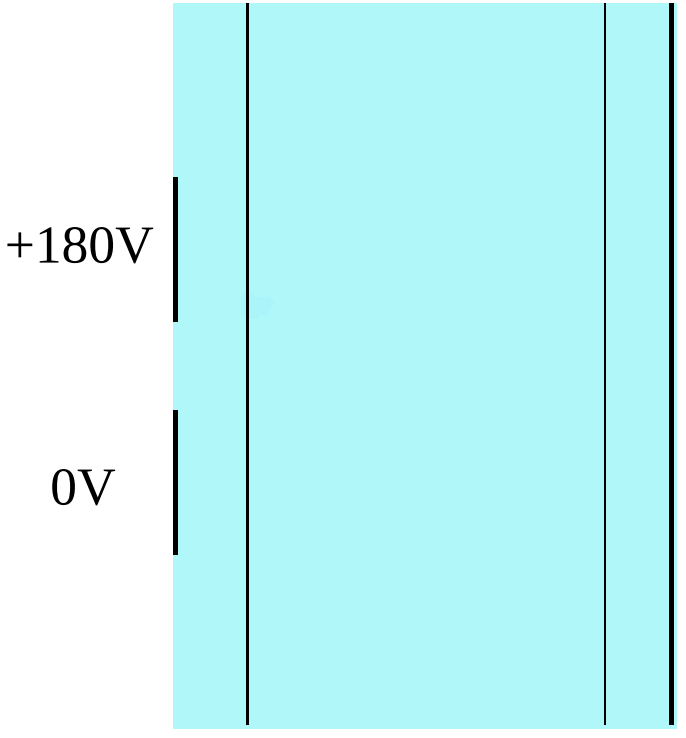
- CCD 이미지



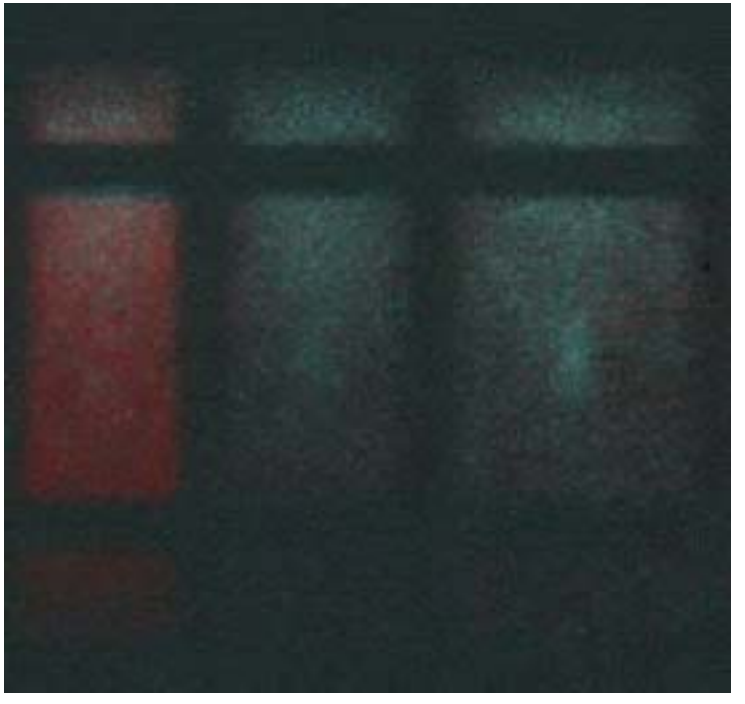


Principles of PDP

- Simulation of discharge(2D) & CCD image(동영상)



Simulation (side view)



CCD image (top view)

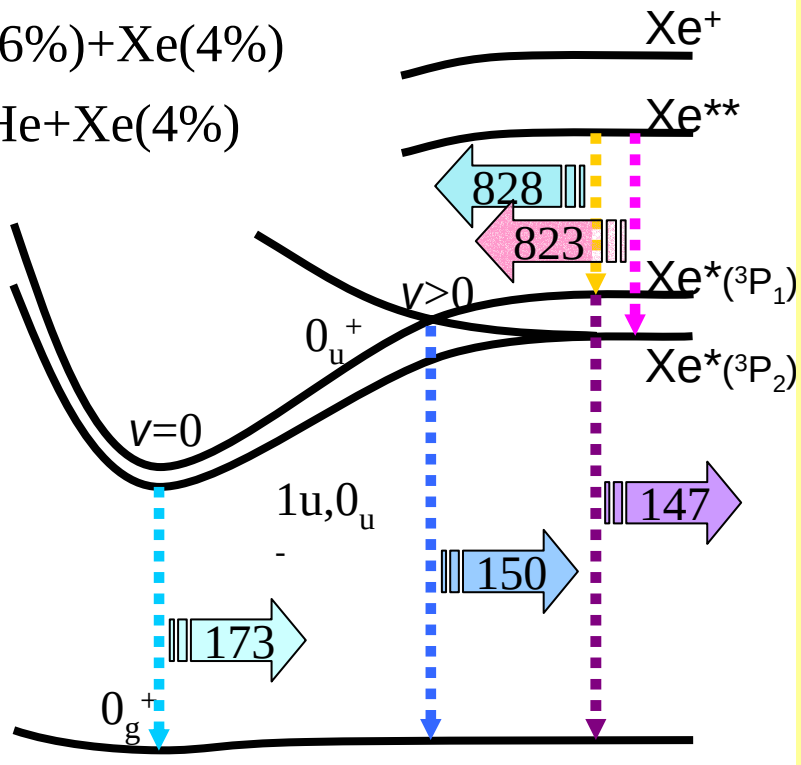
Principles of PDP

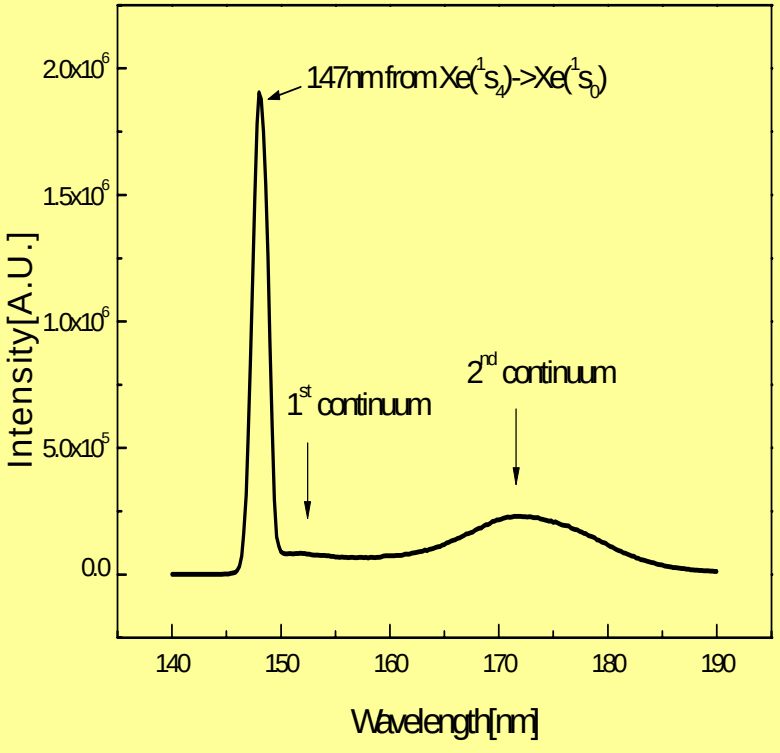
Xe의 방출 스펙트럼

He(96%)+Xe(4%)

Ne(96%)+Xe(4%)

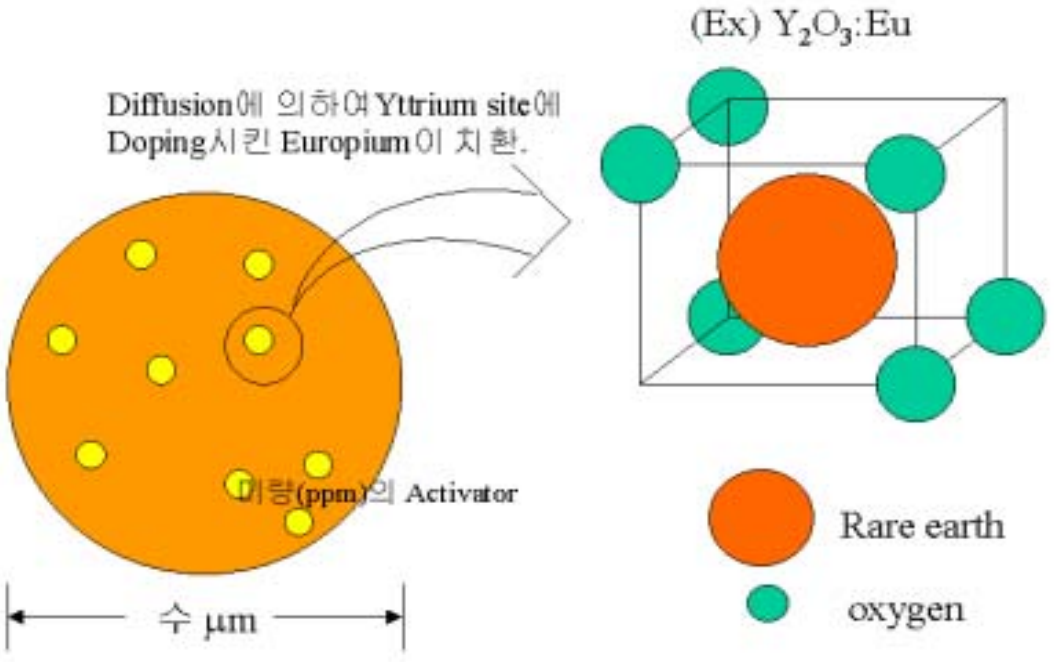
Ne+He+Xe(4%)





Principles of PDP

형광체의 정의

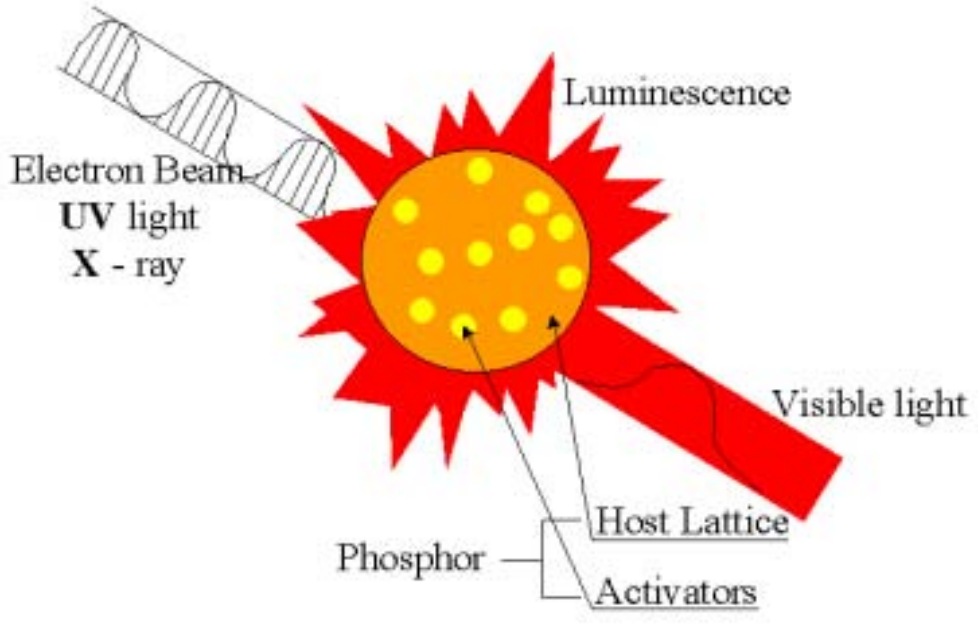


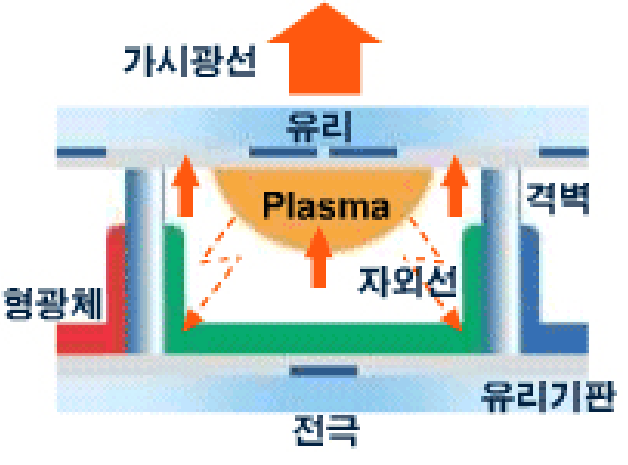
Host lattice+Activator

(Y_2O_2) (Eu)

Principles of PDP

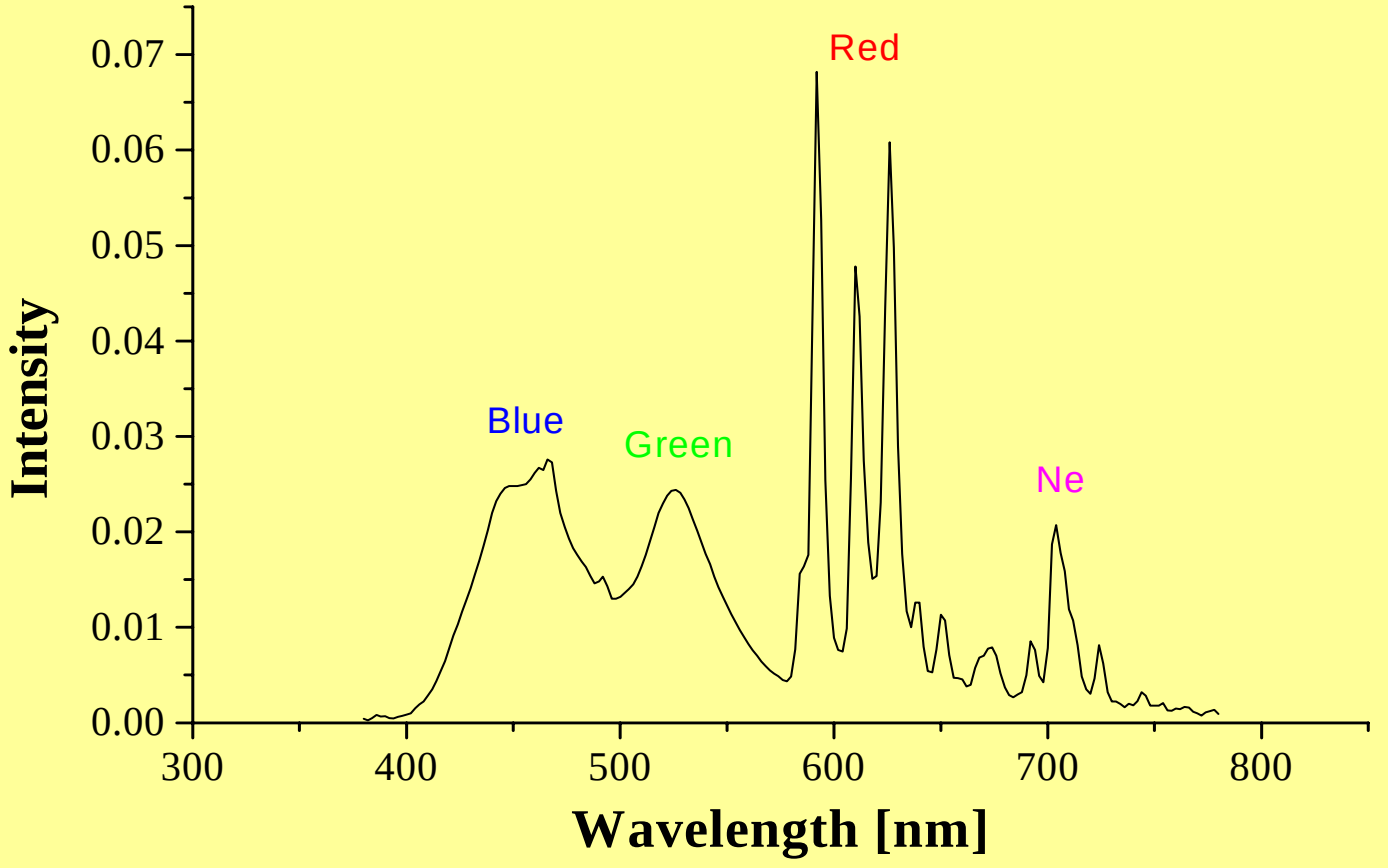
- 형광체의 발광 원리





Principles of PDP

- 가시광의 스펙트럼 Red, Green, Blue (PDP)

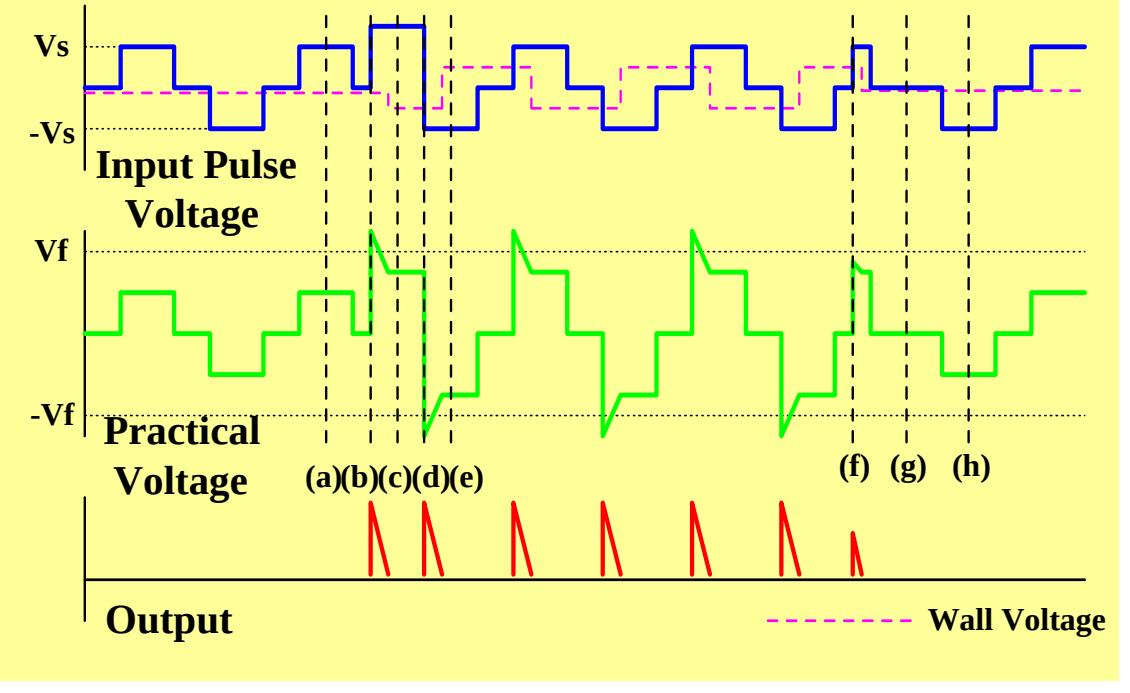


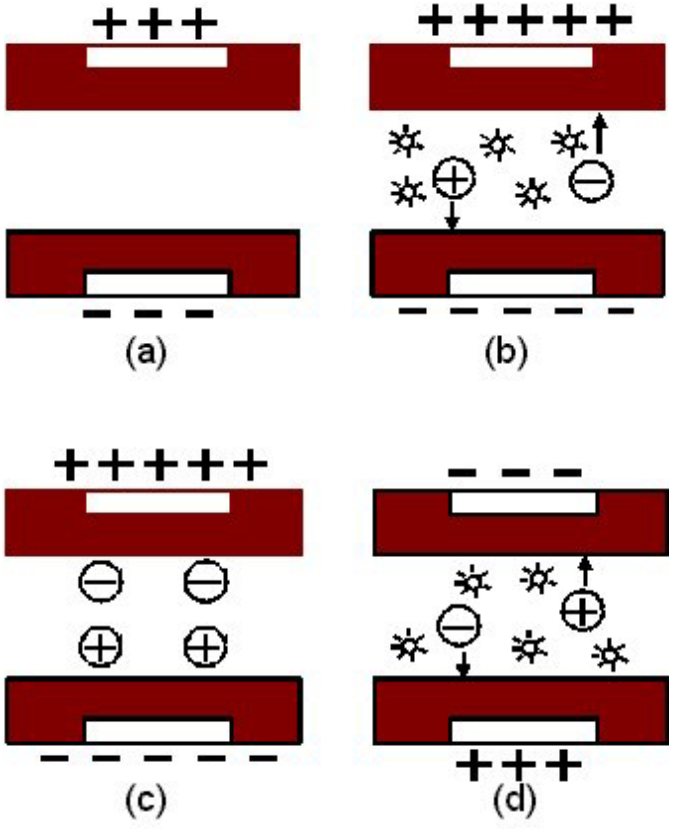
Section 3: Driving Mechanism

- PDP Driving scheme
- Necessity of Reset Pulse
- Driving scheme
  - Using Strong Discharge Reset
  - Ramp Pulse with Wall Voltage
- Driving scheme using Ramp Reset

Driving Mechanism

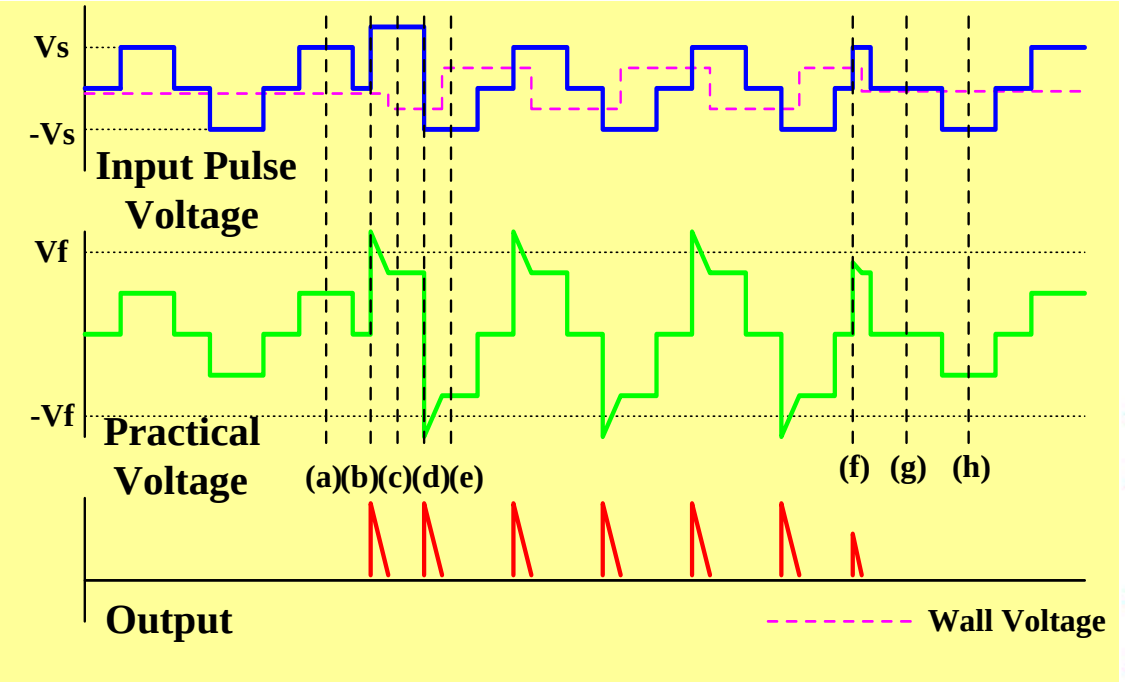
- PDP Driving scheme

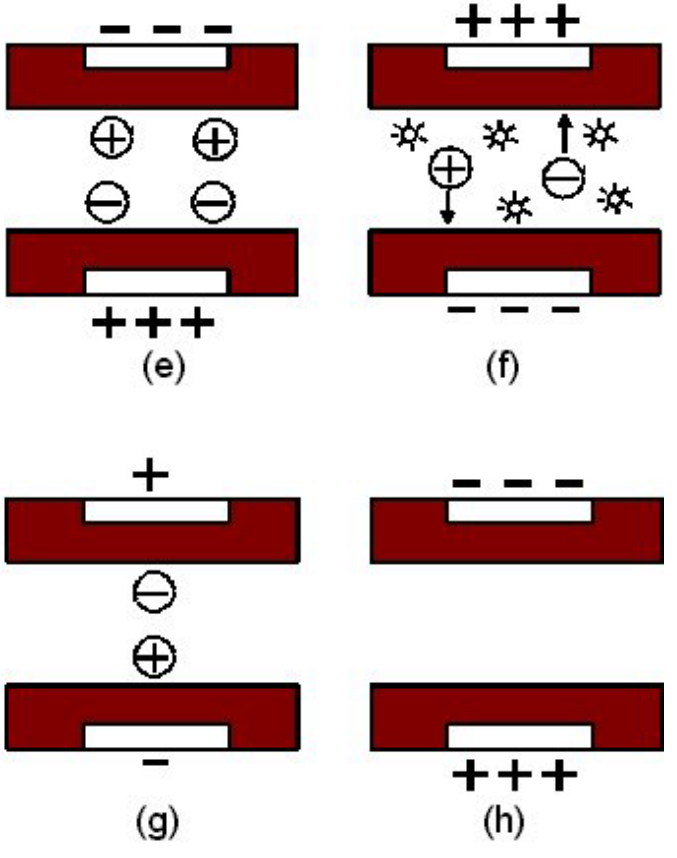




Driving Mechanism

- PDP Driving scheme





Driving Mechanism

PDP Driving step

- Reset and Erase step
  - Strong discharge reset (Pulse reset)
  - Ramp reset
- Address step

- Sustain step

Driving Mechanism

Necessity of Reset

- **Erasing of wall charges** made by previous discharge and set-up wall charge to do addressing discharge.
- **Reducing the discharge voltage difference** in PDP cell
- **Reducing of background light**
  - ➔ Improve the contrast ratio
- For **Low address voltage**

Driving Mechanism

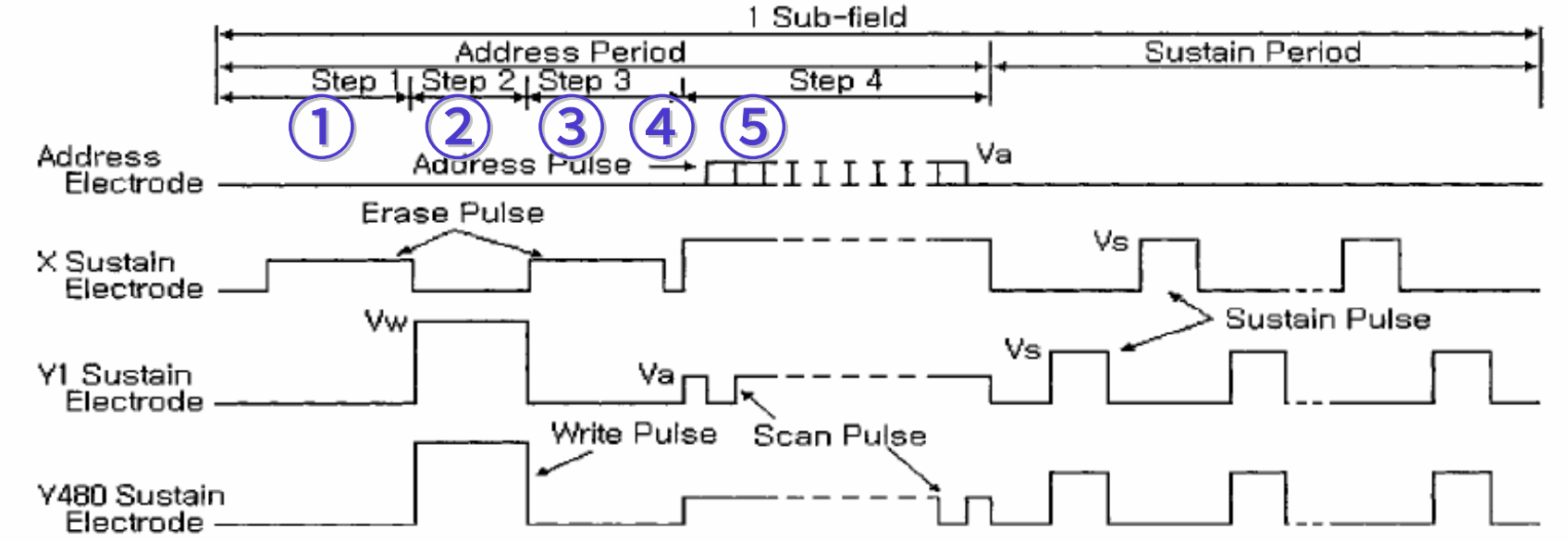
Reset pulse

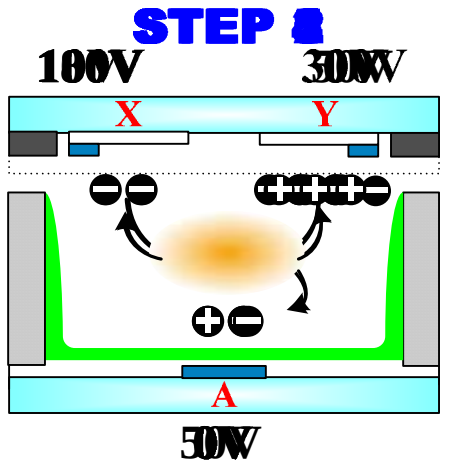
- Erasing wall charge
  - Narrow width pulse
  - Low voltage pulse
  - Ramp pulse

- Redistribution of wall charge
  - Self-erasing discharge (using strong discharge)
  - Ramp pulse (using weak discharge)

Driving Mechanism

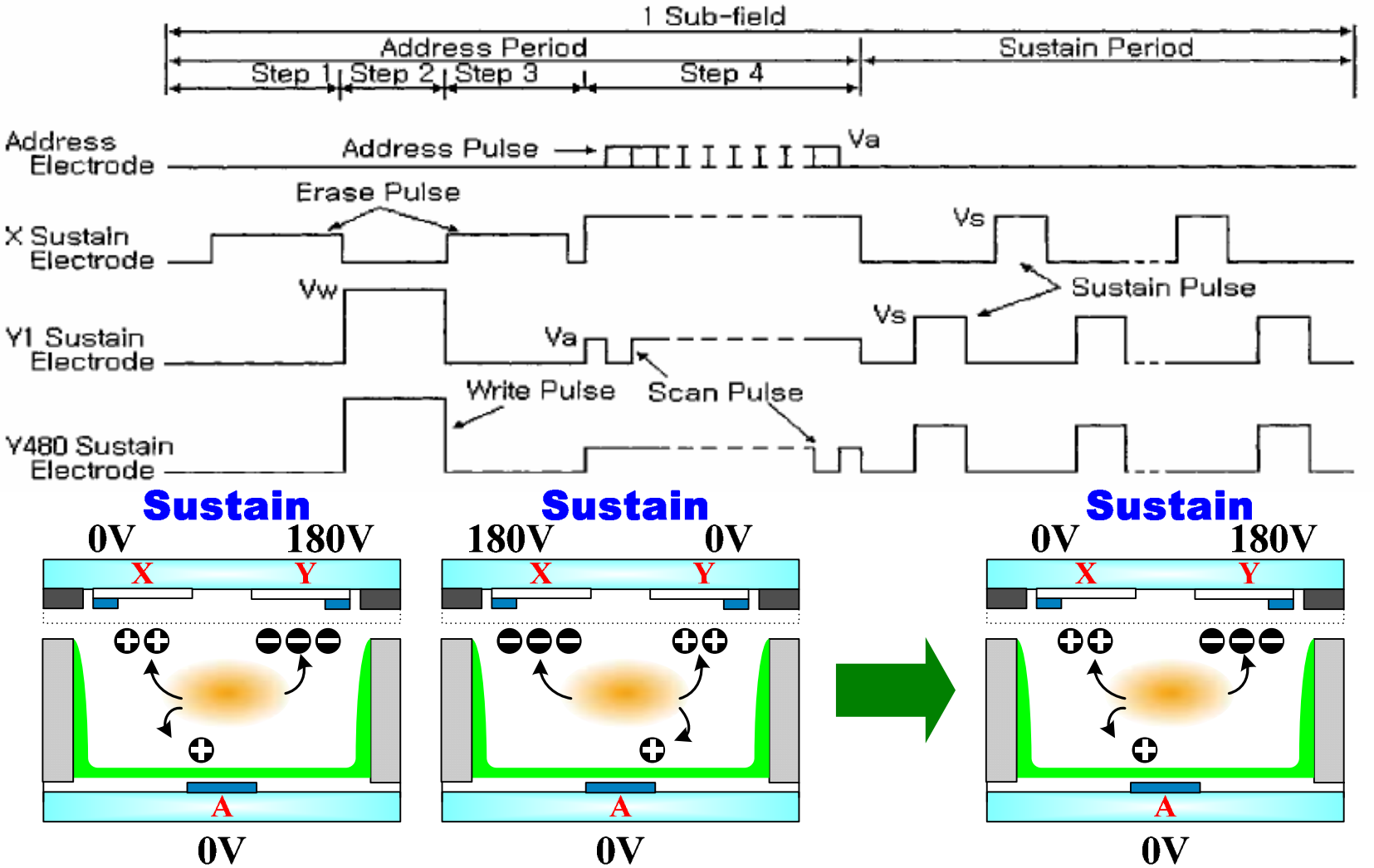
- Strong discharge reset





Driving Mechanism

- Strong Discharge Reset



Driving Mechanism

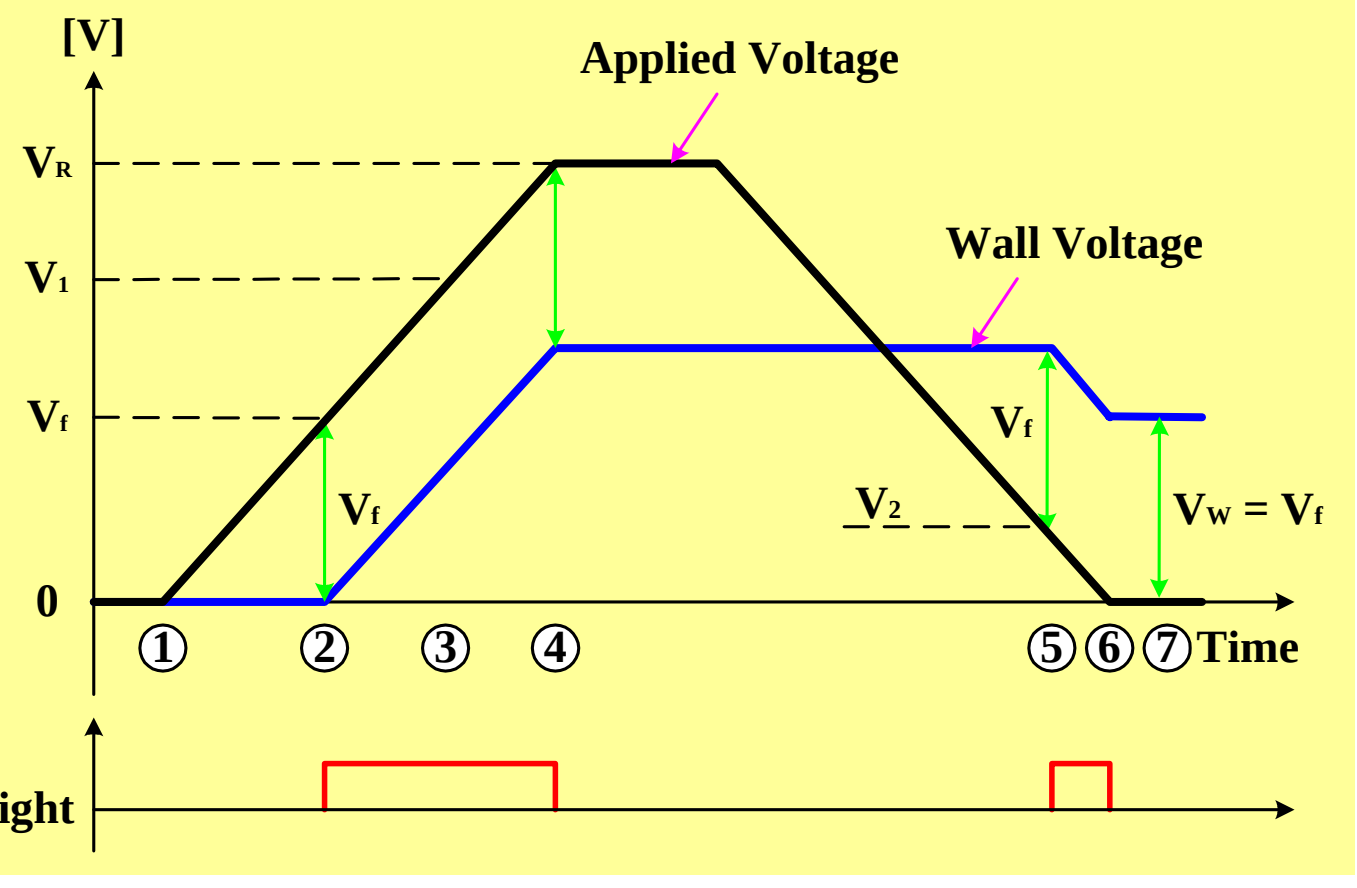
Merit & Defect in strong discharge reset

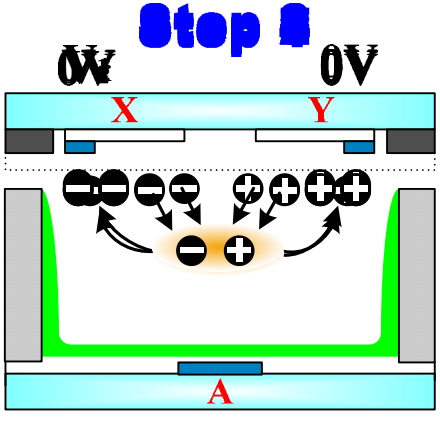
- Merits
  - Short reset time
  - Redistribution of wall charges

- Defect
  - High driving voltage
  - Self-erasing discharge
  - Low contrast ratio

Driving Mechanism

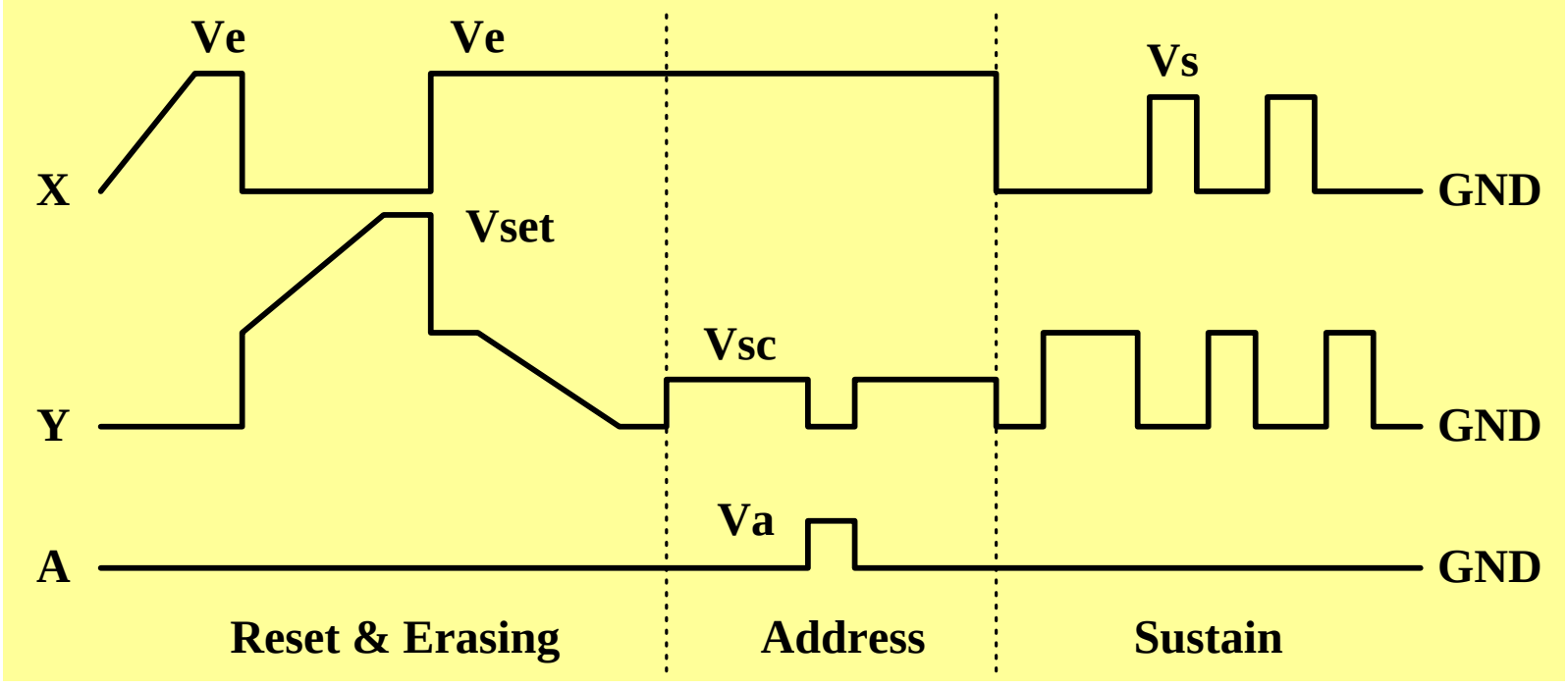
- Ramp waveform





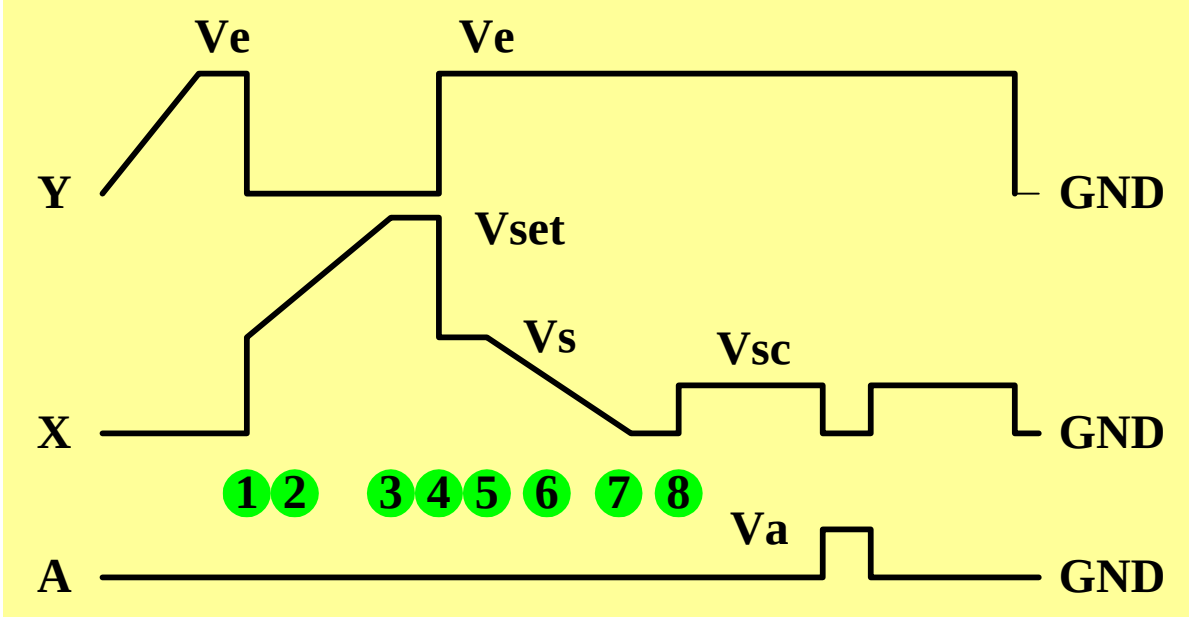
Driving Mechanism

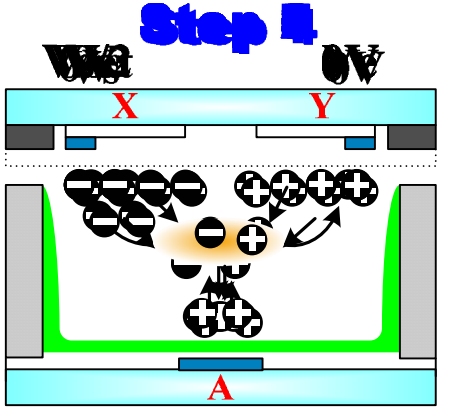
- Matsushita Driving pulse



Driving Mechanism

- Matsushita Ramp reset mechanism





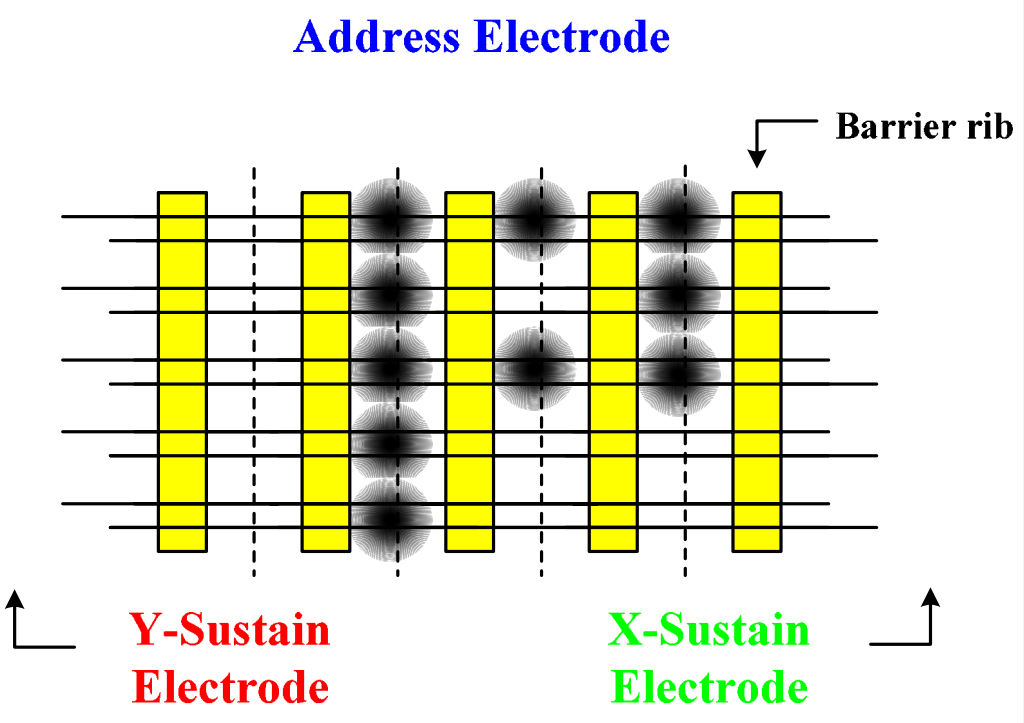
Driving Mechanism

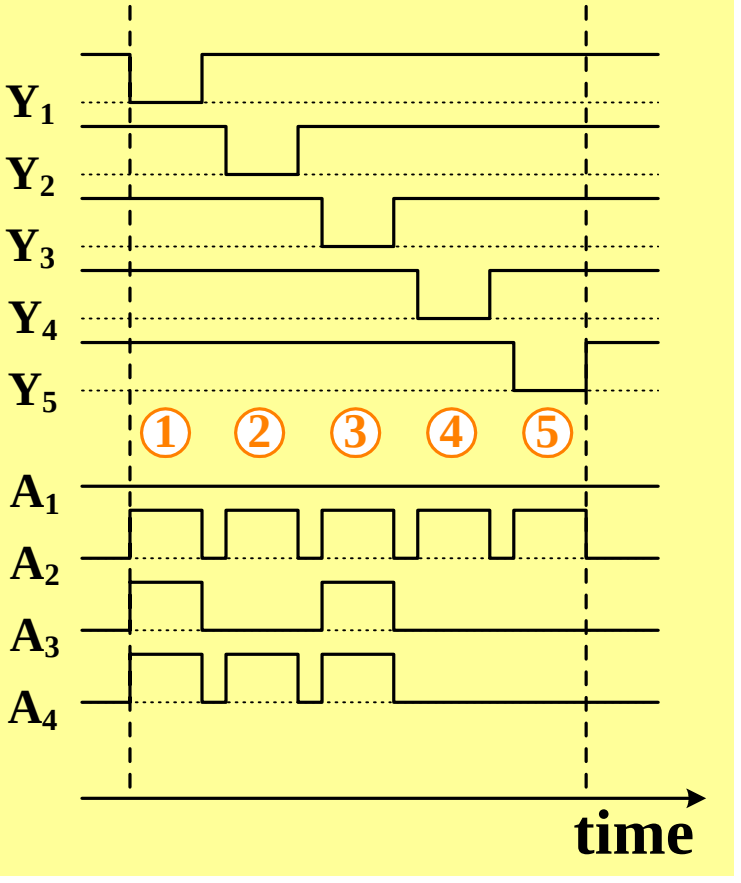
Merit and Defect of Matsushita Ramp reset

- Merits
  - High contrast ratio (Weak discharge)
  - Strong Redistribution of wall charges
  - Low address driving voltage
  - Stable
- Defect
  - Long reset time
  - High reset voltage

Driving Mechanism

- Modeling of Address step





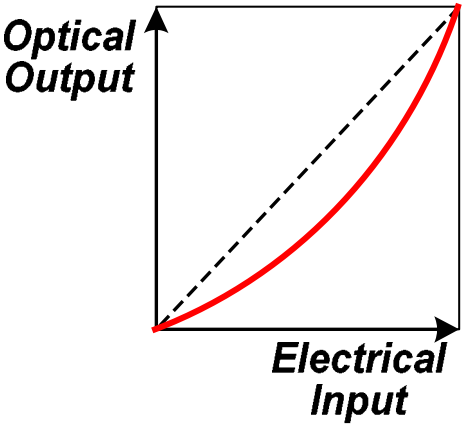
Section 4: Expression of image in PDP

- Pulse Number Modulation Driving
- Luminance Control in PDP
- Wall Charge
- Line-by-Line Scanning, Matrix Driving
- Subfield Method
- Block Diagram of Signal Circuit in PDP

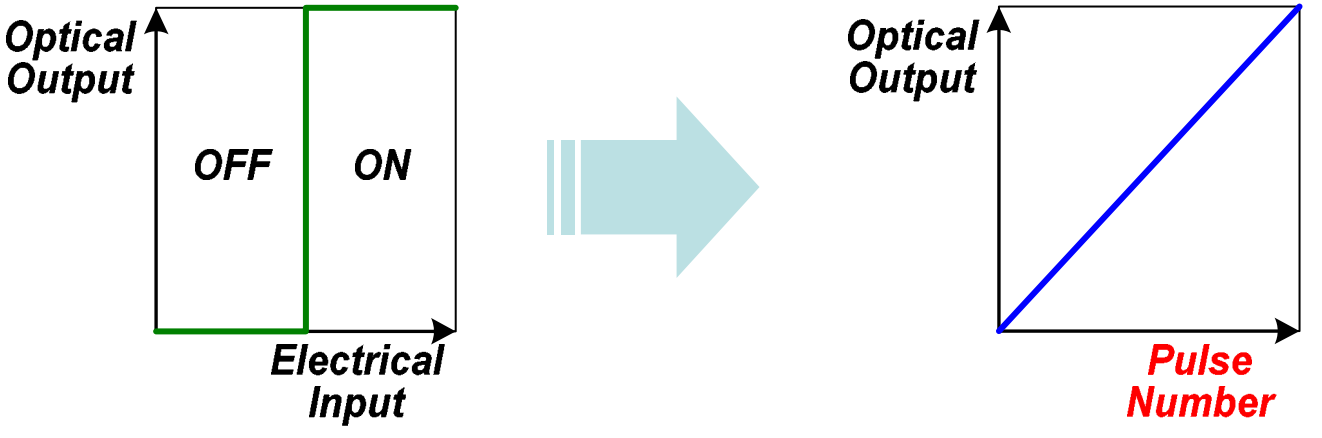
Expression of image in PDP

Pulse Number Modulation Driving

- Cathode Ray Tube :



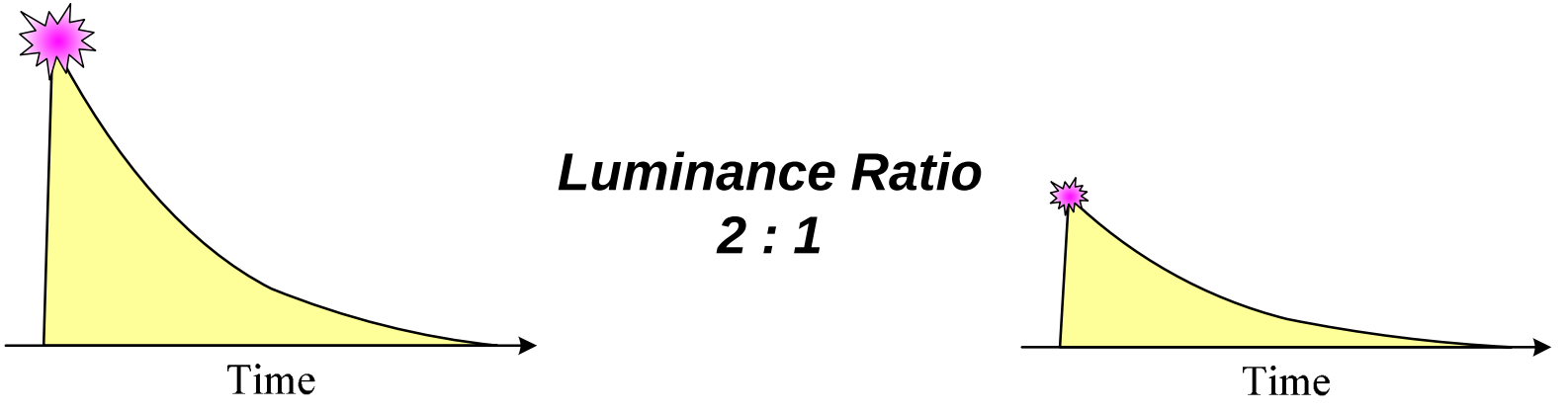
- Plasma Display Panel :



Expression of image in PDP

Luminance Control in CRT and PDP

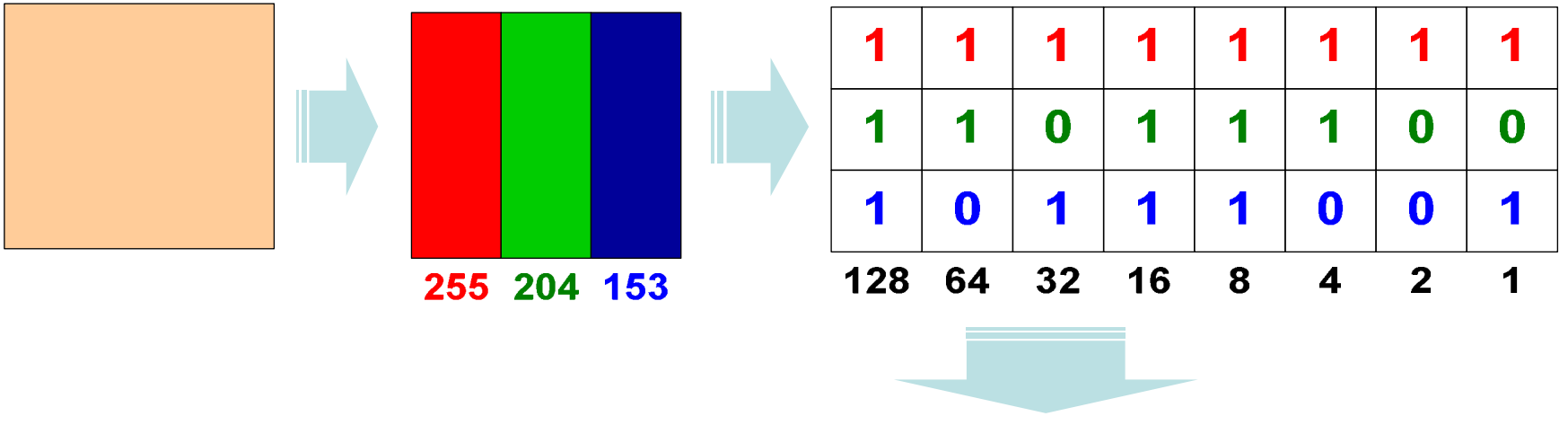
- CRT : Control the Luminance using Electron Beam Intensity



- PDP : Control the Luminance using Number of Light Pulses

Expression of image in PDP

- 8 Bit Binary Code ➔ 8 Subfield



Expression of image in PDP

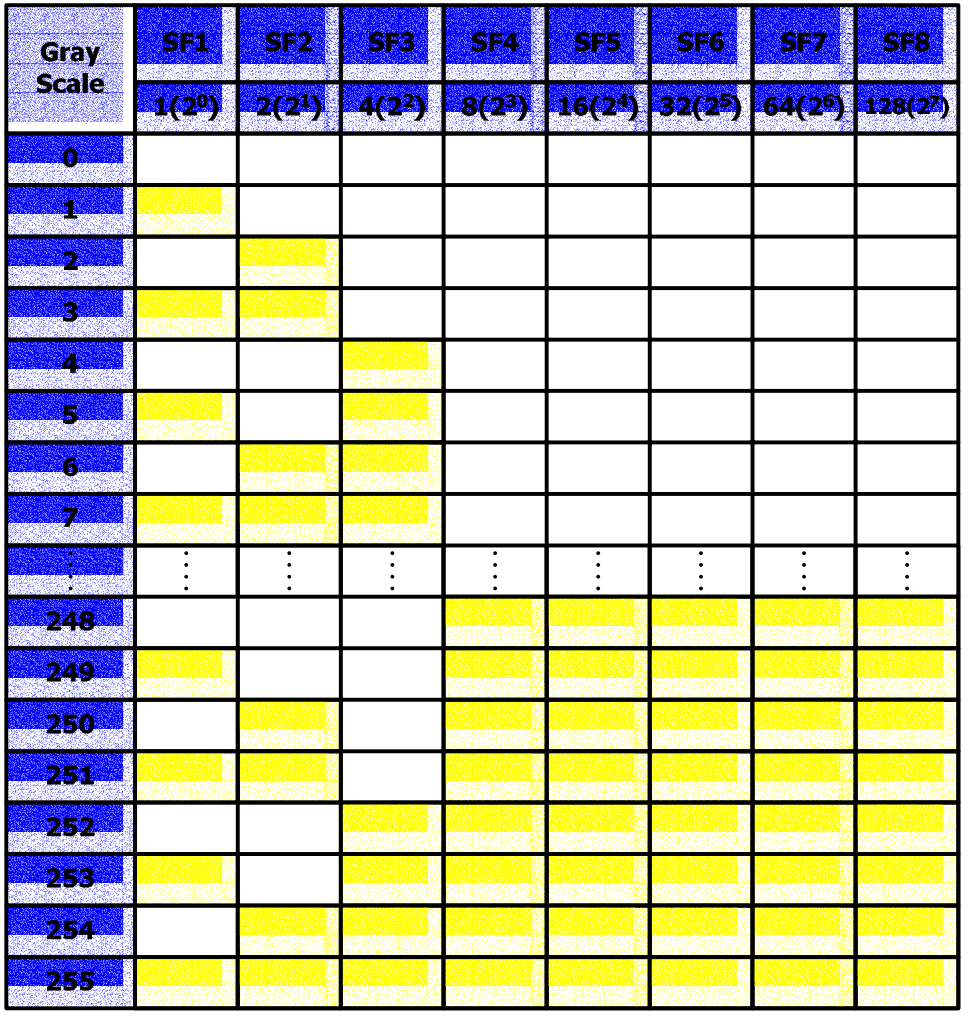
- 8 Bit Binary Code

➔8 Subfields

➔256단계의 밝기조절 가능

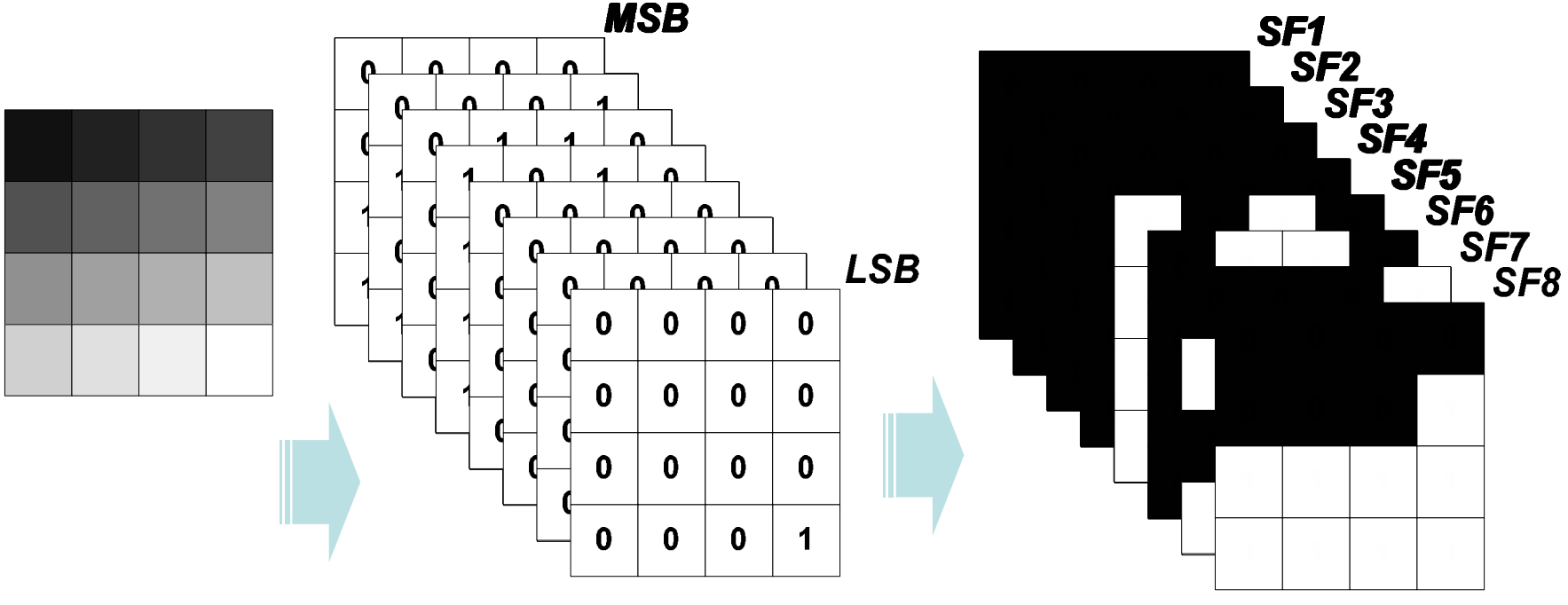
➔16,777,216가지의 색을 만들 수 있다.

R(256)
G(256)
B(256)
16,777,216



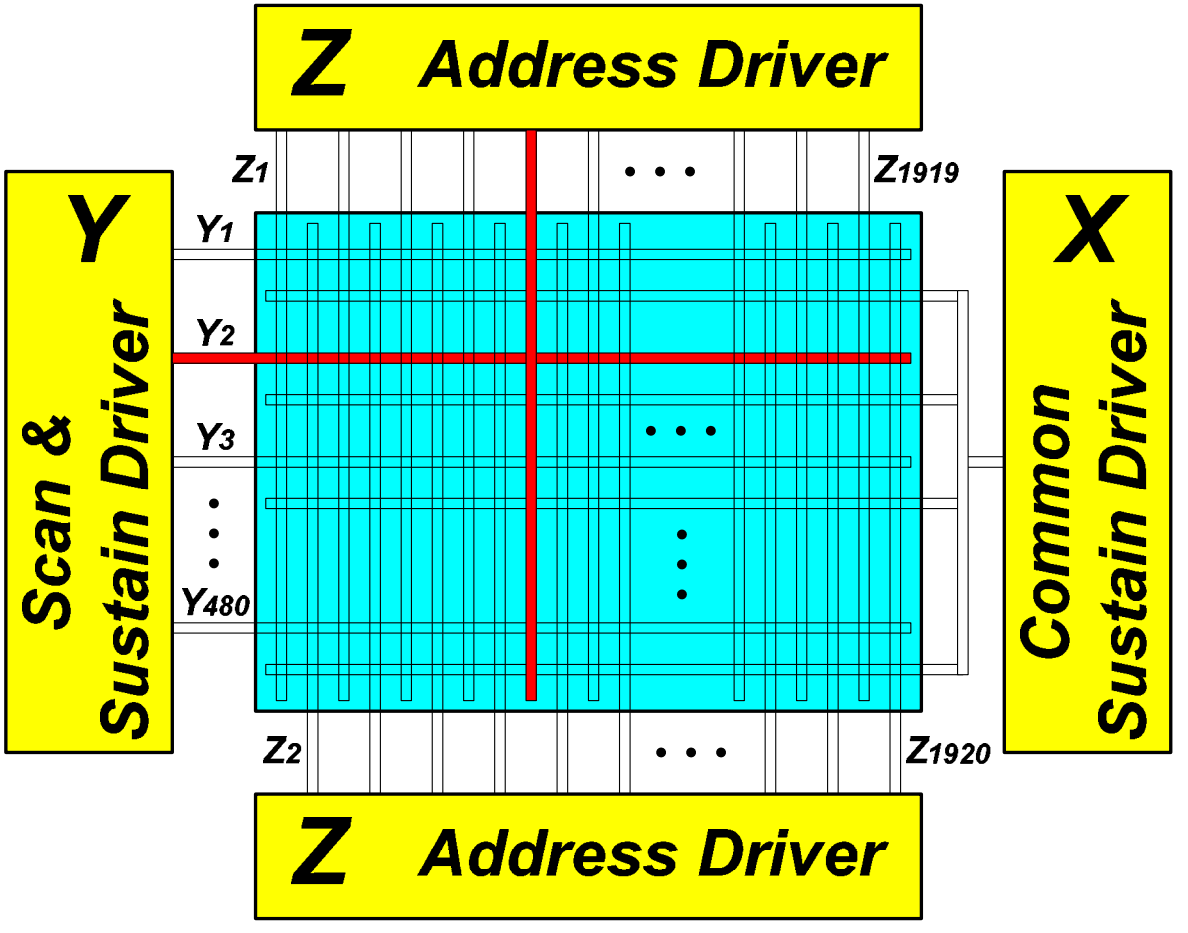
Expression of image in PDP

- 8 Bit Binary Code ➔ 8 Subfield



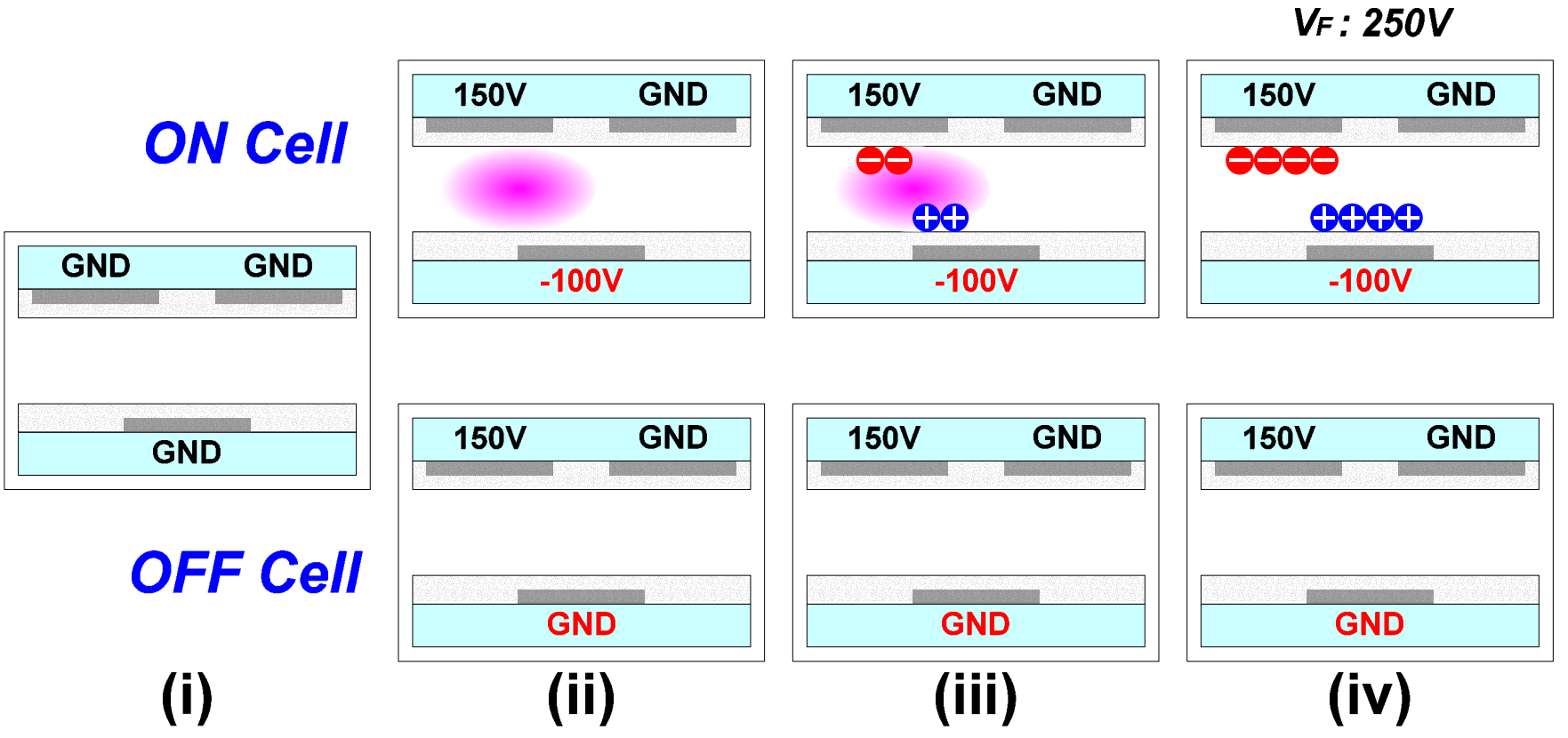
Expression of image in PDP

- Addressing (셀 선택)



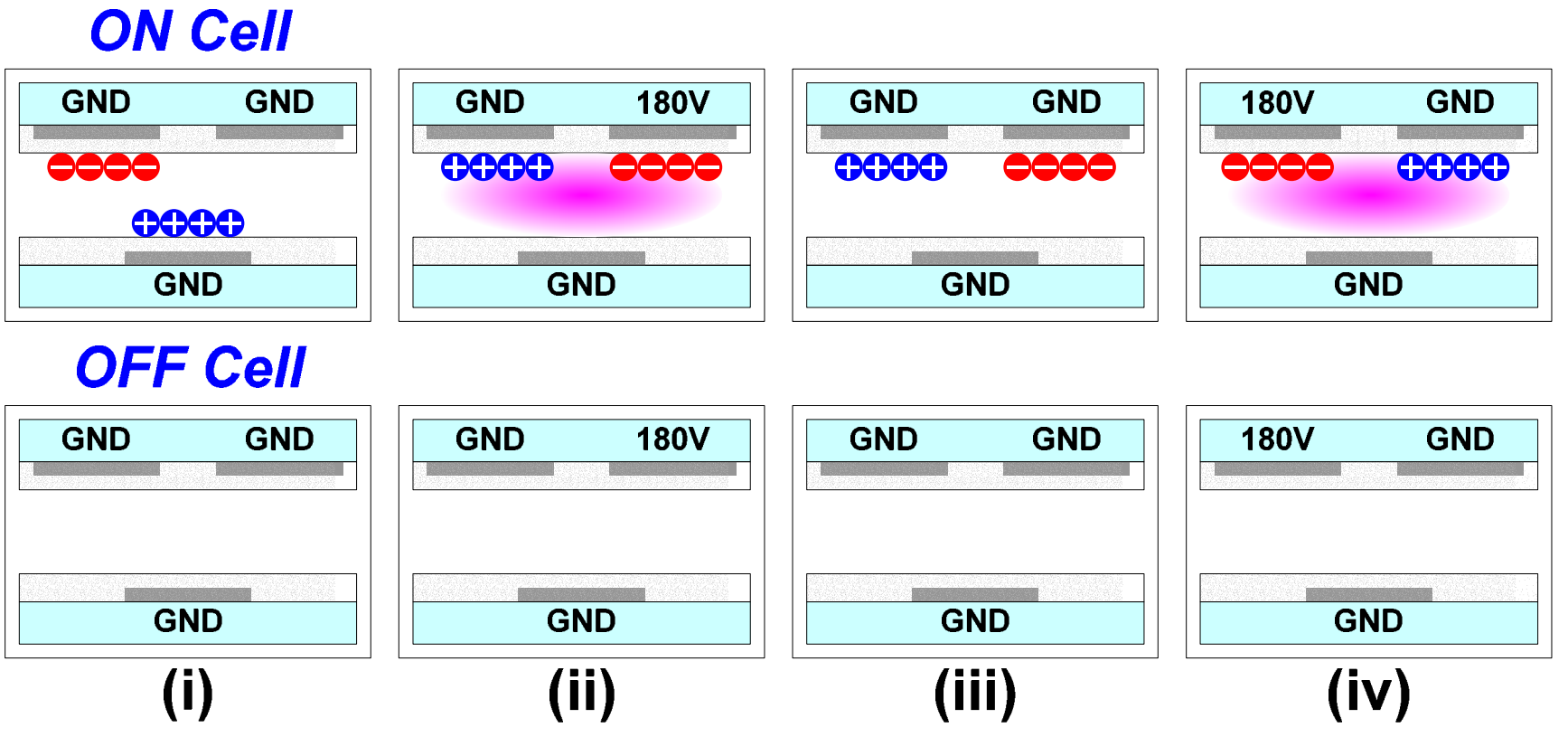
Expression of image in PDP

- ON/OFF State Selection



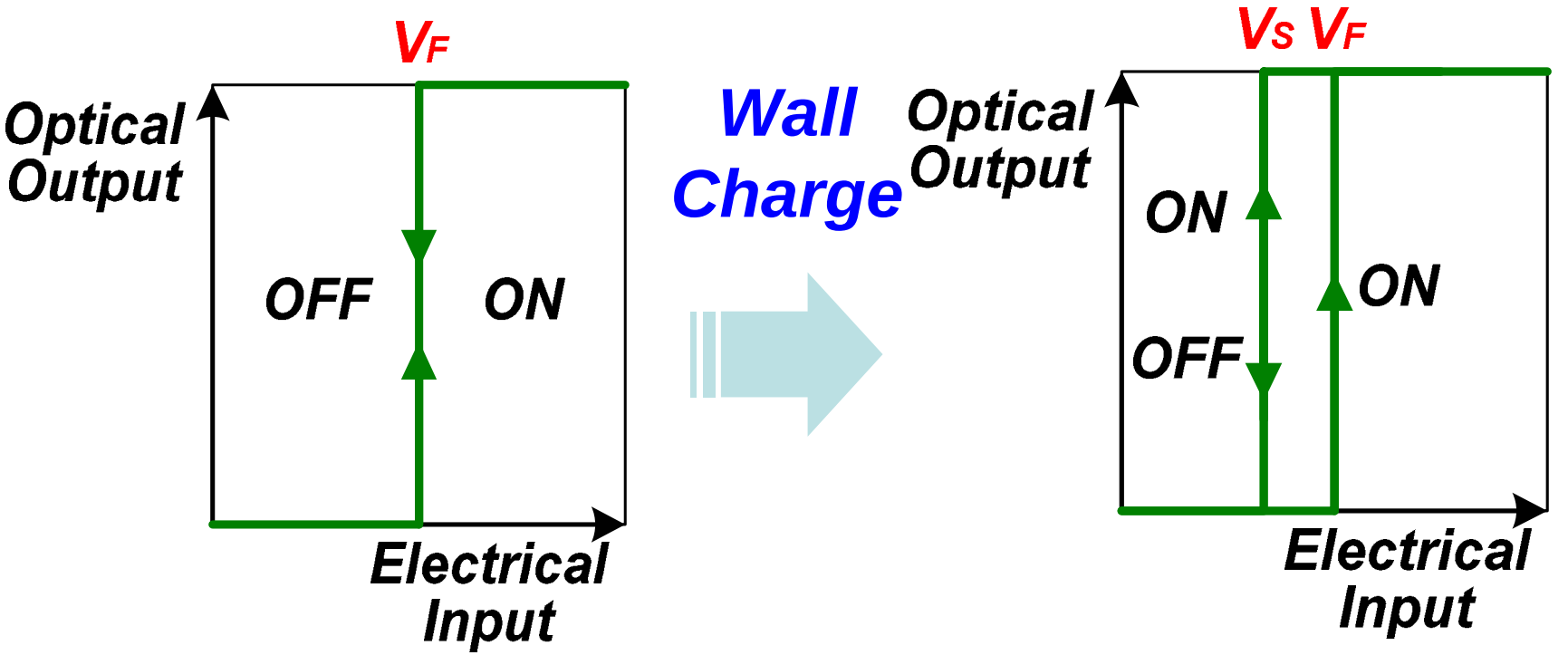
Expression of image in PDP

Sustain Discharge



Expression of image in PDP

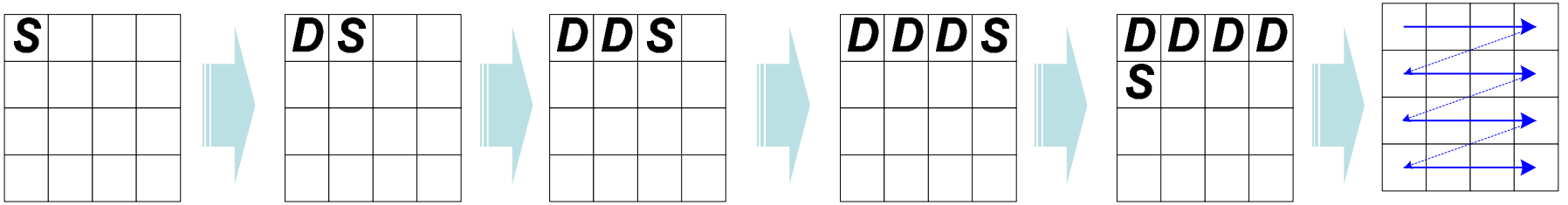
- Effect of Wall Charge



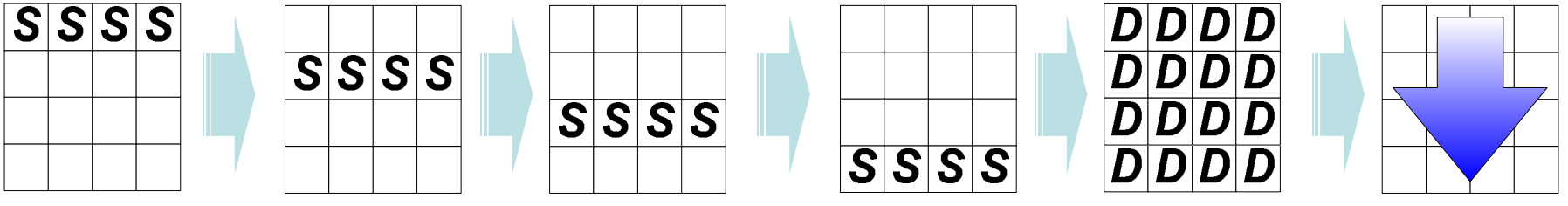
Expression of image in PDP

Line-by-Line Scanning

- Cathode Ray Tube : Cell-by-Cell Scanning

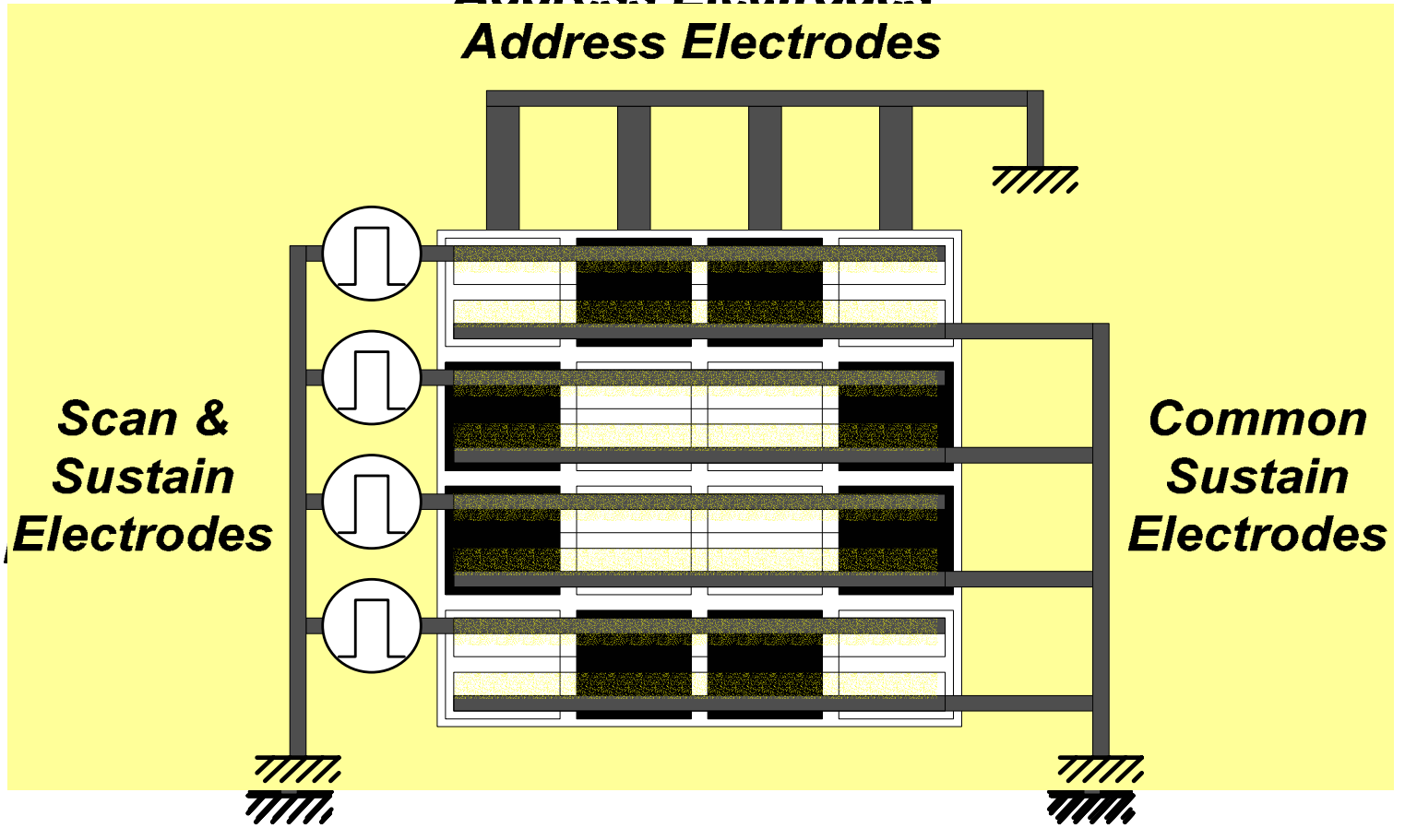


- PDP : Line-by-Line Scanning



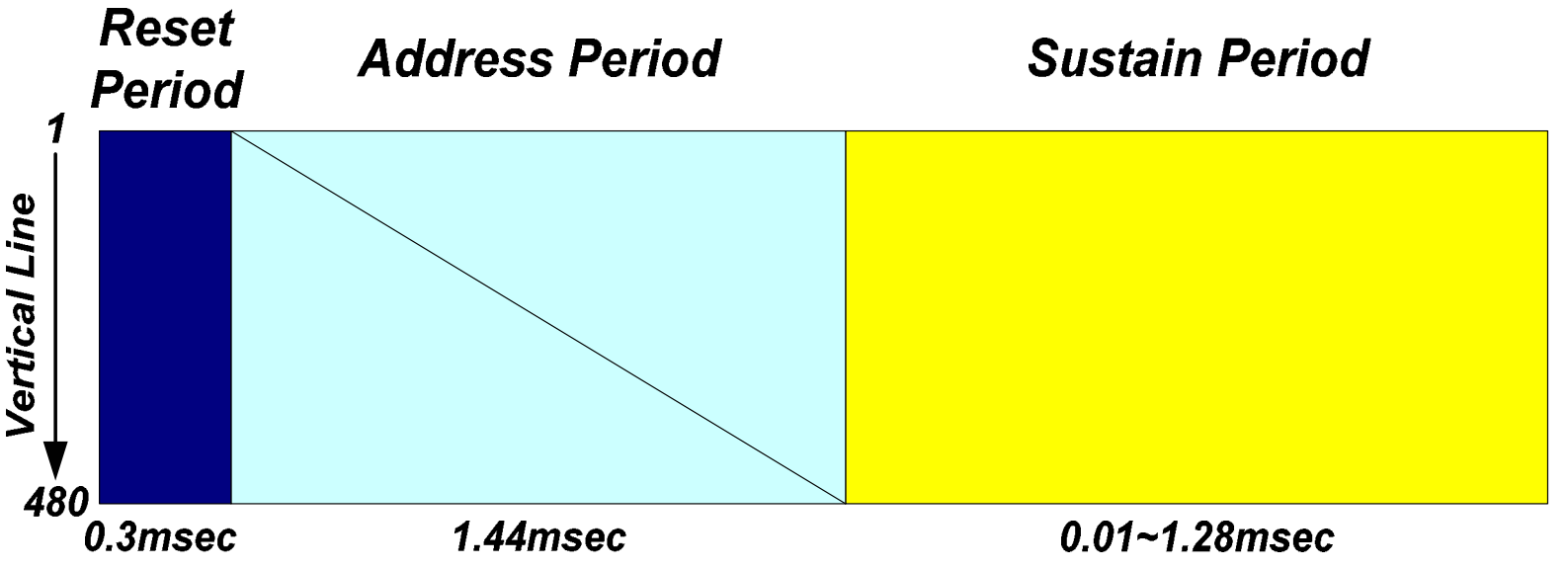
Expression of image in PDP

- Matrix Driving



Expression of image in PDP

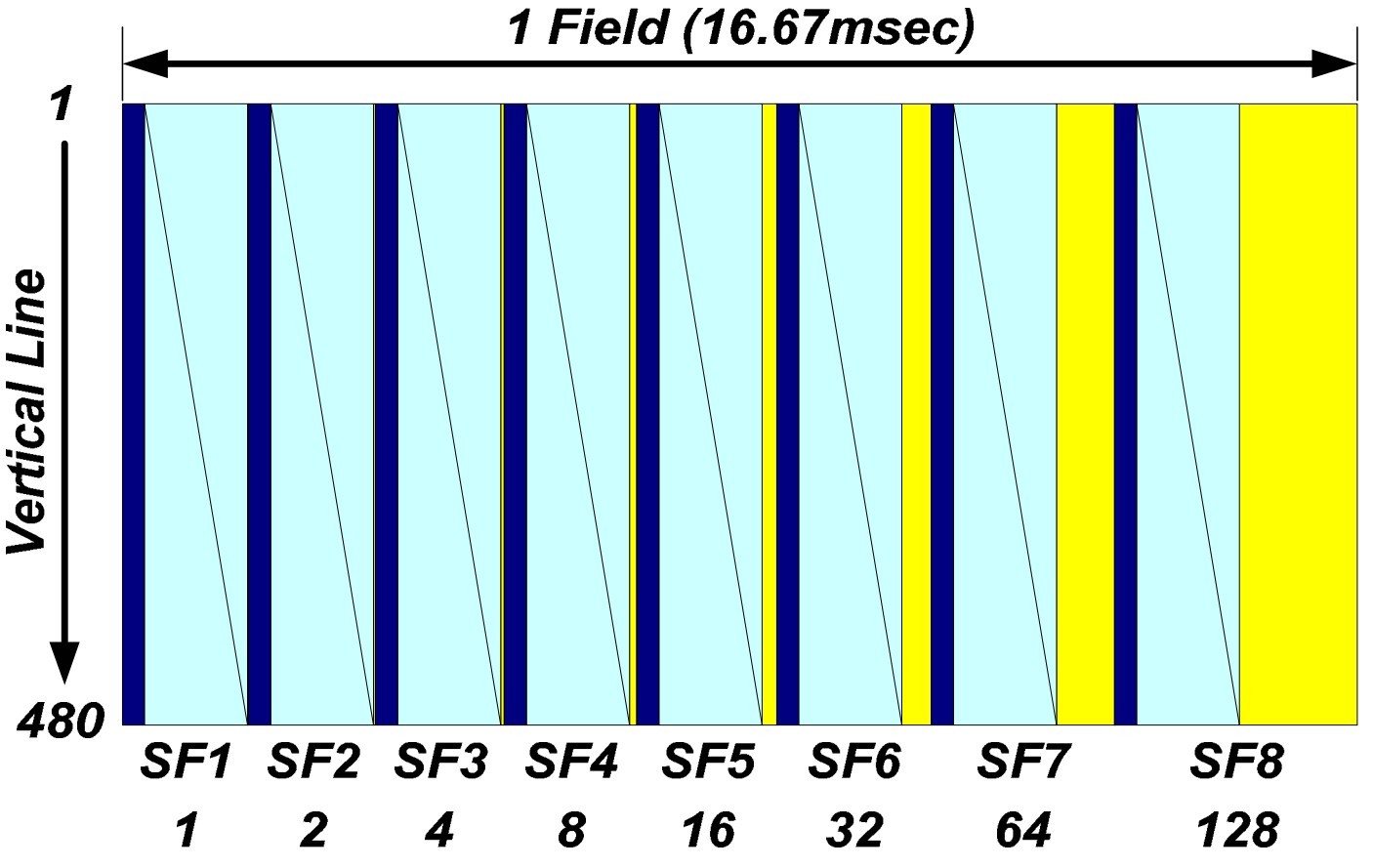
- Composition of 1 Subfield



Spec : VGA (640*480)
8 Subfield
0.03msec Address Pulse
100KHz Sustain Freq.

Expression of image in PDP

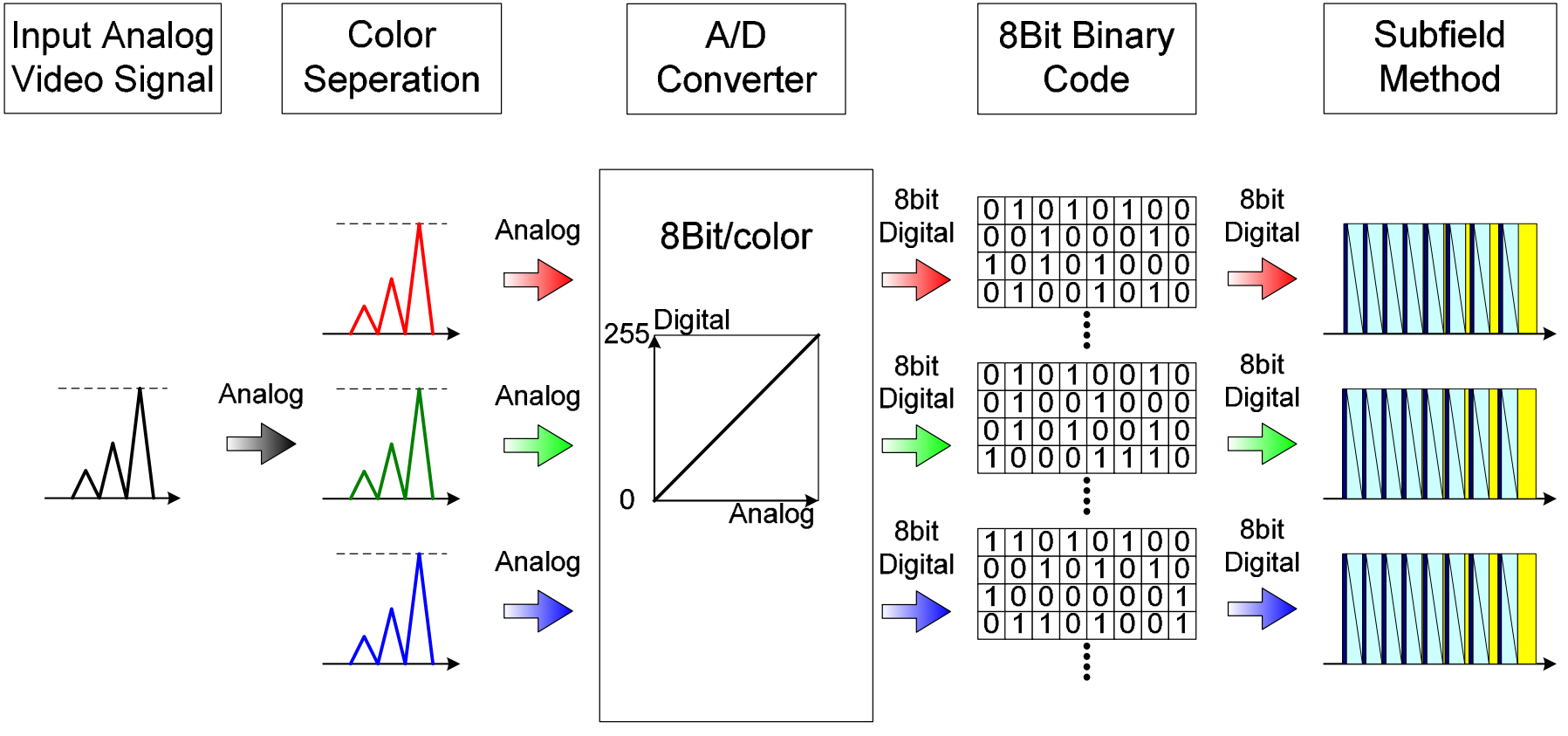
- 8 Subfield in 1 TV-Field (ADS)



Expression of image in PDP

Video Signal Processing

- Analog Video Signal ⇨ Digital Pulse Signal



Expression of image in PDP

- Subfield Method – Example (Addressing)

Original Image

SF1

SF2

SF3

SF4

SF5

SF6

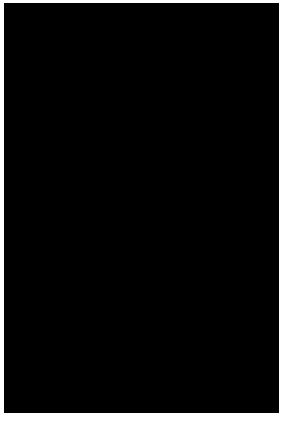
SF7

SF8

Expression of image in PDP

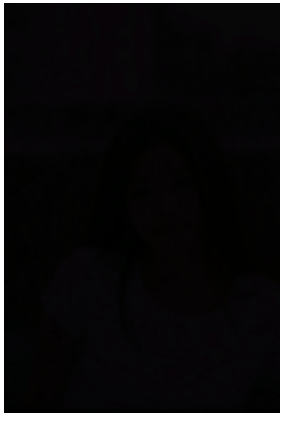
- Subfield Method – Example (Displayed)

Original Image



SF1

SF2



SF3

SF4

SF5

SF6

SF7

SF8

Future Work

- High luminance efficiency
  (목표: 5 lm/W)
- High image quality
  (color temperature, contrast ratio,
  dynamic false contour, image sticking)
- Low cost
  (materials, manufacturing processes)