Basic Principle of Plasma Display Panel

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• Principle of AC-PDP
• Driving Mechanism
• Image in PDP
Section 1: What is the ‘PDP’?

- Definition of PDP
- What is ‘plasma’?
- Plasma
- Applications of PDP
- Advantages of PDP
What is the ‘PDP’?

Definition

Input → Digital Logic Circuit → High Voltage Driver → Plasma (Gas Discharge) → Phosphor → Visible light → Human eye

Plasma: ұңғымасыз
Display: ұңғымасыз
Panel: ұңғымасыз
What is the ‘PDP’?

What is ‘Plasma’?

Low temperature  Low pressure

Low temperature  Low pressure

High temperature  High pressure

Solid  Liquid  Gas  Plasma

atom  ion  electron  ion  electron
What is the ‘PDP’?

I. 4

II. 

III. (-) (+)

IV. (collective behavior)
What is the ‘PDP’?

Applications of PDP

Home                                    Public                  Commercial
Entertainment                         Industrial                Business
What is the ‘PDP’?

Advantages of PDP

- Large screen
- Thin
- Lightweight
- Wide viewing angle
- Good Uniformity
- Distortion-Free with M.F.
Section 2: Principles of PDP

- Gas Discharge
- Structure of AC-PDP
- Gas in PDP
- Basic of AC discharge
- Emission of VUV
- Definition of Phosphor
- Spectrum of Visible light
Principles of PDP
Principles of PDP

γ-process (ion, excited species)  α-process (electron)

- Electron
- Ion
- Neutral species
- Excited species
Principles of PDP

AC Type PDP

- [Diagram of AC Type PDP]
Principles of PDP

Structure of AC PDP

Visible Light
Principles of PDP

Structure of AC PDP

- [Diagram showing the structure of AC PDP]

- MgO layer

- Y-axis

- X-axis

- Bus electrodes

- Transparent layer

- Transparent conductor
Principles of PDP

Structure of AC PDP (Structure of AC PDP)

- [ ]
- [ ]
- [ ]
- [ ]
## Principles of PDP

<table>
<thead>
<tr>
<th>Gas</th>
<th>Ionization Energy (eV)</th>
<th>Wavelength (nm)</th>
<th>Excitation Energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>He</td>
<td>21.2</td>
<td>58.4</td>
<td>24.59</td>
</tr>
<tr>
<td>Ne</td>
<td>16.54</td>
<td>74.4</td>
<td>21.57</td>
</tr>
<tr>
<td>Ar</td>
<td>11.61</td>
<td>107</td>
<td>15.76</td>
</tr>
<tr>
<td>Xe</td>
<td>8.45</td>
<td>147</td>
<td>12.13</td>
</tr>
</tbody>
</table>

The diagram illustrates the energy levels and transitions between them. The initial state is labeled as $E_1$ and the final state as $E_2$, with an ultraviolet emission indicated.
Principles of PDP

Wall charge
Polarization of dielectric (図 1 の図）
Principles of PDP

• Wall charge
Principles of PDP

CCD
Principles of PDP

Simulation of discharge (2D) & CCD image (side view)
He(96%)+Xe(4%)
Ne(96%)+Xe(4%)
Ne+He+Xe(4%)

Principles of PDP
Principles of PDP

Host lattice + Activator
(Y₂O₂)   (Eu)
Principles of PDP
Principles of PDP

Red, Green, Blue (PDP)
Section 3: Driving Mechanism

- PDP Driving scheme
- Necessity of Reset Pulse
- Driving scheme
  - Using Strong Discharge Reset
  - Ramp Pulse with Wall Voltage
- Driving scheme using Ramp Reset
Driving Mechanism

- PDP Driving scheme

- Vs
- Vf
- Vf
- Output

- Input Pulse Voltage
- Practical Voltage
- Wall Voltage

(a)(b)(c)(d)(e) (f) (g) (h)

Driving Mechanism

- PDP Driving scheme

- Vs
- Vf
- Vf
- Output

- Input Pulse Voltage
- Practical Voltage
- Wall Voltage

(a)(b)(c)(d)(e) (f) (g) (h)
Driving Mechanism

PDP Driving scheme

\[ \begin{align*}
V_s & \quad \text{Input Pulse Voltage} \\
-V_s & \\
V_f & \quad \text{Practical Voltage} \\
-V_f & \quad \text{(a)(b)(c)(d)(e)} \\
\text{Output} & \quad \text{(f)(g)(h)}
\end{align*} \]
Driving Mechanism

- Reset and Erase step
  - Strong discharge reset (Pulse reset)
  - Ramp reset
- Address step
- Sustain step
Driving Mechanism

- **Necessity of Reset**

- **Erasing of wall charges** made by previous discharge and set-up wall charge to do addressing discharge.

- **Reducing the discharge voltage difference** in PDP cell

- **Reducing of background light**
  - Improve the contrast ratio

- **For Low address voltage**
Driving Mechanism

- **Reset pulse**

- Erasing wall charge
  - Narrow width pulse
  - Low voltage pulse
  - Ramp pulse

- Redistribution of wall charge
  - Self-erasing discharge (using strong discharge)
  - Ramp pulse (using weak discharge)
Driving Mechanism

- Strong discharge reset

![Diagram of Driving Mechanism]

1. Sub-field
2. Address Period
3. Step 1
4. Step 2
5. Step 3
6. Step 4
7. Sustain Period

- Address Electrode
- X Sustain Electrode
- Y1 Sustain Electrode
- Y480 Sustain Electrode

STEP 8

- 100V
- 300V

- X
- Y
- A
Driving Mechanism

- **Strong Discharge Reset**

1 Sub-field

Address Period

Step 1 | Step 2 | Step 3 | Step 4 | Sustain Period

Address Pulse

Erase Pulse

X Sustain Electrode

Y1 Sustain Electrode

Y480 Sustain Electrode

---

<table>
<thead>
<tr>
<th>Sustain</th>
<th>0V</th>
<th>180V</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[Diagrams showing the discharge process and voltage levels]
Driving Mechanism

- Merit & Defect in strong discharge reset

  - Merits
    - Short reset time
    - Redistribution of wall charges

  - Defect
    - High driving voltage
    - Self-erasing discharge
    - Low contrast ratio
Driving Mechanism

- Ramp waveform

![Graph showing a ramp waveform with labels for VR, V1, Vf, VW = Vf, step 5, and light output.

Applied Voltage

Wall Voltage

Vf

VW = Vf

Time

0 1 2 3 4 5 6 7

Light
Driving Mechanism

Matsushita Driving pulse

Diagram:

- Ve
- Vset
- Vsc
- Va
- Vs
- GND

X
Y
A

- Reset & Erasing
- Address
- Sustain
Driving Mechanism

- Matsushita Ramp reset mechanism

![Diagram of driving mechanism](image)
Driving Mechanism

Merit and Defect of Matsushita Ramp reset

• Merits
  – High contrast ratio (Weak discharge)
  – Strong Redistribution of wall charges
  – Low address driving voltage
  – Stable

• Defect
  – Long reset time
  – High reset voltage
Driving Mechanism

Modeling of Address step

Address Electrode

Y-Sustain Electrode

X-Sustain Electrode

Barrier rib

Y1
Y2
Y3
Y4
Y5
A1
A2
A3
A4

① ② ③ ④ ⑤
time
Section 4: Expression of image in PDP

- Pulse Number Modulation Driving
- Luminance Control in PDP
- Wall Charge
- Line-by-Line Scanning, Matrix Driving
- Subfield Method
- Block Diagram of Signal Circuit in PDP
Expression of image in PDP

- **Pulse Number Modulation Driving**

  - Cathode Ray Tube:

  - Plasma Display Panel:
Expression of image in PDP

**Luminance Control in CRT and PDP**

- **CRT**: Control the Luminance using **Electron Beam Intensity**

  ![Luminance Ratio 2:1 (CRT)](image1)

- **PDP**: Control the Luminance using **Number of Light Pulses**

  ![Luminance Ratio 2:1 (PDP)](image2)
Expression of image in PDP

8 Bit Binary Code → 8 Subfield

MSB

<table>
<thead>
<tr>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
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<tbody>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

LSB

128  64  32  16  8   4   2   1

SF1  SF2  SF3  SF4  SF5  SF6  SF7  SF8

| 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |

Red, Green, Blue

Image Expression
Expression of image in PDP

- 8 Bit Binary Code
- 8 Subfields
- 256 Subfields
- 16,777,216 Subfields

R(256) → 16,777,216
G(256) → 16,777,216
B(256) → 16,777,216
Expression of image in PDP

- 8 Bit Binary Code ➔ 8 Subfield
Expression of image in PDP

Addressing (¼¿ ¼±ÅÃ)
Expression of image in PDP

ON/OFF State Selection

ON Cell

150V GND
-100V

150V GND

OFF Cell

(i) GND

(ii) GND

(iii) GND

(iv) GND

VF: 250V
Expression of image in PDP

**Sustain Discharge**

**ON Cell**

(i) GND  GND
(ii) GND  180V
(iii) GND  GND
(iv) 180V  GND

**OFF Cell**

(i) GND  GND
(ii) GND  180V
(iii) GND  GND
(iv) 180V  GND
Expression of image in PDP

Effect of Wall Charge

Wall Charge

Optical Output

OFF

ON

Electrical Input

V_F

VS V_F

Optical Output

OFF

ON

Electrical Input
Expression of image in PDP

- Line-by-Line Scanning
  - Cathode Ray Tube: Cell-by-Cell Scanning
  
  \[
  \begin{array}{cccc}
  S & DS & DDS & DDDS \\
  \hline
  & & & \\
  & & & \\
  & & & \\
  & & & \\
  \end{array}
  \]

- PDP: Line-by-Line Scanning
  
  \[
  \begin{array}{cccc}
  SSSSS & SSSSS & SSSSS & SSSSS \\
  \hline
  & & & \\
  & & & \\
  & & & \\
  & & & \\
  \end{array}
  \]
Expression of image in PDP

Matrix Driving

Address Electrodes

Scan & Sustain Electrodes

Common Sustain Electrodes
Expression of image in PDP

Composition of 1 Subfield

Reset Period  Address Period  Sustain Period

Vertical Line

0.3msec  1.44msec  0.01~1.28msec

Spec: VGA (640x480)
  8 Subfield
  0.03msec Address Pulse
  100KHz Sustain Freq.
Expression of image in PDP

8 Subfield in 1 TV-Field (ADS)

1 Field (16.67 msec)
Expression of image in PDP

Video Signal Processing

- Analog Video Signal $\Rightarrow$ Digital Pulse Signal

Input Analog Video Signal  |  Color Separation  |  A/D Converter  |  8Bit Binary Code  |  Subfield Method

![Diagram showing the process of converting analog video signal to digital pulse signal through color separation, A/D conversion, and binary code, followed by subfield method.](image-url)
Expression of image in PDP

Subfield Method – Example (Addressing)

Original Image

SF1

SF2

SF3

SF4

SF5

SF6

SF7

SF8
Expression of image in PDP

Subfield Method – Example (Displayed)
Future Work

- High luminance efficiency
  (5 lm/W)

- High image quality
  (color temperature, contrast ratio, dynamic false contour, image sticking)

- Low cost
  (materials, manufacturing processes)