CERN Accelerator School
ADCs and DACs
(Analogue to Digital and Digital to Analogue Converters)

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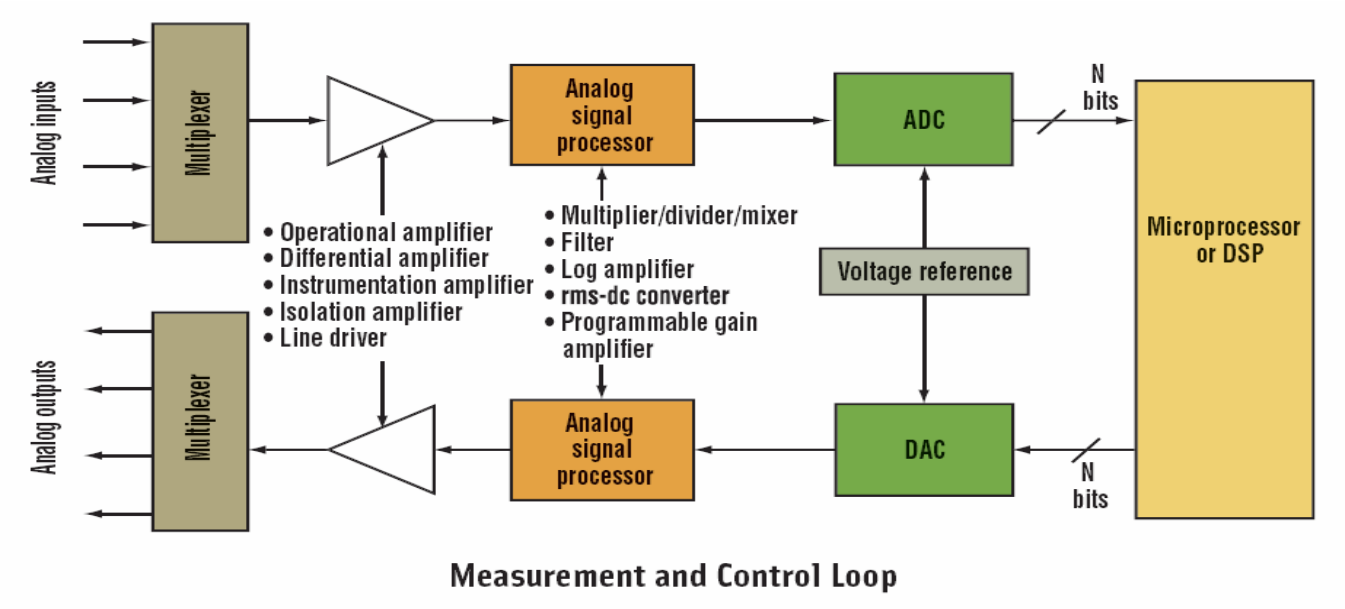
With grateful acknowledgment to Alan Belcher of Signal Conversions Ltd., Swansea, UK and Analog Devices Inc.

ADCs & DACs General Use

- **Interface between Analogue & Digital environments**
- **Trend is “Digital to the Antenna”**
- **Most ADCs contain DACs in a feedback loop**



Measurement and Control Loop

ADC DAC Subjects

- **Terms, nomenclature, standards and specs.**
- **Common ADC types**
  - **Will discuss DACs within ADC types**
  - **Flash**
  - **Pipeline**
  - **Successive Approximation Register (SAR)**
  - **Charge Balance, DVMs**
  - **Delta Sigma**
- **Applicability of types**
- **Some application problems & solutions**
- **The future for accelerators?**

Terms, Nomenclature & Specs

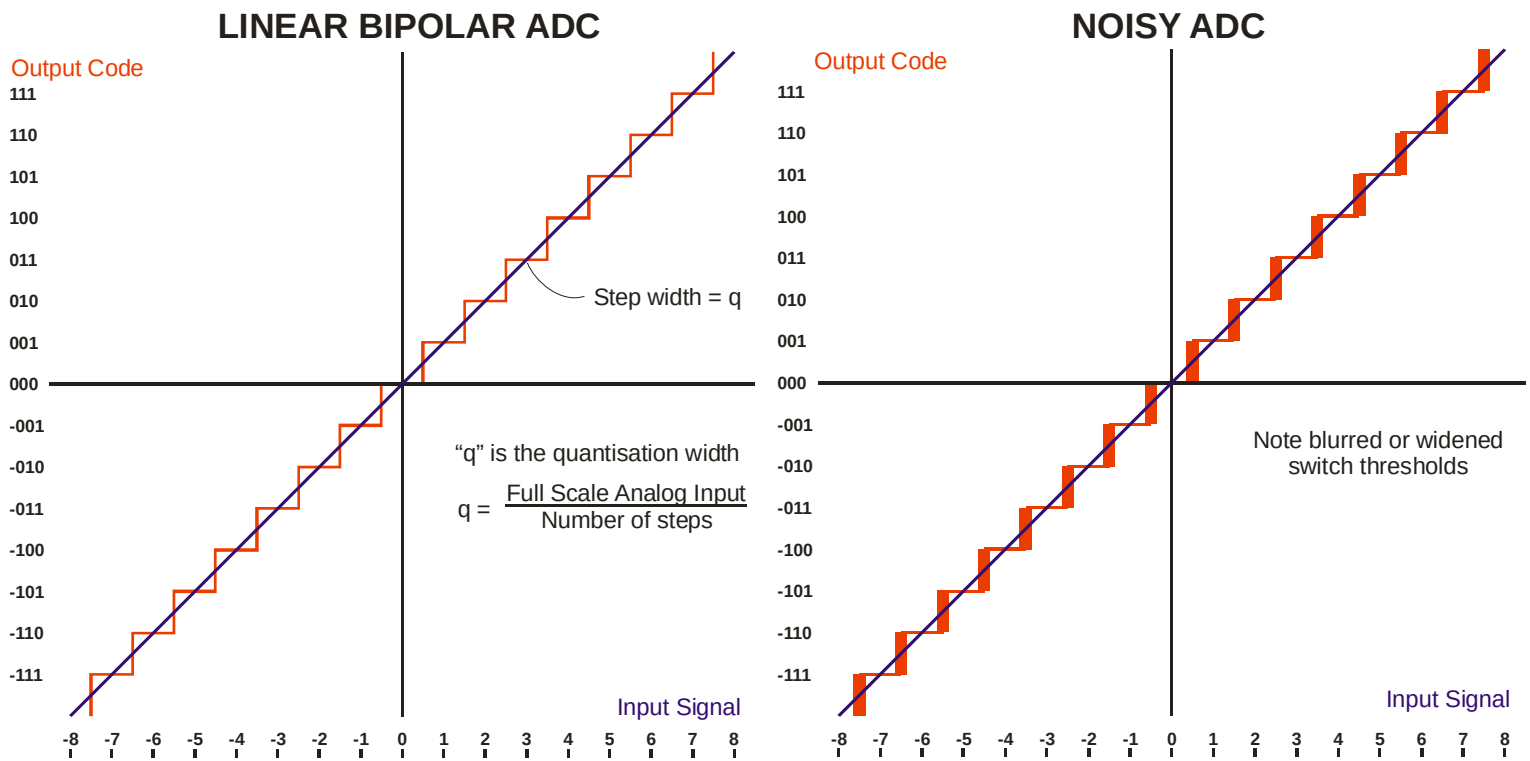
- **Many terms relate to AC measurement**
  - **Eg “SINAD”, “Over-sampling”**
  - **Standards IEEE1241 and DYNAD are primarily for Dynamic performance**
    - ***Methods & draft standards for the DYNamic testing of Analog to Digital converters, European project SMT4-CT98-2214***
- **Many misunderstood terms and specs.**
  - **Eg. “resolution”, “linearity”, “noise”**
  - **Useful general standard is IEC 60748-4**
    - ***Currently being updated to include dynamic performance by incorporating IEEE1241 and DYNAD***

Terms, Nomenclature & Specs

- **Resolution…the first quantity to know!**
  - **"Smallest *repeatably* discernable increment", ie resolvable increment.**
    - ***IEC 60748-4 says, for ADCs, "nominal value of the step width" THIS IS QUITE WRONG IN MY VIEW.***
    - ***Very often applied as "N" bits or "digits" where it is the theoretical, error free, noise free digital scale increment***
    - ***The term resolution is not even defined in IEEE1241 and DYNAD!!***
- **Noise….the second?**
  - **ADCs generally specify in RMS % of the bipolar scale length. DVMs in peak % of unipolar scale length.**
    - ***This is a 6:1 difference!!***

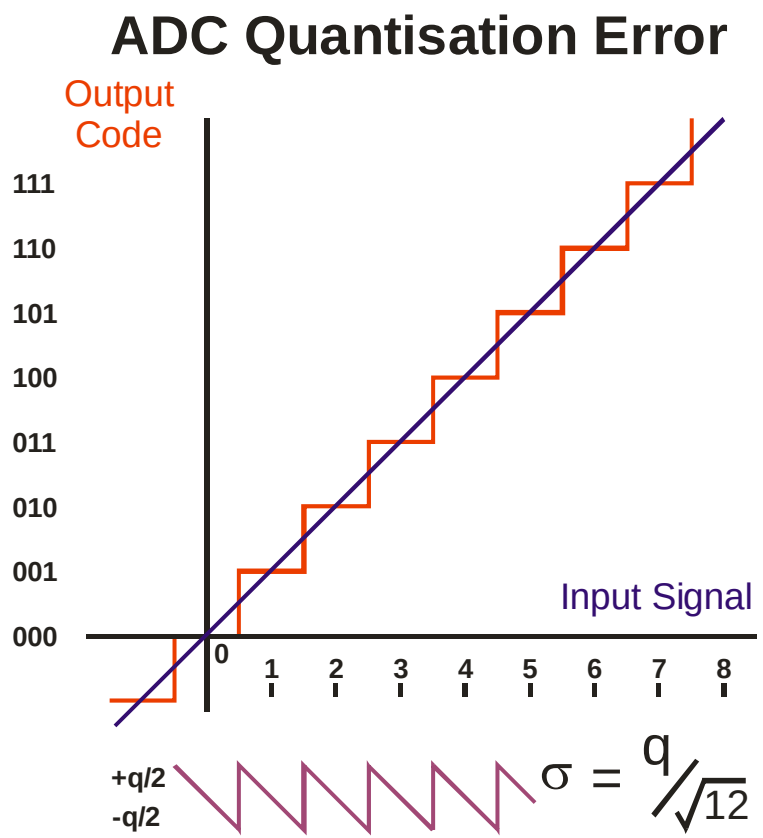
Terms, Nomenclature & Specs

- **A perfect Bipolar ADC transfer function**



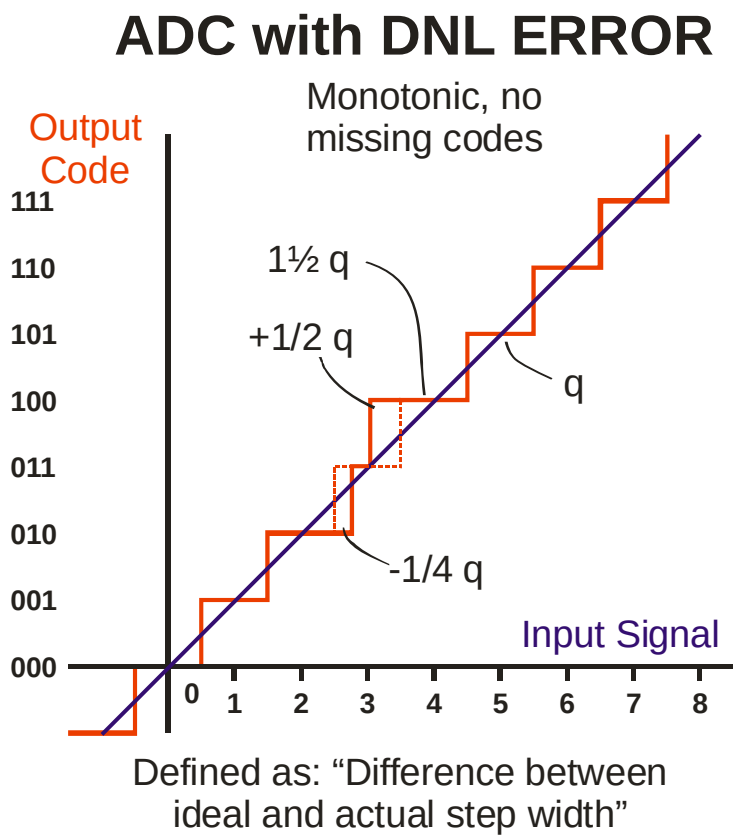
Terms, Nomenclature & Specs

- **Quantisation Error**
  - **"q" is the width of the LSB in linear ADCs**
  - **As input signal is increased the error has a saw-tooth distribution.**
  - **Peak error in an ideal ADC is q/2.**
  - **Standard deviation is q/√12**
  - **Dynamically, "quantisation noise" is therefore ……q/√12 RMS**



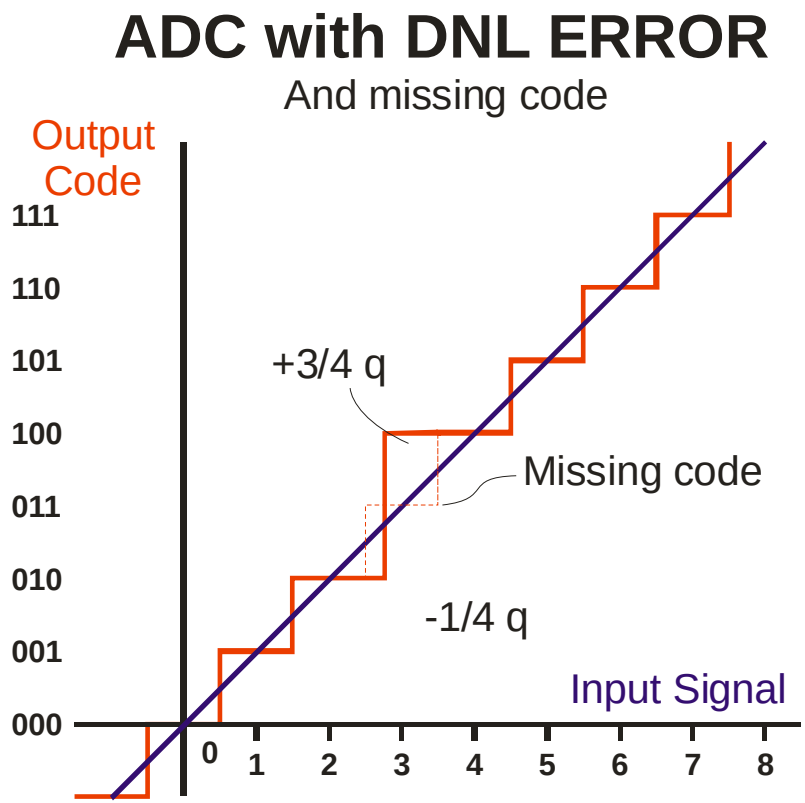
Terms, Nomenclature & Specs

- **DNL…Differential Non-Linearity**
  - **Defined as the difference between ideal and actual step width**
  - **Significant problem in SAR ADCs and ladder DACs at major code transitions**
  - **Can be many bits.**
  - **Think of as a sudden step change in output.**



Terms, Nomenclature & Specs

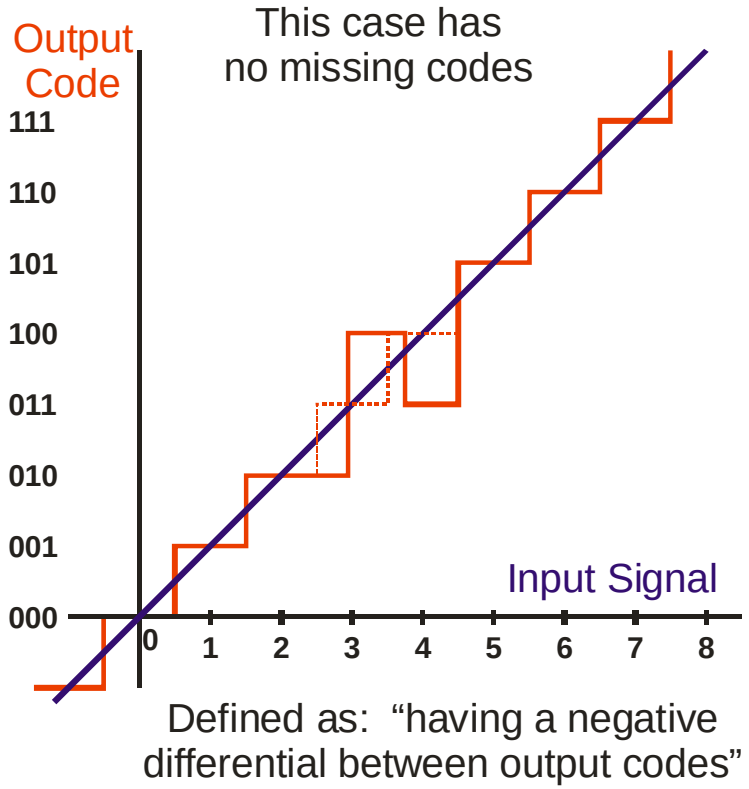
- **Missing Codes**
  - **Extreme DNL, especially if > 1 LSB, can lead to missing codes and non-monotonic performance.**



Terms, Nomenclature & Specs

- **Non-Monotonic**
  - **Usually taken to mean that different inputs can produce the same output code…ie two codes.**
  - **In this unusual example all codes are unique although one is wrong.**
  - **Definition is that the differential output takes a negative value for +ve differential input (and vice versa).**

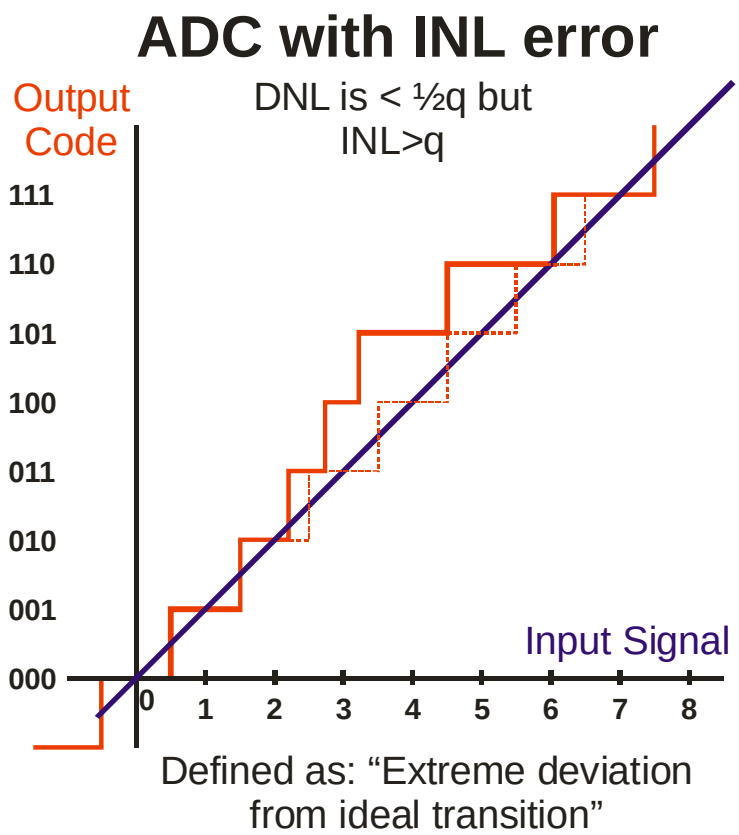
NON-MONOTONIC ADC



Defined as: "having a negative differential between output codes"

Terms, Nomenclature & Specs

- **INL…Integral Non-Linearity**
  - **Usually the limiting performance for high resolution, low speed ADCs**
  - **Is actually an accumulation of DNL errors over many steps.**
  - **“ideal transitions” are assumed to be on a straight line. The line may be between calibrated end-points which is the worst case but for specmanship reasons, a best fit regression line is sometimes used**



Terms, Nomenclature & Specs

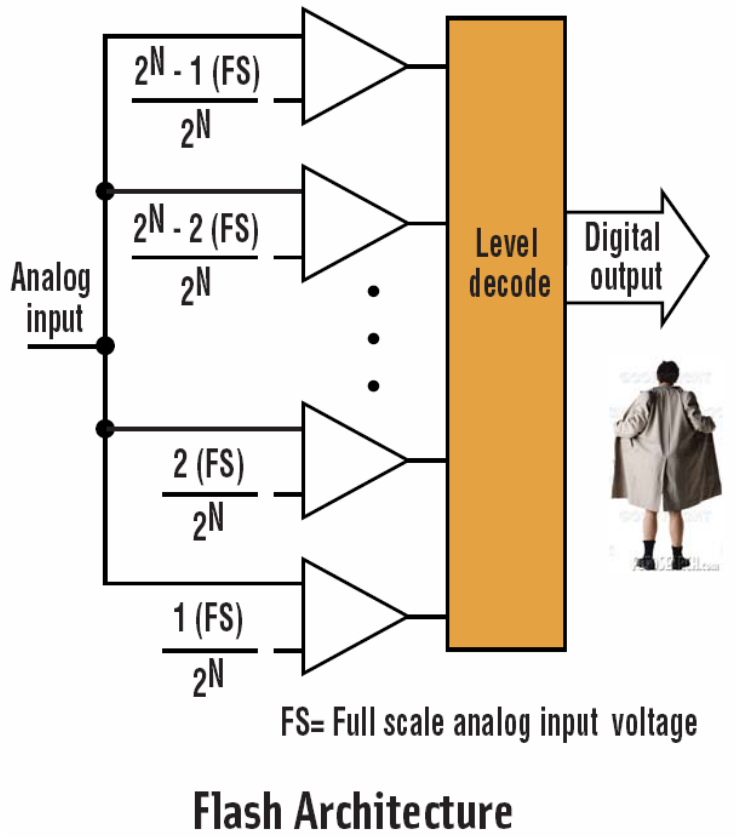
- **Dynamic terms mainly used for AC**
  - **SNR, Signal to Noise Ratio**
    - *Ratio in dB of the RMS of a full excursion sine wave to the RMS of all of the noise including quantisation noise (with that signal applied and therefore specified).*
  - **SFDR, Spurious Free Dynamic Range.**
    - *Ratio in dB of the value of a full scale sinewave signal to the highest spurious or harmonic tone generated by the ADC's operation*
  - **SINAD, Signal to Noise and Distortion.**
    - *As SNR but including all distortion terms, treated as noise*
  - **N_{ef} or "ENOB", effective number of bits.**
    - *The effective resolution of the converter under the above conditions.*

$$N_{ef} = (SINAD_{dBFS} - 1.76dB)/6.02$$

  - **"Oversampling"…A confusing term for DC!!**
    - *Sampling faster than the Nyquist rate, ie faster than 2X the signal bandwidth. This is an inadequate description for DC since, by definition it is infinite. In reality "oversampling" ADCs and DACs improve measurement of AC or DC by averaging multiple samples in the presence of dither or noise.*

Flash ADCs

- **At its simplest a single comparator…….**
  - **In practice one comparator per level or 2^n-1 for "n" bits.**
  - **A 16 bit converter therefore needs 65,535 comparators with thresholds set to an accuracy of .0015% of FS!**
  - **However, at low resolution is often a sub-component in other types of ADC architecture.**



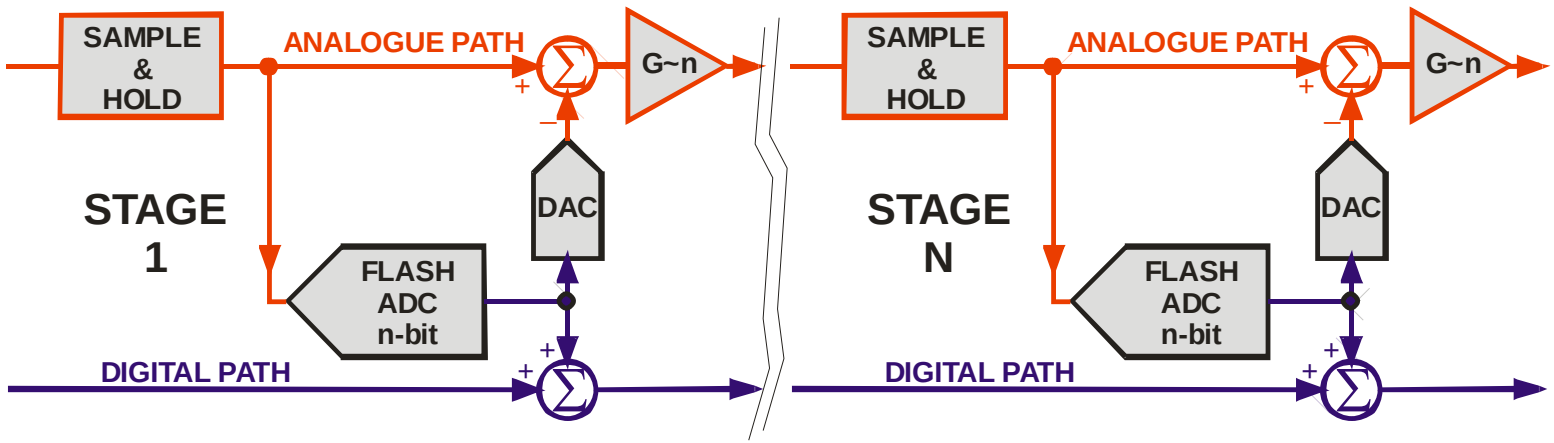
Flash Architecture

Flash ADCs, characteristics

- **The flash ADC is one of the few types that does not include a DAC in a feedback loop**
  - **This means that there is the shortest possible path between signal and output, ie between Analogue and Digital.**
    - ***Flash converters are very fast, the fastest available.***
    - ***They have very short delays as well as high bandwidth.***
    - ***They are therefore relatively easy to integrate into feedback loops.***
    - ***They are used within both Pipeline and Σ-Δ converters.***

Pipeline Converters

- **Pipeline ADCs are multi-stage flash converters**
  - ***If the resolution of each stage is the same, say n bits, then the result is n^N bits where N is the number of stages. In practice 1 bit or more is "lost" in each stage to allow calibration correction.***



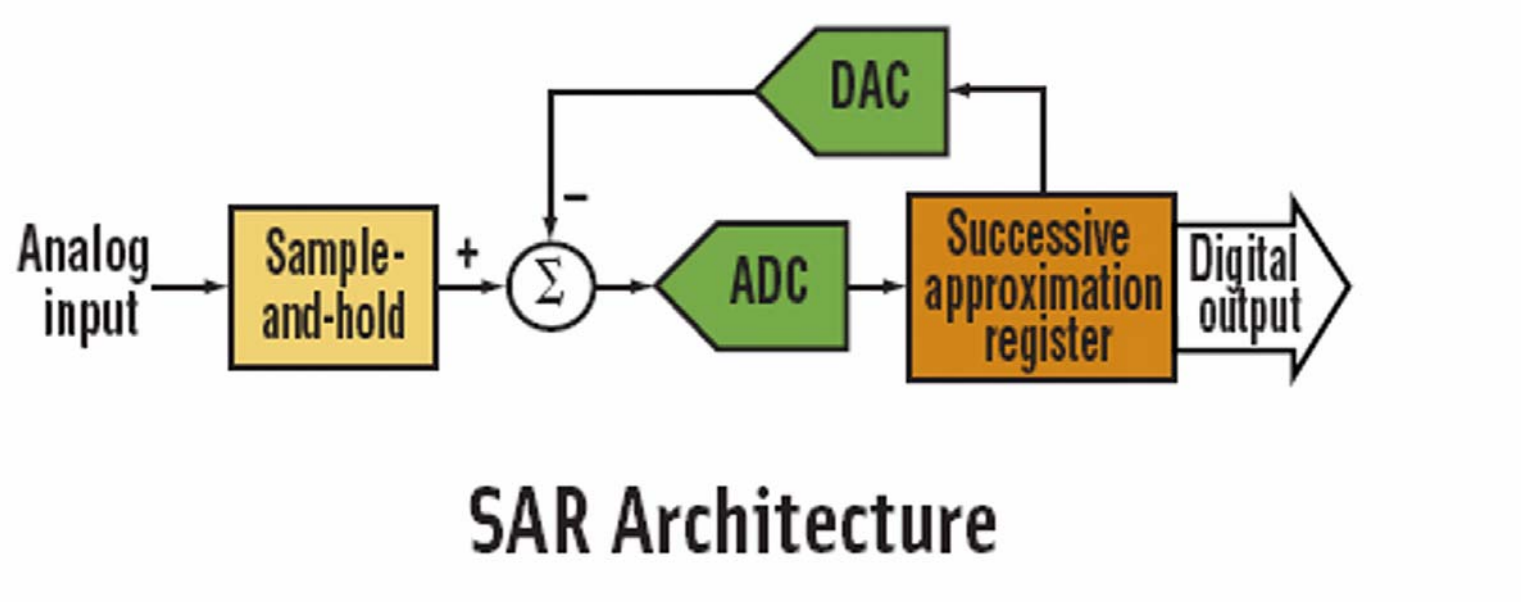
Principle of Pipeline ADC with n^N bits

Pipeline Converters, characteristics

- **Commercial Converters…**
  - **Are typically 10 to 16 bits, 5MHz to 25MHz bandwidth**
  - **Are clocked at 10MHz to 50MHz**
  - **“Pipeline” 3 to 8 stages requiring one clock per stage.**
    - ***This results in significant delay which can be high compared with the bandwidth. This delay can be very problematic when they are used within feedback loops.***

Successive Approximation, SAR

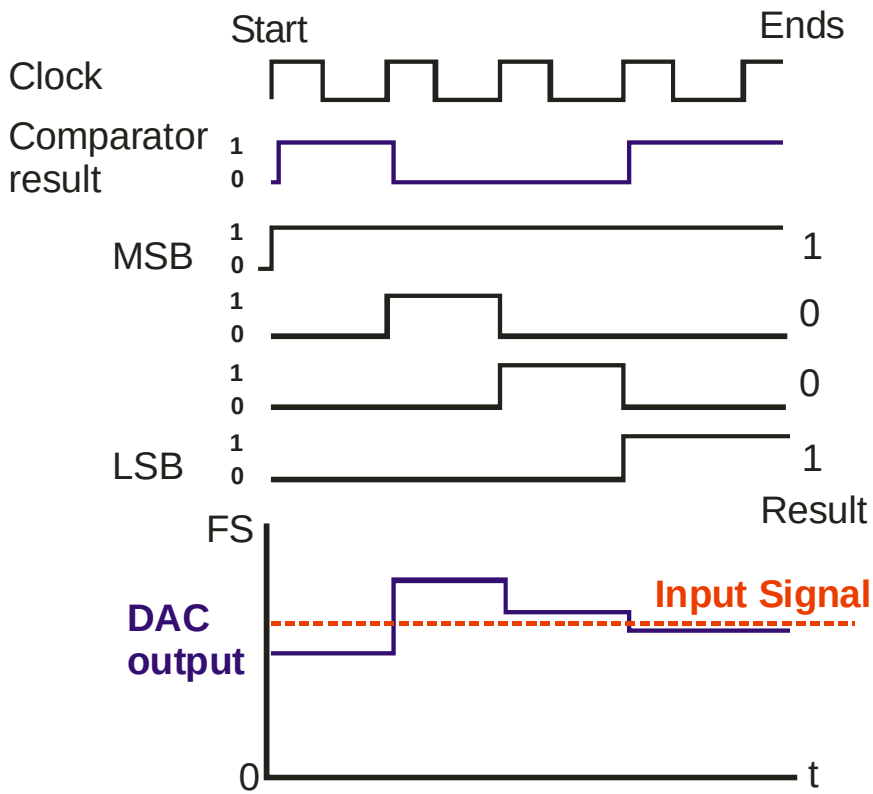
- **SAR ADCs use ladder DACs in a feedback loop to iterate towards a null balance between the signal and the DAC output.**
  - ***The ADC in the diagram below can be a simple comparator or a Flash Converter.***



SAR Architecture

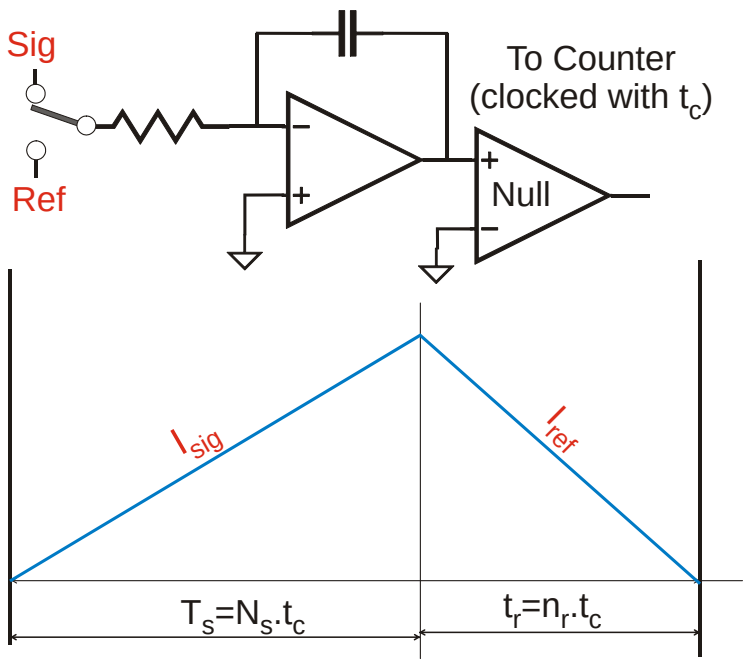
SAR, operation and characteristics

- **Typically the converter divides the scale in two and tests successively for the DAC > or < the signal. Each test sets a “1” or “0” in the register at the appropriate weight**
  - **Capable of higher resolution than pipeline at somewhat lower speed.**
  - **Since it uses a binary ladder network, high order bit transitions can cause very bad DNL**



Charge Balance, Dual-slope

- **Dual Slope A-D Sequence and Schematic**



- **Charge Balance equation**

Charge integrator with signal (I_{sig}) for fixed period T_s

Discharge for variable period t_r with known reference (I_{ref})

$$I_{sig} \cdot T_s = I_{ref} \cdot t_r$$

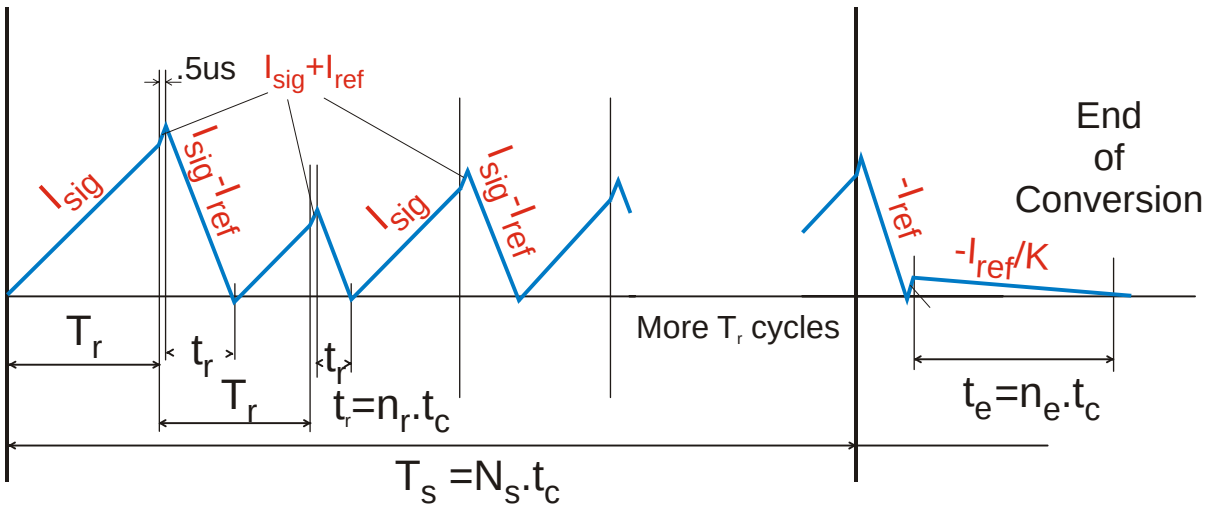
$$\therefore I_{sig} = t_r \cdot \frac{I_{ref}}{T_s}$$

$$I_{sig} \cdot N_s \cdot t_c = I_{ref} \cdot n_r \cdot tc$$

$$\therefore I_{sig} = n_r \cdot \frac{I_{ref}}{N_s}$$

Charge Balance, Multi-slope

- **The Multi-slope makes two key improvements:**
  - ***Removes "glugs" of reference charge allowing a smaller integrator cap and thus higher gain to reduce effect of null detector noise.***
  - ***Ends at a slow (but known) discharge rate whilst counting at reduced digital significance thus improving resolution by "K" without a faster clock.***



Charge Balance, characteristics

- **Most DVMs use Charge balance ADCs**
  - ***But tend not to use ADC terminology and are specified in terms of near worst case measurement errors. They also treat each polarity as having its own "FS". They are optimised for DC so speed is slow.***
- **DVM specifications expressed as A-D "bits"**
  - ***The following table gives ADC equivalent specs and is for a high end DVM, however, this is an 18 year old design!***

Specification Description	DVM data-sheet specification	ADC "bit" specification
Nominal resolution:	±8½ digits	28+ bits
Real (2σ) resolution	±7½ digits	24+ bits
Integral Non-linearity (INL)	0.1ppm ($1X10^{-7}$)	23 bits
Differential Non-linearity	No spec. "perfect"	28 bits

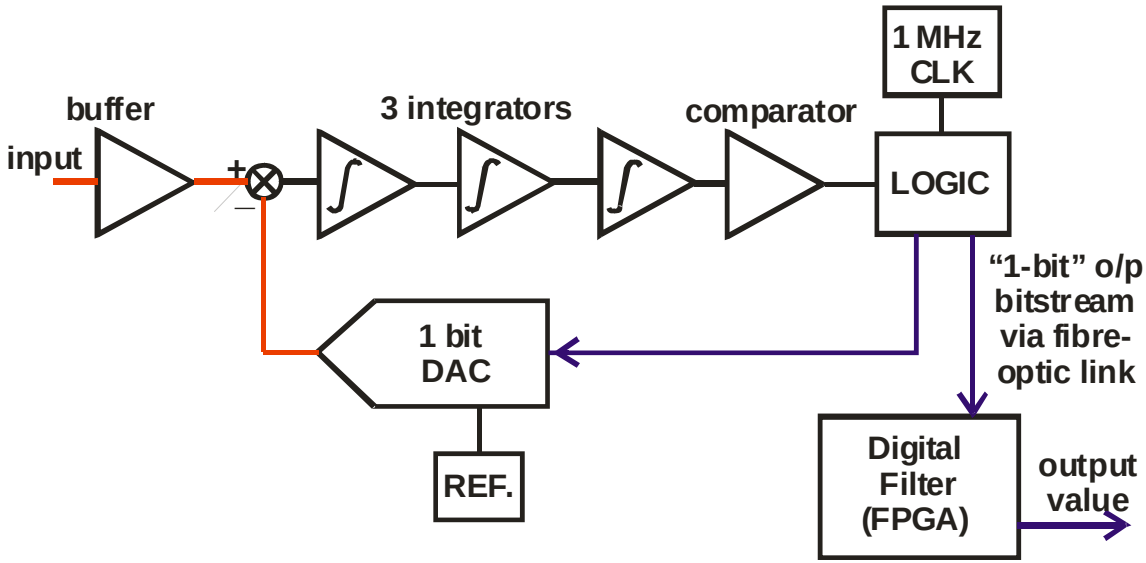
Charge Balance v Sigma-Delta

- **Charge Balance "Rule"**
  - ***Charge IN = Charge OUT***
  - ***The best possible resolution is the smallest discrete charge that can be determined, compared with the total charge.***
  - ***This normally means the ratio of t_c to T_s but in multi-slope this is extended by reducing the final charge current.***

- **The CERN Sigma-Delta**
  - ***A Sigma-Delta ADC was designed at CERN for controlling magnet currents to 1ppm. (ADDA 1999).***
  - ***It uses a 1 MHz "1-bit" topology with a digital filter that settles to 1ppm in 1000 clocks:- thus only 1000 quanta so:***
    Charge in $\neq$ Charge out!!
  - ***It has been proven to reliably resolve 1ppm!***

Sigma-Delta

- **Most Sigma-Delta ADCs use a "1-bit" DAC**
  - **The CERN architecture is shown below:**



Note that DACs based on the same Σ–Δ principle simply "swap" over the digital feedback and analogue input paths to give analogue feedback and a digital input bitstream that can be optimised for best response.

Sigma-Delta, 1-bit, 200 clocks

- **Excel Simulation Output for 1 bit Σ–Δ, 4X50 dig filter**
  - **The plot below shows the output of the last three filter registers over the last 140 out of 210 clocks. The Y scale is +/- 0.5%FS.**

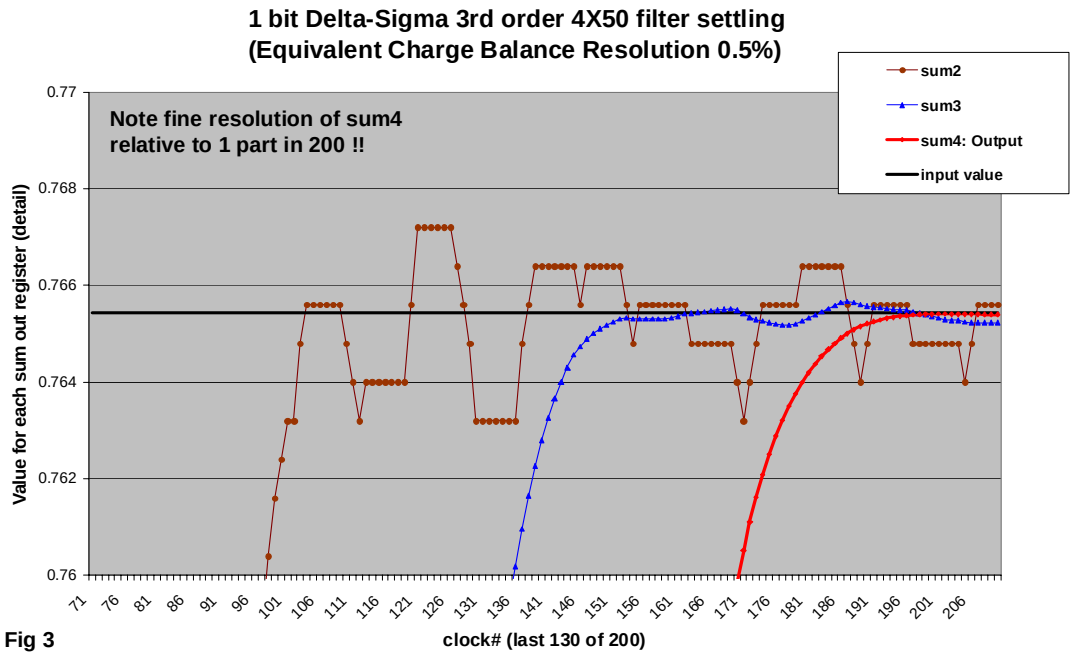


Fig 3

In this time dual-slope would only achieve a resolution of 1/200, ie 0.5%!

Sigma-Delta characteristics

- **Commercial Integrated Circuit (IC) converters**
  - **Mainly designed for audio frequency AC**
    - ***Therefore specs tend not to be DC & LF "friendly"***
    - ***High manufacturing volume means low cost***
  - **Bandwidths are DC to 200kHz**
    - ***Noise-Resolution trade-off is readily available***
    - ***Considerable delay "latency" in dig filter***
    - ***But the digital filter can be tapped at different points and sampled concurrently. This may allow "feed-forward" techniques to be used in loop controlled systems***
  - **DC performance is usually limited…look carefully!**
    - ***Although "24 bit" devices are claimed, the stability and linearity is really in the 18 bit region for the best "merchant semiconductor" IC devices.***

Sigma-Delta characteristics

- **Problem Characteristics**
  - **"Idle tones"**
    - ***Bit patterns can repeat at low frequency if the Σ–Δ loop does not "randomise" enough, a particular tendency in 3rd order or below.***
    - ***These are called tones because they show up as low level 1Hz-300 Hz lines in an FFT analysis of output.***
    - ***They are, at least in part, due to unwanted feedback in the modulator. PCB layout and supply filtering is critically important.***
  - **"Sticky Zero"**
    - ***Perhaps can be considered as a DC "idle tone" this shows up as a tendency to maintain a symmetrical, zero condition, bit pattern in the modulator when operating just off zero. Synchronous noise, particularly in reference switching edges, is often the culprit.***

Choosing the right type

- **The following table attempts to "score" the suitability of a technology against application requirements**

\ADC type Requirement\	Flash	Pipeline	SAR	Charge Balance	Sigma-Delta
Throughput:	excellent	v.good	good	poor	fair
Bandwidth:	excellent	excellent	v.good	v.poor	fair
Resolution:	poor	good	v.good	excellent	excellent
Latency/Hz:	excellent	fair	v.good	poor	fair
Multiplexing:	excellent	poor	v.good	fair	poor
Linearity/bit:	v.good	good	fair	v.good	v.good
Comments:	Power! Cost	v.fast clock	DNL stability	DC only	Easy Anti-alias

Choosing the right spec.

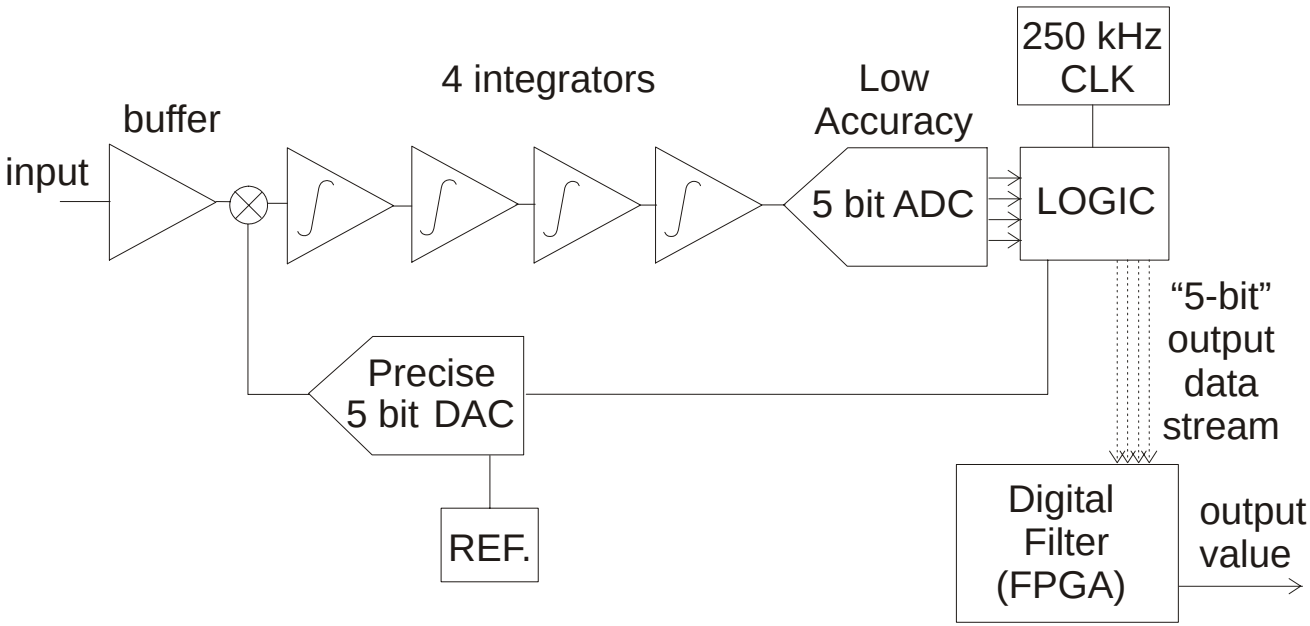
- **Choice of ADC**
  - ***After choosing the type of ADC there are important specification subtleties to consider***
  - **Internal/External Reference**
    - ***Most IC ADCs and DACs use low voltage CMOS technology and therefore internal references, if offered, are based on bandgap technology. These have high 1/f noise so an external Zener based reference may give significantly better performance.***
  - **Bipolar Operation**
    - ***Many ADCs/DACs are designed to be unipolar and there can be some difficulty or performance degredation in converting to bipolar.***
  - **Overloads**
    - ***Look at how cleanly overloads are dealt with and the consequent system implications.***
  - **Linearity**
    - ***INL is often <u>ORDERS</u> worse than the "bit" spec quoted***

Application Problems

- **Noise, Noise, Noise!**
  - **High frequencies**
    - ***Use "ground" planes on PCB***
    - ***Bury HF traces between planes on PCB***
    - ***Make signal traces differential if possible***
    - ***Use Common mode chokes***
    - ***Think HF current paths, minimise length, make differential***
    - ***Make smooth "flow" Analogue-to-Digital***
    - ***Remember aliasing and provide adequate filtering***
  - **Additional for Low frequencies**
    - ***Use "meccas" to control current paths: think current!***
    - ***Remember 1/f cannot be averaged out***
    - ***Thermal EMF balance, avoid air flow if possible***
    - ***Chopper stabilise sensitive input stages***

Application of fast ADC

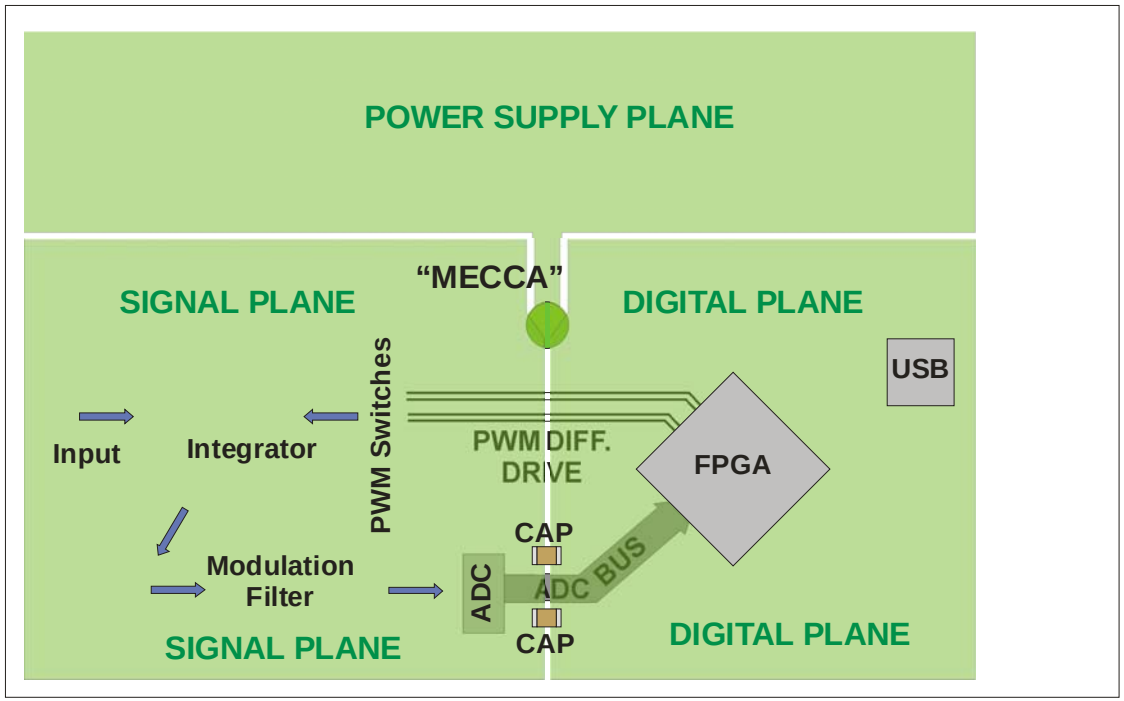
- **Enhanced Performance with 5 bit DAC**
  - **5 bit 4th order gives excellent performance.**



Application Layout

- **Using a fast ADC in a Sigma Delta loop**

- **Think Current!**
  - *Uses 20MHz ADC inside 28 bit loop sensitive to <1uV*
  - *PWM drive has sub ns edges.*
  - *MECCA controls LF currents*
  - *HF currents out & return locally*
  - *PWM differential*
  - *ADC bus return via caps between planes*



Finally…why not use the cryogenics?

- **Use Josephson Junction Arrays for the DAC**
  - **Future accelerator applications could take advantage of local cryogenics to use Squids and Josephson arrays.**
    - ***Low resolution high accuracy JJ arrays are being developed now. They could realise the full potential of the Sigma-Delta ADC architecture.***