11 EMBEDDED MEMORY

OVERVIEW

Embedded memory is any non-stand-alone memory. It is an integrated on-chip memory that supports the logic core to accomplish intended functions. High-performance embedded memory is a key component in VLSI because of its high-speed and wide bus-width capability, which eliminates inter-chip communication.

During the past several years, a lot of development has taken place in the embedded memory market. Most recently, many new products were introduced with embedded memory, with a particularly high interest in embedded DRAM.

Figure 11-1 shows the increasing performance gap between microprocessors and DRAMs. As this gap has widened, chip designers placed greater emphasis on the development of embedded memory devices. Their task was made easier by at least two factors. First, the complexity of process technology made it possible to incorporate logic and memory on the same chip. Secondly, larger die size allows the incorporation of both logic and memory on the same chip.

Several advantages of using embedded memories are provided below. They include reduced number of chips, reduced pin count, multi-port memories, less board space requirements, faster response with memory embedded on-chip, dedicated architecture, memory capacity specific for an application, reduced power consumption, and greater cost effectiveness at the system level.

The main disadvantages of embedded memories are that they are generally larger in size and are more complex to design and manufacture. Additionally, a trade-off must often be found between design and technology since the optimized technology for a memory cell is not the same as that for embedded logic devices. Furthermore, processing becomes even more complex when the designer integrates different types of memory on the same chip. Figure 11-2 presents a DSP from Texas Instruments that includes embedded memories. Note that the memory portion consumes about half the total area of the chip. RAM, ROM, and logic on one chip makes for a challenging design and for challenging manufacturing.

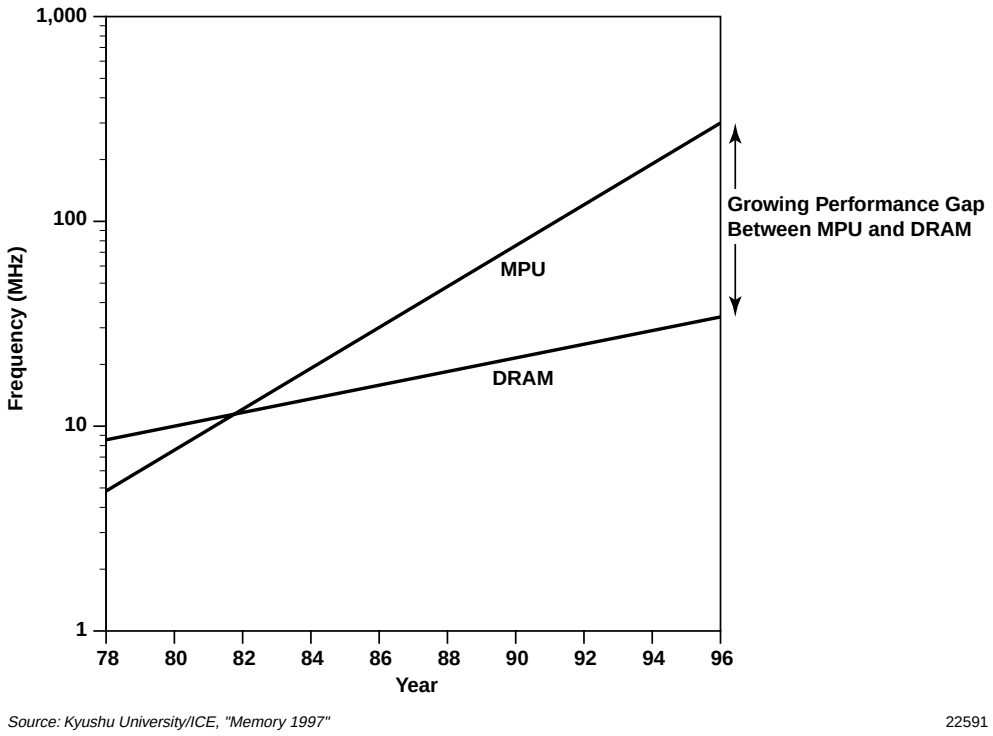
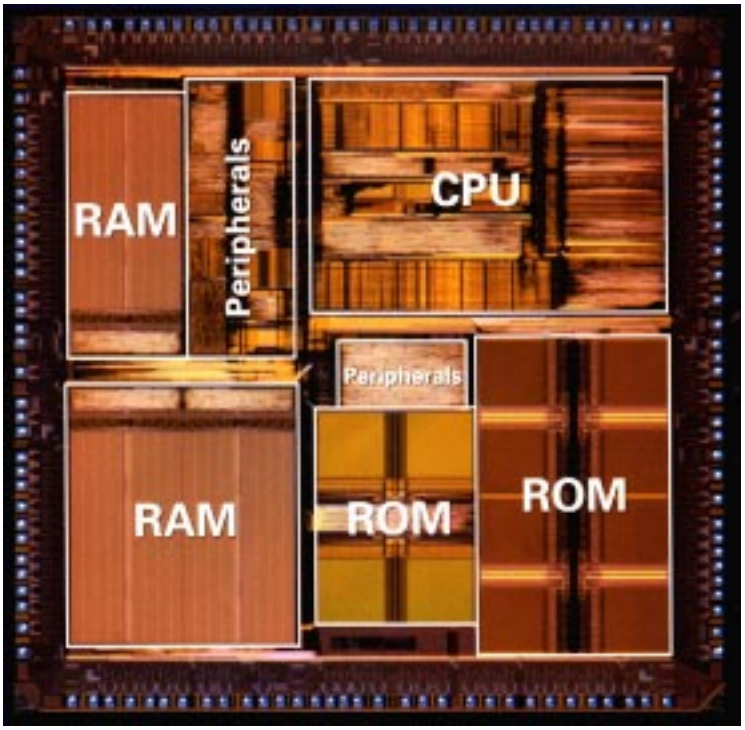


Figure 11-1. MPU Versus DRAM Performances

Figure 11-3 shows the key differences between embedded and stand-alone flash memories. On a standard memory device, cell size is the most critical issue. However, if the memory area is not a significant part of the full chip area, cell size is not a critical factor for a chip with embedded memory. For this reason, chip designers will often use a conservative cell design for embedded memories. EPROM, flash, or DRAM may have more than one transistor per cell. SRAM will often use the CMOS six-transistor (6T) cell design instead of the four-transistor (4T) memory design, along with some additional transistors.

EMBEDDED DRAM

Embedded DRAMs are in the introduction phase of the product lifecycle. Due to the complexity of DRAM process technology, suppliers did not quickly develop embedded DRAMs. Embedded DRAM capacitors that store data require several processing steps not needed when making logic devices. The threshold voltage of DRAM transistors must be high enough to ensure that they will not create memory cell capacitor leakage. This constraint on low sub-threshold current may cause some speed penalty on the logic portion of the device. DRAM processes are a central issue in an embedded DRAM device using a process developed for logic chips.



Source: TI/ICE, "Memory 1997" 22600

Figure 11-2. TI's 1-V DSP for Wireless Communications

	Embedded	Stand-Alone
Typical Array Size (Bits)	2K - 2M	1M - 16M
Typical Percent of Chip Area	5% - 40%	100%
Cell Size Very Critical	No	Yes
Cell Type	NOR	NOR/NAND/AND
Dual Gate-Oxide	Likely	Not Likely
Multiple Modules	Yes	No
Redundancy Repairing	Rare	Yes

Source: Motorola/ICE, "Memory 1997" 20813

Figure 11-3. Key Differences Between Embedded and Stand-Alone Flash Memories

In 1996 and 1997, numerous announcements were made regarding embedded DRAMs, revealing the great interest in this type of device. Until recently, DRAMs were the least-used embedded memory cell due to process complexity.

Embedded DRAMs will become a more widespread solution to designer needs as on-chip memory increases and the use of system-on-a-chip rises. One reason for the interest in embedded DRAM is speed. As illustrated in Figure 11-4, embedded DRAM offers a large increase in memory bandwidth performance compared to several other currently used alternatives. Most of the current embedded DRAM developments are for graphics and multimedia applications.

Memory Type	Bandwidth
Standard (256K x 16)	240MB/sec.
High-Speed (256K x 16)	400MB/sec.
2MB x 8 RDRAM (Rambus DRAM)	500MB/sec.
SDRAM (Synchronous DRAM)	640MB/sec.
Embedded DRAM (32K x 256)	2,560MB/sec.

Source: Silicon Magic Corp/ICE, "Memory 1997" 20811A

Figure 11-4. Memory Bandwidth Comparisons

Several companies are developing embedded DRAMs. Figure 11-5 shows a sampling of DRAM/Logic devices that have recently been introduced. Silicon Magic is a 1994 fabless startup that develops embedded DRAMs for systems requiring very high memory bandwidth. They offer a chip that combines graphics, audio, and video functions with DRAM.

At the 1996 ISSCC conference, Mitsubishi presented a 32-bit Multimedia RISC microprocessor with 16Mbits of embedded DRAM. This device was manufactured using a 0.45µm, double-metal technology process. It also included 16Kbits of cache SRAM. Figure 11-6 shows a description of this product.

Toshiba announced two ASIC families with embedded DRAM. One is based on the company's one-transistor DRAM trench capacitor cell process technology while the second family is based on its three-transistor cell logic process.

DRAM Memory Cell

The memory cell of standard DRAM memory chips consists of one transistor and one capacitor. In the new DRAM generations, the capacitor is either a trench or stack capacitor design.

Company	Product	Comments
NeoMagic	MagicGraph	Graphics controller chip for notebook computers that has 1M of embedded DRAM. Available now.
Silicon Magic	Max-H	IC that couples 1.25M of DRAM with VGA graphics acceleration, audio, and MPEG-1 decompression fuctions. Available now.
Mitsubishi	M32R/D	32-bit RISC processor (54MIPS at 66MHz) and 16M DRAM. Device is built using 0.45μm, two-layer metal technology. Die size: 153.7mm^2. Available now.
NEC	PIP-RAM	Parallel-image processing (PIP) RAM for real-time image processing applications. PIP-RAM integrates 16M DRAM and 128 8-bit processors. In development stage.
Hitachi	"Media Chip"	Prototype optimized for 3-D graphics. The device integrates four 2M DRAM macros and four pixel processors.
SGS-Thomson	Omega	The chip integrates DRAM, ST-20 microprocessor core, an MPEG Audio and video recorder, and SRAM cache memory.

Source: ICE, "Memory 1997" 21211A

Figure 11-5. Companies Explore DRAM/Logic on Same Chip

CPU core	32b RISC architecture
VAX MIPS	52.4 MIPS at 66.6 MHz (Dhrystone V2.1)
Memory	16Mbit DRAM with 16KBit cache (SRAM)
Peripheral logic	32b x 16b DSP-like multiply accumulator memory controller, etc.
External bus	24b address, 16b data
Clock	66.6MHz (internal) / 16.67MHz (external)
Supply voltage	3.3V
Power	700mW(typ.) / ≤2mW (stand-by)
Die size	153.7mm^2
CPU size	5.7mm^2
Process technology	0.45μm CMOS, 2-metal layers
Package	80-pin plastic QFP

Source: ISSCC 1996/ICE, "Memory 1997" 20832

Figure 11-6. Mitsubishi Multimedia 32-bit RISC Chip Overview

The memory cell of embedded DRAMs using a standard logic process will often be a three-transistor design with separate read and write access. An additional capacitor is sometimes added to ensure a minimum value of 30pF. The larger the capacitor, the less sensitive to noise or alpha particle induced soft error the memory cell will be. Figure 11-7 shows the different types of DRAM cells. The advantages of a three-transistor cell over a one-transistor cell are compatibility with standard digital CMOS technology, higher access speed, dual-port (separate read and write access ports) and nondestructive readout.

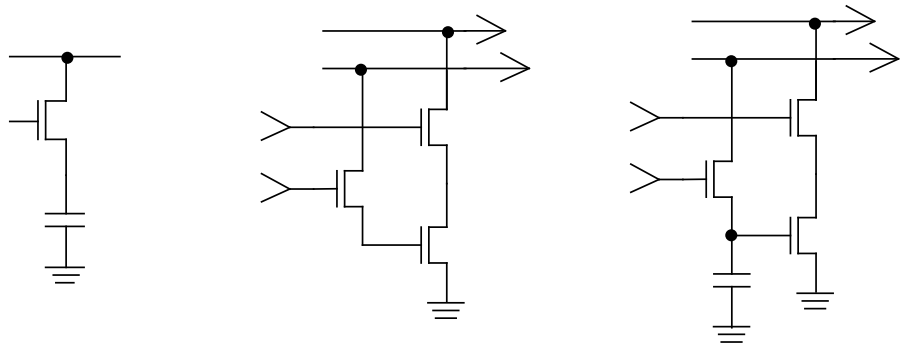


Figure 11-7. DRAM Memory Cells

An illustration of this embedded DRAM design diversity was made by Toshiba. The company proposed both a one-transistor cell and a three-transistor cell for ASIC applications. The one-transistor cell is based on a 0.25µm DRAM trench capacitor process and is proposed for applications needing 1Mbit to 32Mbit DRAM density. The three-transistor cell is based on a 0.3µm logic process and is proposed for applications needing no more than 1Mbit DRAM density.

EMBEDDED SRAM

Embedded SRAM is widely used. The embedded SRAM market is even larger than the stand-alone SRAM market! Whether faster speed, greater density, or lower power consumption, several vendors have emerged to supply improved embedded-SRAM devices.

SRAM as Cache Memory

Most CPUs, DSPs, and MCUs have a small quantity of cache memory on chip. This on-chip memory is called primary cache or level-one (L1) cache. L1 cache is backed up by a larger off-chip secondary or level-two (L2) cache. Figure 11-8 shows the quantity of L1 cache used in AMD and Intel MPUs.

SRAM in ASIC

SRAM cells are also implemented in ASICs. They may be used for the programmability or implemented as a block. Figure 11-9 shows a block diagram of Actel's 3200DX FPGA that incorporates blocks of high speed (5ns) dual-port SRAM.

	AMD-K5	AMD-K6	Intel P55C	Pentium Pro
L1 Cache	16Kbytes instr 8Kbytes data	32Kbytes instr 32Kbytes data	16Kbytes instr 16Kbytes data	8Kbytes instr 8Kbytes data
MMX?	No	Yes	Yes	No*
Out-of Order Execution?	Yes	Yes	No	Yes
Max Clock	100MHz	180+MHz	200MHz	200MHz
Voltage	3.3V	~2.9V	2.5V	3.3V
Transistors	4.3 million	8.8 million	4.5 million	5.5 million
IC Process	0.35μm	0.35μm	0.28μm	0.35μm
Metal Layers	3M	5M	4M	4M
Die Size	181mm^2	180mm^2	140mm^2	196mm^2
Production	Now	1H97	1H97	Now

***Klamath, a single-chip version of the Pentium Pro, will feature MMX technology.**

Source: MDR/Vendors/ICE, "Memory 1997" 21738A

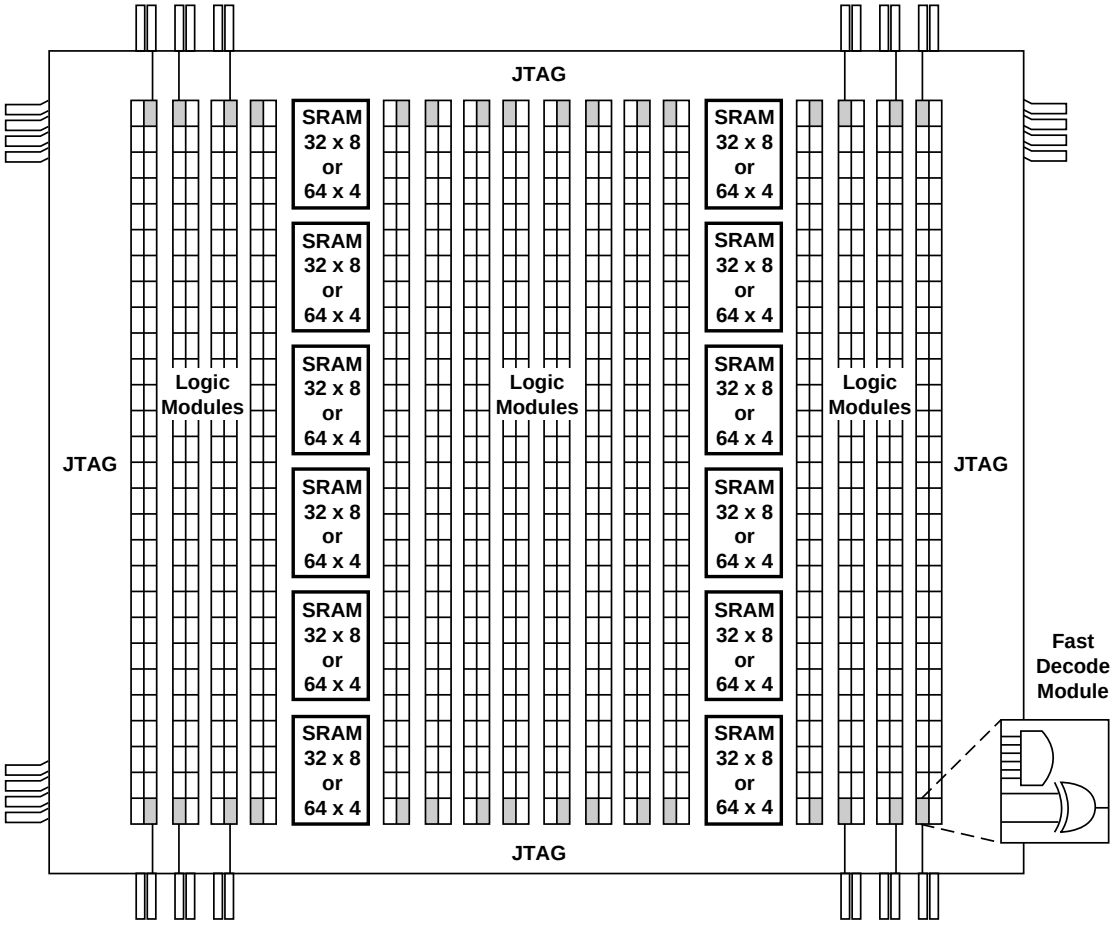
Figure 11-8. L1 Cache in AMD and Intel MPUs

6T SRAM Cell

A six-transistor CMOS architecture will be often used to make the SRAM memory cell. This architecture provides better electrical characteristics (speed, power consumption, noise immunity) and is compatible with a logic process as only one polysilicon level is required. The cell size, however, is larger than a four-transistor cell. Figure 11-10 shows SRAM cell dimensions of CPU products analyzed by ICE's laboratory. All the SRAM cells presented on the list are six-transistor cells.

Embedded SRAMs can also utilize more transistors than the classical 6T cell. This helps improve the electrical performance of the embedded circuit. Also, multi-port memory cells are also often used as embedded SRAM.

Figures 11-11 and 11-12 show two embedded SRAMs using more than the classical 6T structure. Figure 11-11 presents a cell implemented in an ASIC from IBM that uses nine transistors for a cell size of 120 square microns (0.6μm channel length). Figure 11-12 presents a cell implemented in a CPLD from Philips that also utilizes a nine-transistor cell.



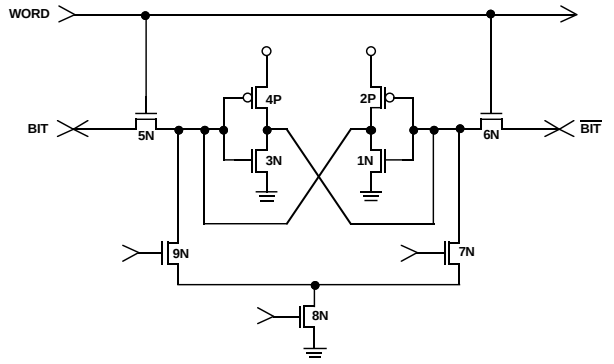
Source: Actel/ICE, "Memory 1997" 20409

Figure 11-9. Actel's 3200DX FPGA Architecture

Product	Gate Length (μm)	Cell Type	Cell Size (μm^2)
Sun Ultra-Sparc 143MHz	0.45	6T	63.7
Intel Pentium Pro 200MHz	0.3	6T	49.0
Cyrix/IBM 6x86	0.35	6T	44.0
DEC Alpha	0.4	6T	43.0
Motorola PowerPC 604e	0.25	6T	36.0

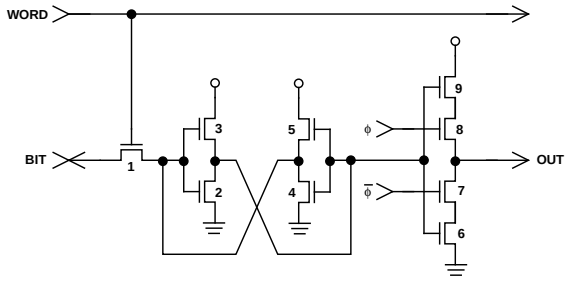
Source: ICE, "Memory 1997" 22593

Figure 11-10. L1 SRAM Cache Cell Dimensions



Source: ICE, "Memory 1997" 22601

Figure 11-11. 9 Transistor SRAM Cell (IBM)



Source: ICE, "Memory 1997" 22602

Figure 11-12. 9 Transistor Design Cell (Philips)

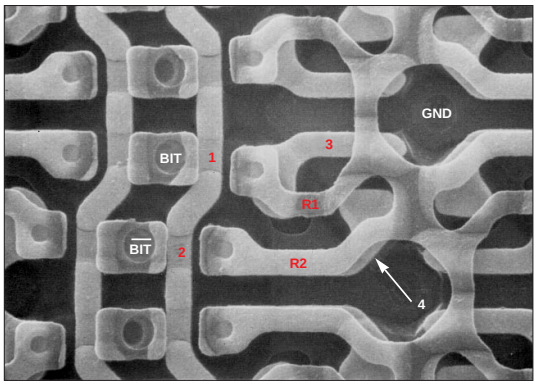
4T SRAM Cell

There are at least two reasons that a company would consider using 4T SRAM cells for embedded memory. First, if the size of embedded memory is important, the use of a smaller memory cell is necessary. Secondly, if a company has experience in stand-alone 4T cell SRAM architecture, it may prefer to implement that architecture in its embedded SRAM application. This is the case of IDT. As illustrated in Figures 11-13 and 11-14, the same SRAM used for its 256Kbit SRAM is used in as embedded SRAM (L1 cache) on its 79R4600 RISC processor.

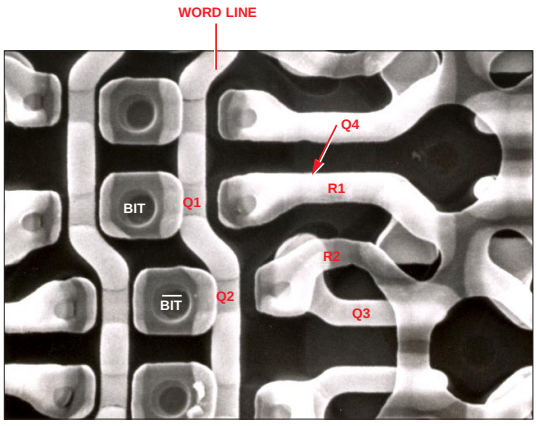
Product	Cell Type	Week Code	Technology	Cell Dimensions (μm)	Cell Area (μm^2)
256K SRAM	4T	9323	0.6μm	8.5 x 5.3	45.1
RISC Processor	4T	9439	0.45μm	7 x 4.5	31.5

Source: ICE, "Memory 1997" 22605

Figure 11-13. Comparison of IDT's Stand-Alone and Embedded SRAM Cells



EMBEDDED SRAM



256K SRAM

Source: ICE, "Memory 1997" 22603

Figure 11-14. Top Views of IDT's SRAM Cells

EMBEDDED ROM

Like embedded SRAMs, there are probably more embedded ROM developments than stand-alone ROM memory shipments. ROM cells do not need a specific technology. Various programming methods may be used such as metal contact, channel implant, and field oxide. The selection of programming method involves a trade-off between cost, cell size, and cycle time. If random high speed is required, the ROM will use a NOR architecture. If this speed requirement is not needed, the NAND architecture may be used to save space.

EMBEDDED EPROM

Figure 11-15 shows a two-transistor EPROM cell developed by Cypress and Altera for programmable logic device (PLD) implementation. The choice of using two transistors was done to separately optimize read and write floating gate transistors. This approach allows a better read current / area ratio compared to standard one-transistor EPROM or two-transistor EEPROM cells.

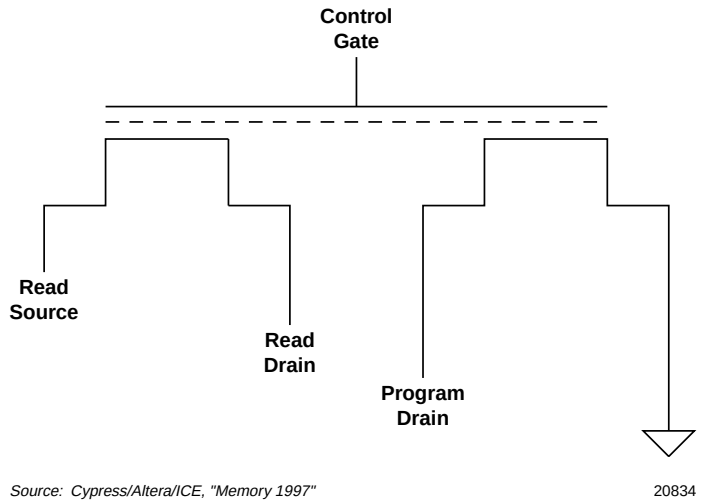


Figure 11-15. Schematic of High Speed 2T EPROM Cell With Separate Read and Write Transistors

One-Time Programmable (OTP) Memory

As product design cycles get shorter, it is more important for MCU suppliers to offer one-time programmable (OTP) memory as an option on their MCU chips. Manufacturers must be flexible enough to rapidly adapt to changing market opportunities. One problem with ROM is that programming, setup, and engineering changes are economical only when system manufacturers purchase large quantities of identically programmed MCUs. Furthermore, if system manufacturers make a software change, the lead time for receiving MCUs with the new program in ROM may be many months.

OTP devices can come programmed or unprogrammed from the semiconductor manufacturer. A single MCU model can be used in a variety of products by varying the program, or the system can be customized to a customer's specific needs. This flexibility reduces the variety of MCUs that the systems manufacturer must stock, which in turn reduces inventory.

EMBEDDED EEPROM

The more common embedded EEPROM devices are made of one polysilicon layer as illustrated by Figures 11-16 and 11-17. Both cells are implemented on programmable logic devices.

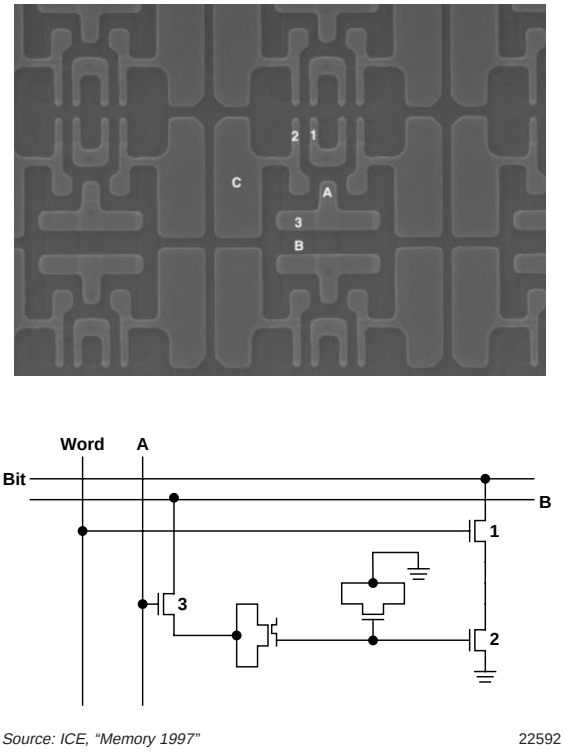
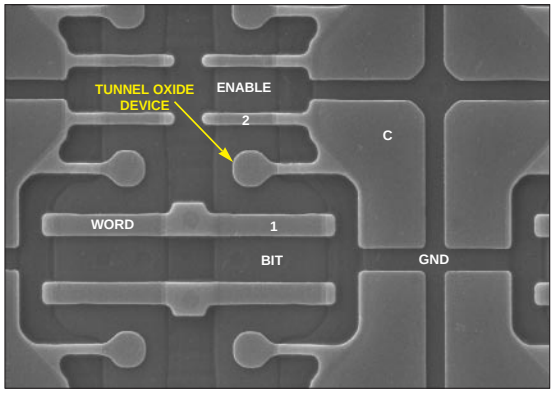


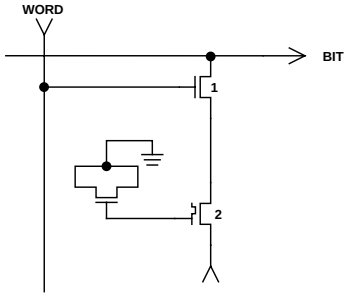
Figure 11-16. PZ5032 CPLD EEPROM From Philips

The main interest of these designs is to use only one level of polysilicon and thus be compatible with a standard CMOS process. They will, however, have an additional step to create the thin oxide of the floating gate needed for programming the cell.

EMBEDDED FLASH MEMORY

Another non-volatile memory option to use is embedded flash memory. As standard flash memories take EPROMs and EEPROMs market shares, flash memories will also replace these types of cells in the embedded applications. Figure 11-18 shows a comparison between the different types of non-volatile memories for embedded applications.





Source: ICE, "Memory 1997" 22606

Figure 11-17. Lattice's Embedded EEPROM

	ROM	EPROM	Single Gate Flash	Split Gate Flash	EEPROM
Density	+++	++	+	-	---
Electrically Prog.	---	+	+	+	+
Electrically Erase.	---	---	+	+	+
Byte Erasable	-	-	-	-	+
Program Disturb	+	+	--	-	++
Over Erase/Program	+	+++	-	+	++
Process Complexity	+++	++	--	+	-
Manufacturability	+++	++	-	+	+
Cost	+++	++	+	+	--

Worst --- -- - + ++ +++ Best

Source: Motorola/ICE, "Memory 1997" 20810

Figure 11-18. Embedded Non-Volatile Memory Comparison

Reprogrammability and in-circuit programming capability provide a highly flexible solution to rapidly changing market demands. To meet these needs, several vendors have embedded flash memory onto their microcontroller or other logic devices. Siemens expects flash to be widely used in microcontroller applications, with as much as 80 percent of all embedded controllers using it in five years. Embedded flash memories may be used in a wide range of applications. Figure 11-19 shows which applications may need flash devices.

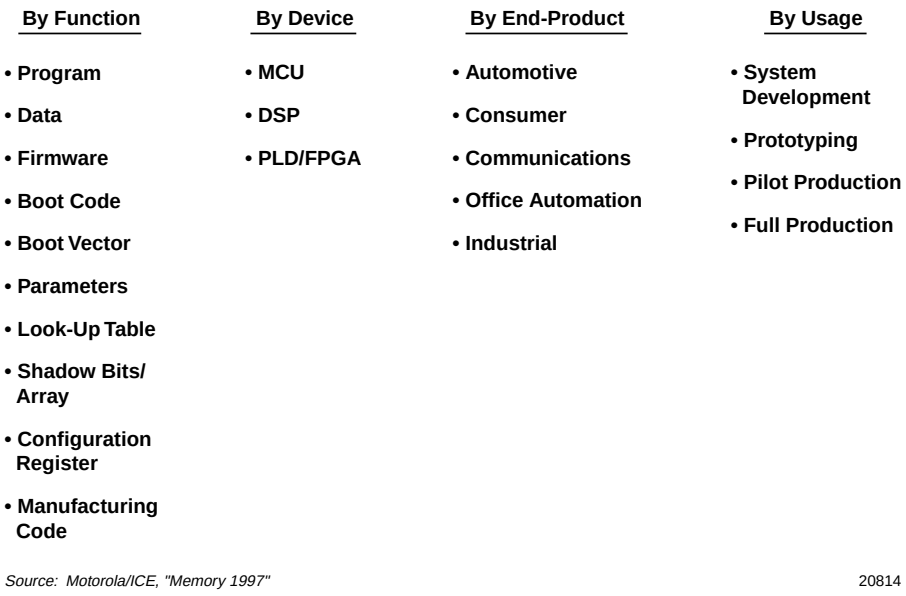
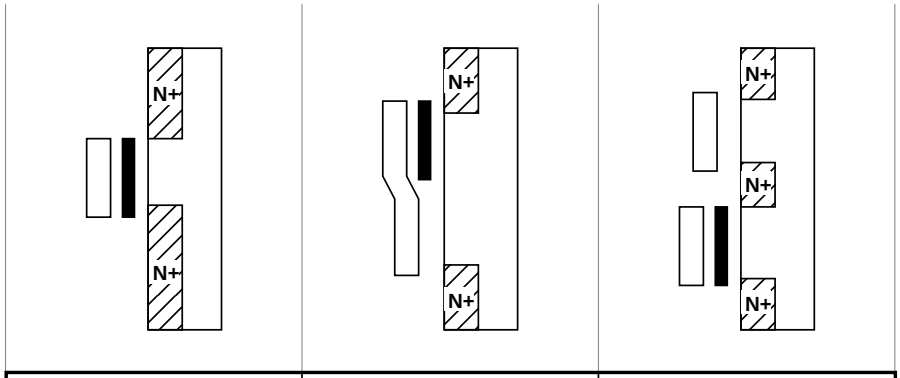


Figure 11-19. Embedded Flash Memory Applications

Like other embedded memory cells, flash memory design will be a trade-off between size, performance, and process compatibility. Figure 11-20 shows the advantages and disadvantages of different types of flash memory cell designs.

Smartcard Products

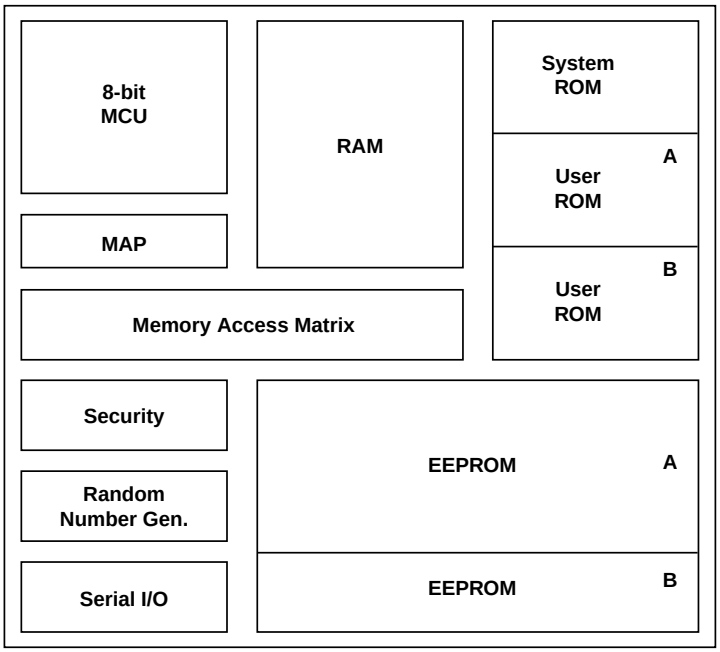
Smartcards are a new and fast growing market using embedded memory. Smartcards may incorporate MCU, different types of memory, advanced security features, and cryptographic processing. Figure 11-21 shows the chip organization of an advanced smartcard.



	Single Gate (1T Cell)	Split Gate (1.5T Cell)	Double Gate (2T Cell)
Advantages	• High Density	• No Over-Erase	• Full Isolation
Disadvantages	• Over Erase/Program • Program Disturb	• Larger Cell Area • Program Disturb	• Very Large Cell Area

Source: Motorola/ICE, "Memory 1997" 20809

Figure 11-20. Advantages and Disadvantages of Flash Memory Cell Gate Structures



Source: SGS-Thomson/ICE, "Memory 1997" 20835

Figure 11-21. Smartcard Chip Organization