3 PACKAGING

Packaging the IC chip is a necessary step in the manufacturing process because the IC chips are small, fragile, susceptible to environmental damage, and too difficult to handle by the IC users. In addition, the package acts as a mechanism to “spread apart” the connections from the tight pitch (center to center spacing of two parallel conductors) on the IC die to the relatively wide pitch required by the Printed Circuit Board (PCB) manufacturer.

A. PAD PITCH

The pad pitch on the IC chip is typically 0.006 inch (6 mils or 152µm). This spacing is already much larger than the 2 to 8 microns (0.08 to 0.31 mils) pitch of the wiring (metallization) on the IC chip. But PCB wiring requires an even larger pitch, usually between 40 and 100 mils. The package acts as a “bridge” between the two sizes, effectively spreading apart the spacing from the IC chip dimensions to the PCB dimensions, as shown in Figure 3-1.

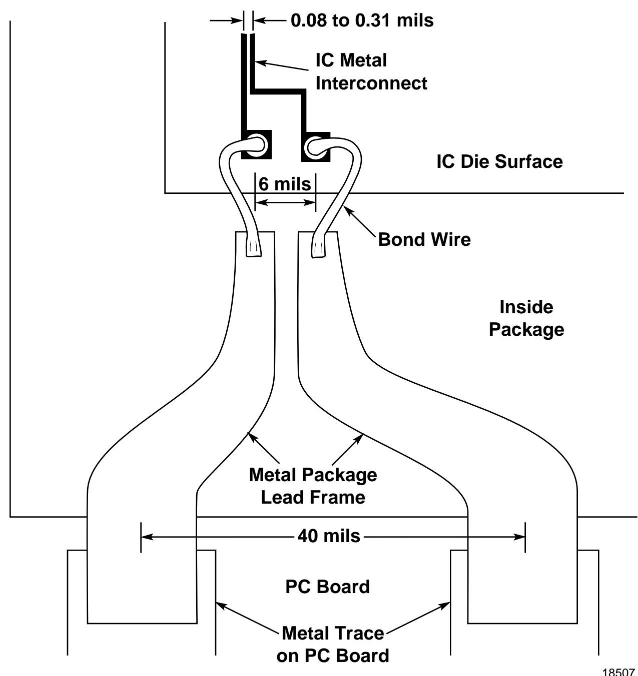

Figure 3-1. IC Chip to PCB Lead Spacing

Early packages were required to expand the pitch to the very large board pitch required for economical manufacture of PCBs used in commercial applications. In addition, the packages were mounted on the PCBs through plated holes, typically on 100 mil pitch. Three package types were used, ceramic and metal for hermetically sealed requirements and plastic for general commercial use. Hermetically sealed parts are ones where the IC chip is enclosed in a sealed compartment and outside chemicals and gases cannot reach the die.

B. DUAL IN-LINE PACKAGES (DIPs)

The case outlines of the plastic and ceramic Dual In-line Packages (DIPs) are nearly identical. The lead configuration consists of two rows of leads, both with 100 mil pitch. The plastic DIP is shown in Figure 3-2. The side-braze and cerdip packages are its hermetic alternatives. The cerdip shown in Figure 3-3 is considerably less expensive than the side-braze shown in Figure 3-4. Both packages are available with quartz windows in the top for EPROM devices so the chip can be erased with ultraviolet light.

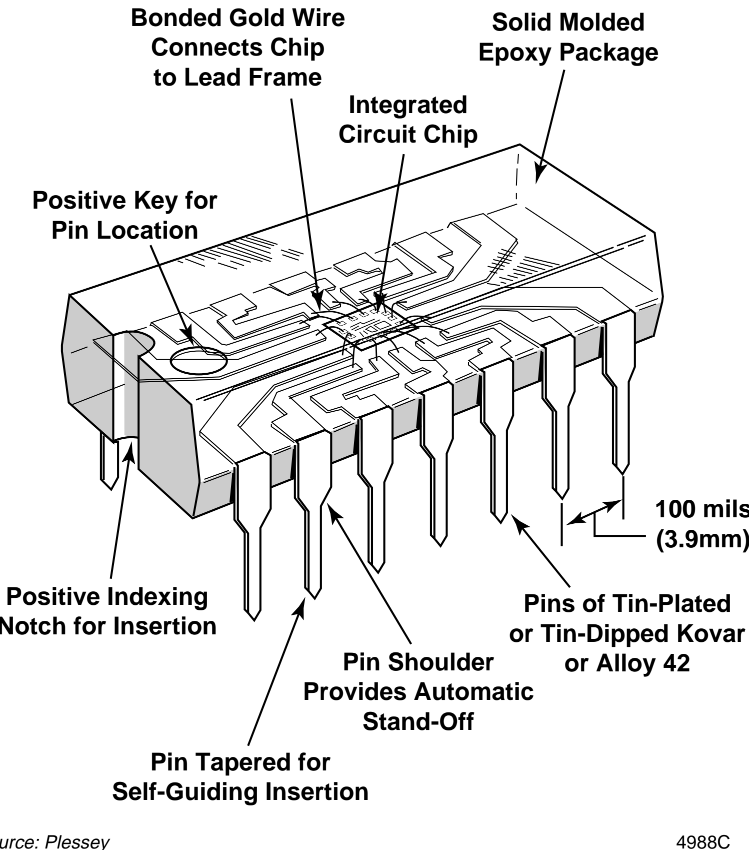

Figure 3-2. Plastic Dual In-Line Package

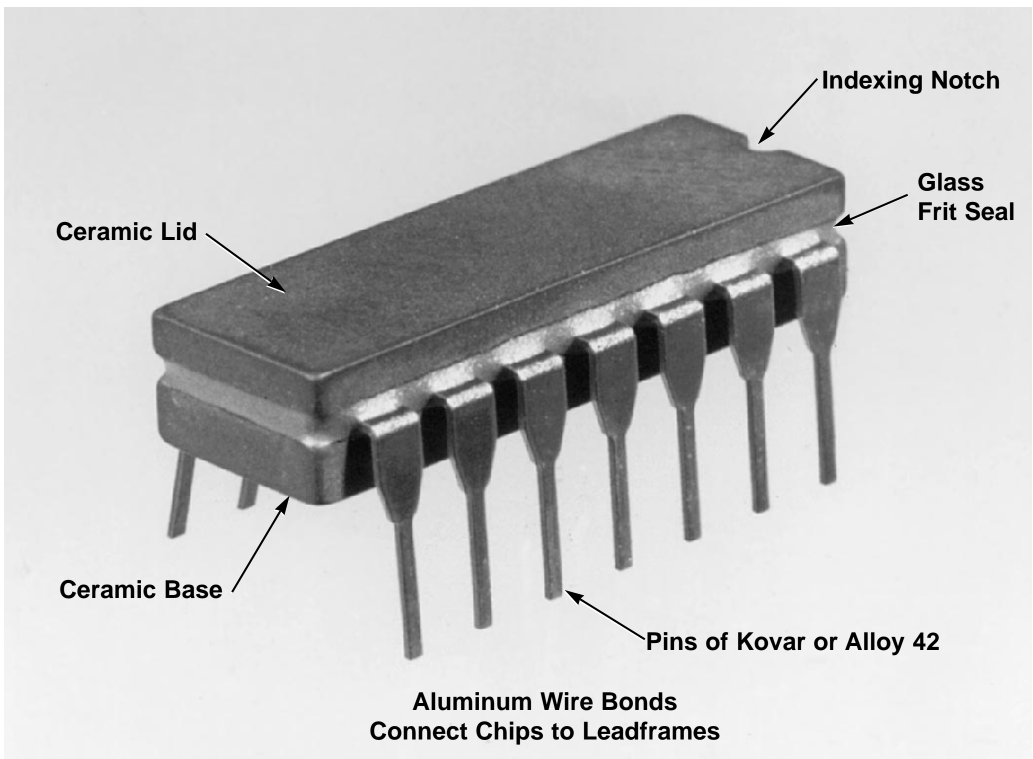

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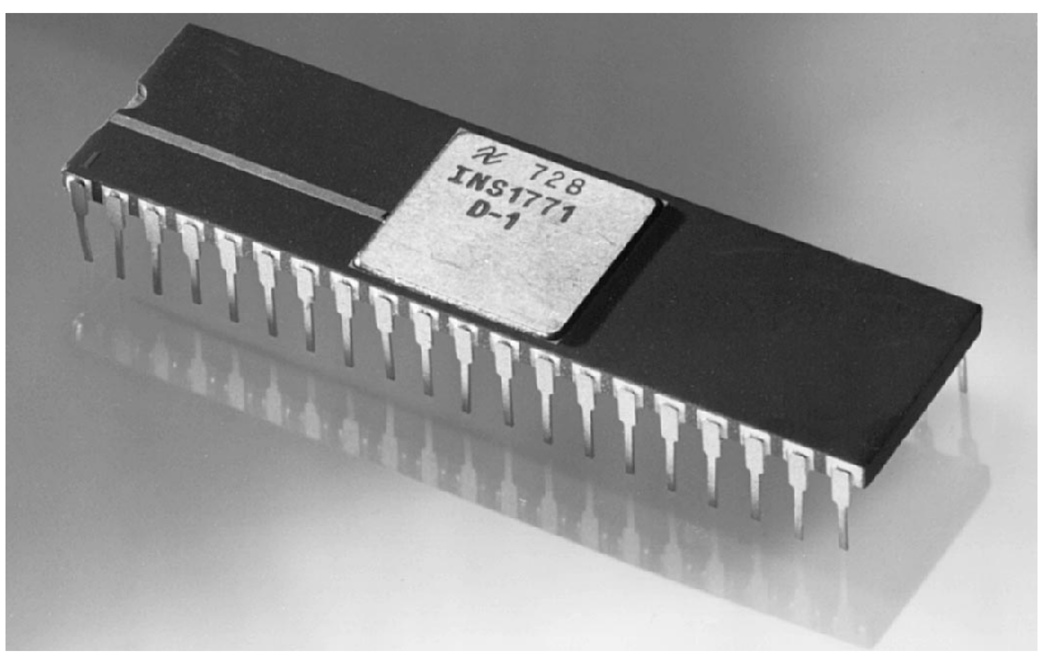
Figure 3-3. Cerdip Package



Courtesy of National Semiconductor 5311

Figure 3-4. Side-Brazed Ceramic DIP

C. SINGLE IN-LINE PACKAGES (SIPs)

Another alternative to the DIP is the single in-line package shown in Figure 3-5. To further reduce the PCB cost — which goes up as the wiring pitch is reduced — some manufacturers use the packages with staggered leads, such as the QUIP in Figure 3-6 or the SIP in Figure 3-7.

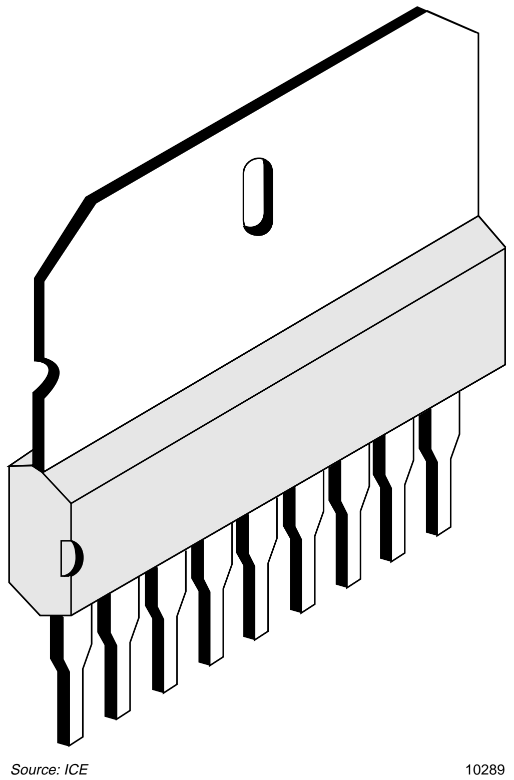


Figure 3-5. 9-Pin Single In-Line Package

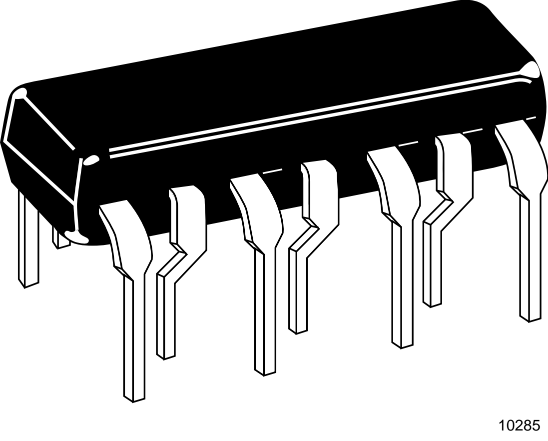


Figure 3-6. 14-Pin Plastic QUIP

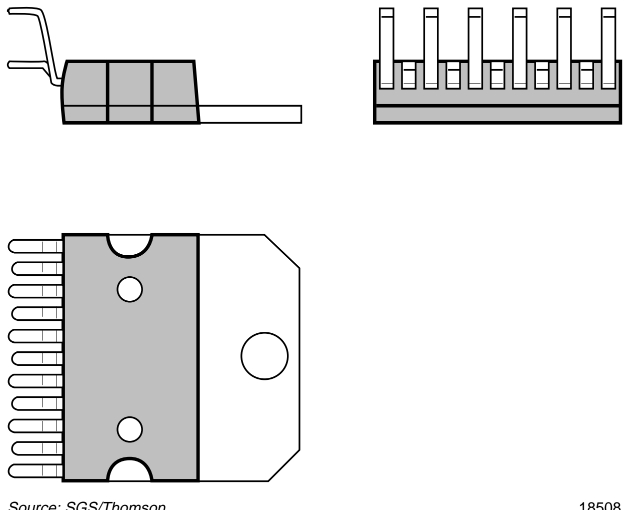


Figure 3-7. Multiwatt 11

D. CERAMIC FLATPACKS

A package used for early ICs in military and space applications was the ceramic flatpack, shown in Figure 3-8. The pitch on this package is 50 mils, allowing smaller system boards. The smaller pitch, however, requires more expensive board processing and more careful IC handling techniques, so the flatpacks were rarely used in commercial applications. These packages are manufactured using the cerdip approach because of the very thin package outline.

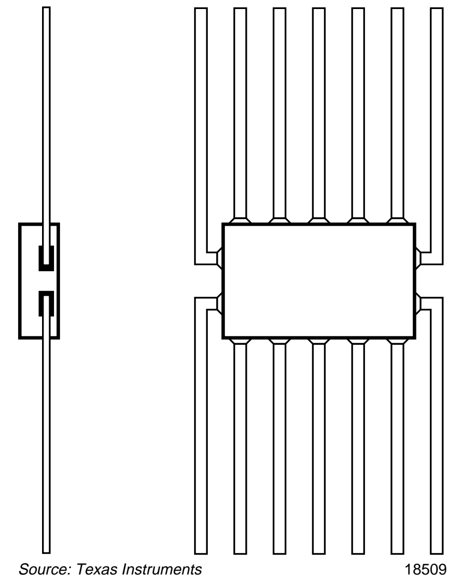


Figure 3-8. Flatpack

E. PIN GRID ARRAYS

The limitation of 100 mil minimum pin spacing for commercial PCBs is a significant problem for two reasons: high pin count IC chip requirements and board space needed for each IC. The first problem is solved by the Pin Grid Array (PGA) shown in Figure 3-9. Here, the pins remain on 100 mil pitch, but cover most of or all of the entire bottom surface of the package. These packages are offered in pin counts from about 100 to 600 pins, and are available with heatsinks (as shown in the figure) to help remove the heat generated inside the package. This can be a problem with fast clock rate microprocessor chips where the frequent switching generates significant heat.

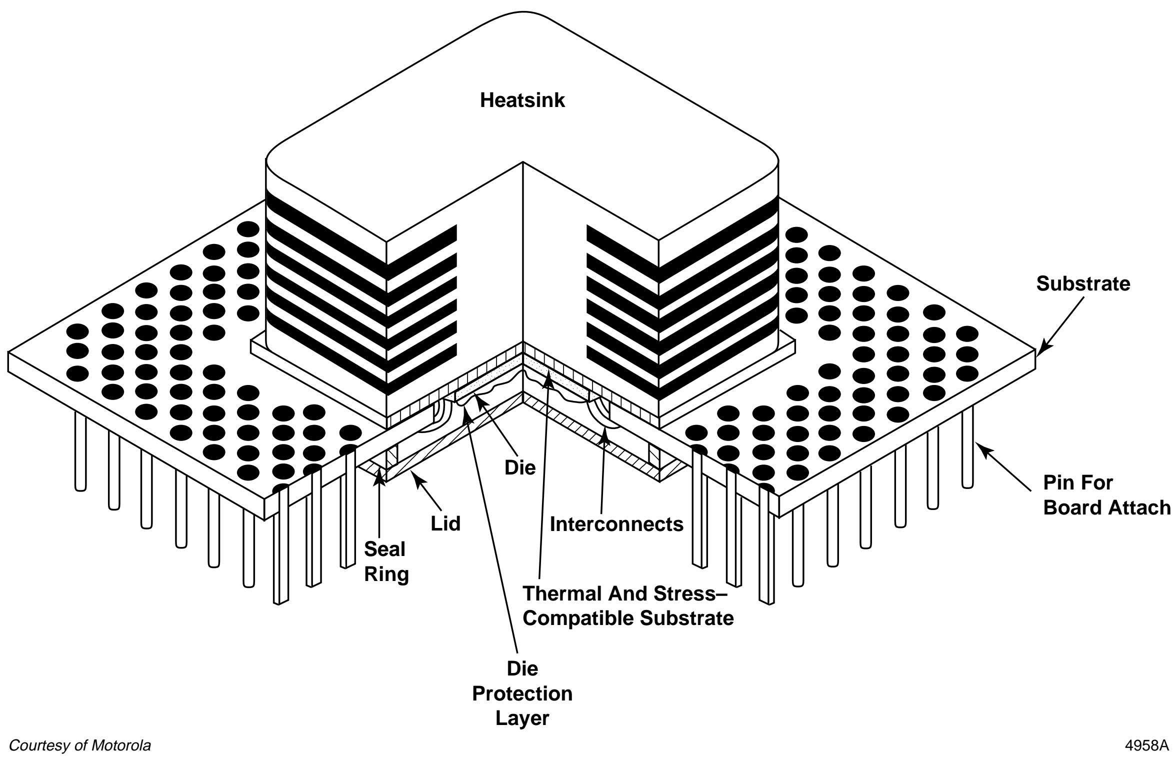


Figure 3-9. Motorola VLSI Package with Die Cavity Below and Finned Heat Sink Above

F. SURFACE MOUNT

1. SOIC, QSOP

The second problem — better use of board space — is solved through the use of surface mount packaging. A comparison of four surface mount packages and one DIP is shown in Figure 3-10. PCB technology improvements have allowed the package pin pitch to be reduced further as shown in the comparison between the Small Outline IC (SOIC) and the Quarter Size Small Outline Package (QSOP) in Figure 3-11.

2. LCC, PLCC, PQFP

Figure 3-12 shows a comparison between the Leadless Chip Carrier (LCC), the Plastic Leaded Chip Carrier (PLCC) and the SOIC. The PLCC and the SOIC use the gull wing lead configuration (sometimes called a Lap Joint). Figure 3-13 shows the most common lead configurations for PLCCs, as well as the advantages and disadvantages of each. Figure 3-14 shows the internal construction of the Plastic Quad Flat Pack (PQFP) with corner bumpers to protect the leads from being damaged.

Package Type	Description	Advantages	Disadvantages
Dual-in-Line	0.100in. Pin Centers 0.125in. Pin Length 0.160in. Body Thickness 0.300in. to 0.900in. Body Width	Capabilities Generally Exist Lowest Implementation Cost Minimum Engineering Effort Well-Established Reliability Database	Pin Count Limited to Less Than 64 I/O Lines Not Surface Mountable
SOIC (Small-Outline IC)	0.050in. Pin Centers 0.030in. Pin Length (Solderable) 0.098in. Body Thickness 0.155in and 0.300in. Body Width	Surface Mountable Lowest Material Cost Allows Magazine Handling Soldering/Rework (Versus Quad Flat Pack)	Significant Equipment Design and Tooling Handling and Test More Difficult Board Routing/Soldering/ Rework of 0.050in. Pin Centers Reliability Questions
Quad Flat Pack	0.050in. Pin Centers 0.030in. Pin Length 0.095in. Body Thickness Variable Body Width	Low Materials Cost Solder Joints Visible (Versus Chip Carrier)	Process and Test Modifications Needed Pin-Count Limitations Handling Difficult Board Routing More Complex Soldering/Rework of 0.050in. Centers Reliability Concerns
Chip Carrier	0.050in. Pin Centers 0.030in. and 0.060in. Standoff 0.100in. Body Thickness JEDEC-Compatible Sizes	High Pin Counts Possible Surface Mountable Less Stressed Than Quad Flat Pack	Development Time and Cost Board Routing/Rework More Difficult Solder-Connect Technology and Joint Reliability
Plastic Chip Carrier	0.050in. Pin Centers 0.100in. Pin Lengths 0.145in. Body Thickness JEDEC-Compatible Sizes	Surface Mountable Minimum Engineering Effort Low Materials Cost	Technology Compatible With Pin Counts Under 84 Leads Board Routing/Rework of 0.050in. Centers

Source: EDN 10036A

Figure 3-10. Package Type Comparisons

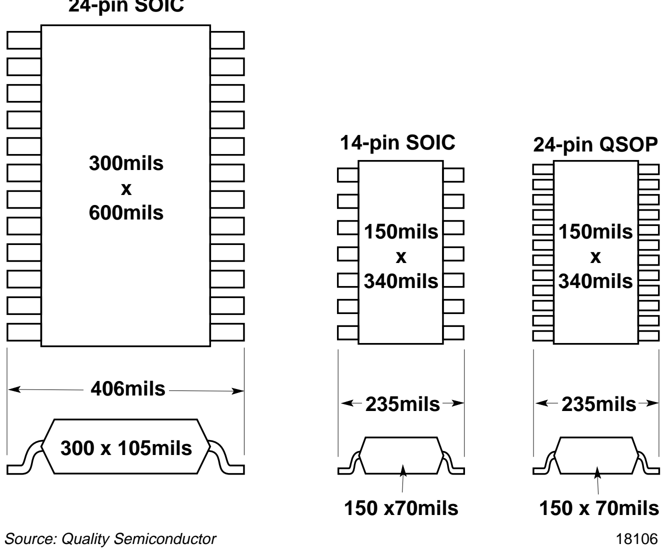


Figure 3-11. QSOP Versus SOIC Packaging

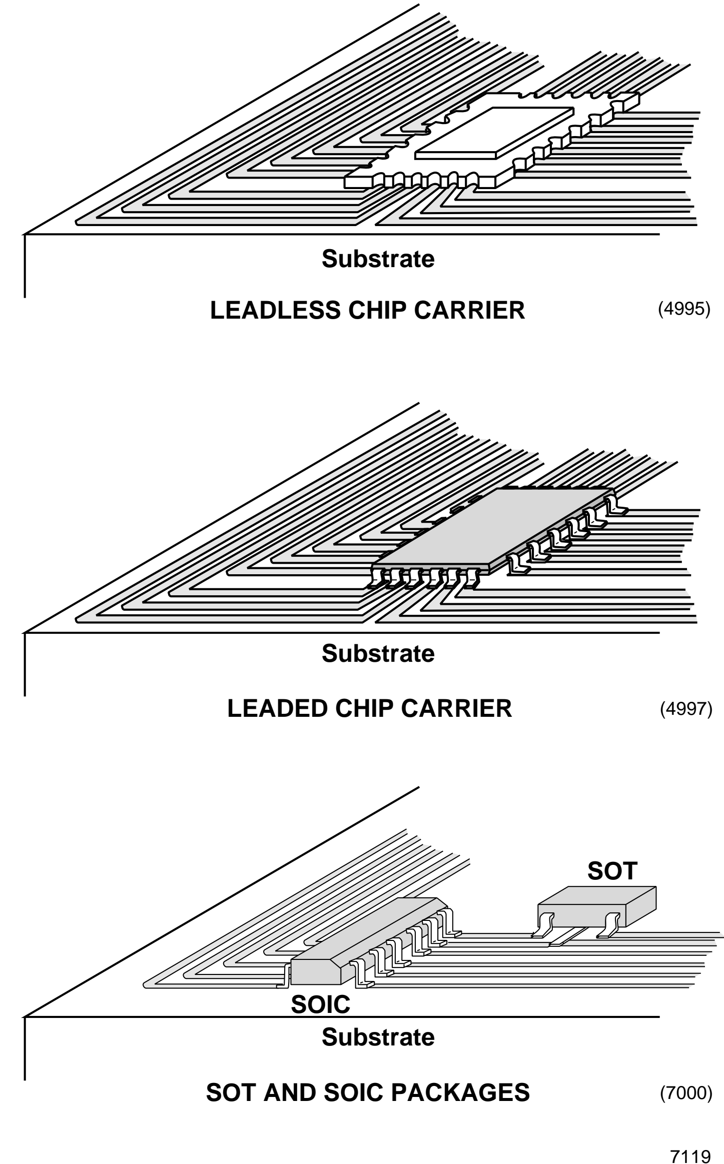


Figure 3-12. Surface-Mount IC Packages

3. Thermal Coefficient of Expansion

One technical compromise is present with all packaging schemes, but becomes very critical with surface mount — mismatch in thermal expansion coefficients of the various elements — the silicon die, the package materials, and the PCB materials. Figure 3-15 shows the expansion coefficients of some of the commonly used materials. As the table shows, most of the materials are inherently incompatible. Therefore, to make the packaging systems work reliably, flexible elements such as package leads are required.

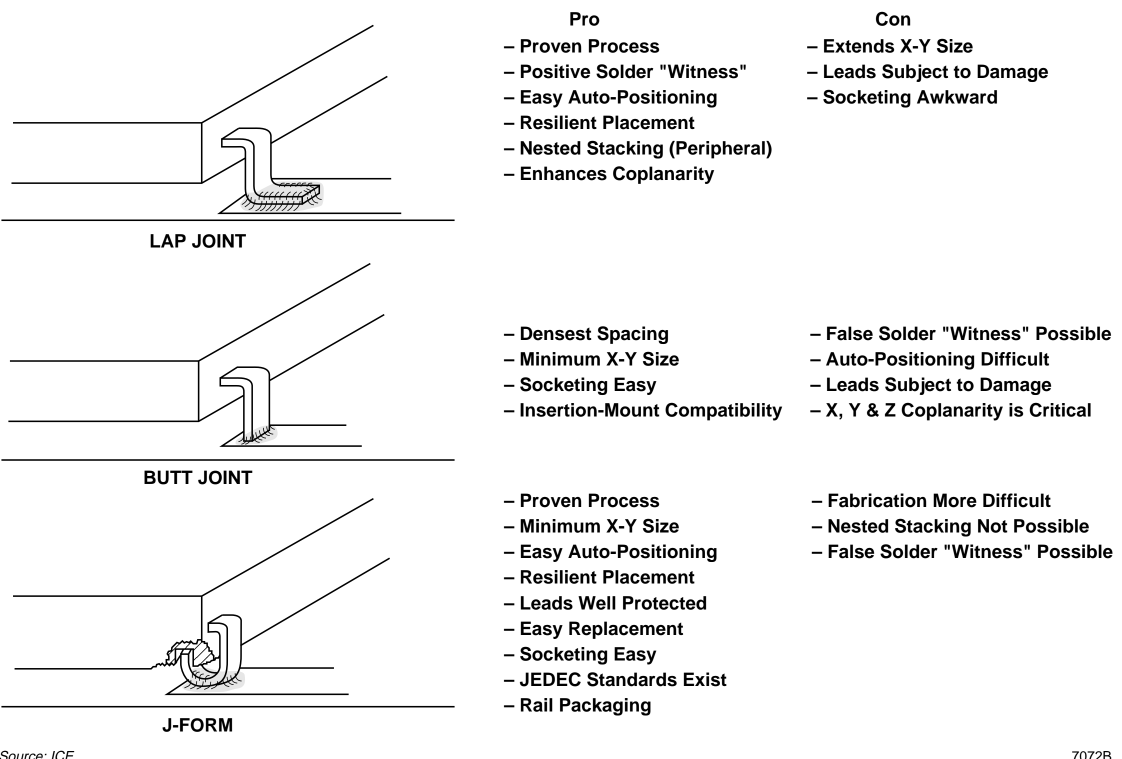


Figure 3-13. Surface Mount Leaded Connections

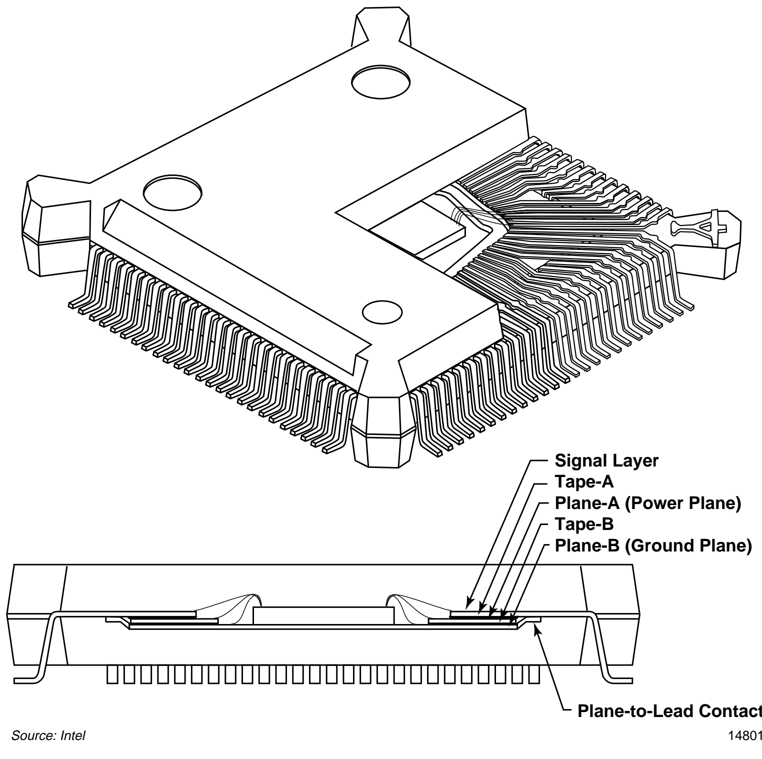


Figure 3-14. Top and Cross-Section Views of MM/PQFP Package

MATERIAL	DIELECTRIC CONSTANT	THERMAL EXPANSION COEFFICIENT (10^{-7}/°C)	THERMAL CONDUCTIVITY (W/m•°K)	APPROXIMATE PROCESS TEMPERATURE (°C)
NON-ORGANICS				
92% Alumina	9.2	60	18	1,500
96% Alumina	9.4	66	20	1,600
Si_3N_4	7	23	30	1,600
SiC	42	37	270	2,000
AlN	8.8	33	230	1,900
BeO	6.8	68	240	2,000
BN	6.5	37	600	>2,000
Diamond				
High Pressure	5.7	23	2,000	>2,000
Plasma CVD	3.5	23	400	≈1,000
Glass-Ceramics	4 – 8	30 – 50	5.0	1,000
Copper Clad Invar (10% Copper)/(Glass coated)	—	30	100	800
Glass Coated Steel	6	100	50	1,000
Silicon	11.7	0.3	1.57	1,420
ORGANICS				
Epoxy-Kevlar (x-y) (60%)	3.6	60	0.2	200
Polyimide-Quartz (x-axis)	4.0	118	0.35	200
Fr-4 (x-y plane)	4.7	158	0.2	175
Polyimide	3.5	500	0.2	350
Benzocyclobutene	2.6	350 – 600	0.2	240
Teflon®	2.2	200	0.1	400

Teflon is a trademark of Dupont Company

15087A

Figure 3-15. Properties of Package Insulator Materials

4. Flip Chip, Multi-Chip Modules (MCMs)

If flexible leads are not available, then the package material must be a close match to the substrate material. IBM has used the flip-chip (small solder balls on each bonding pad) approach for over thirty years. It has been successful for mounting the flip chips on ceramic substrates, as shown in Figure 3-16, for single-chip packages, as well as for Multi-Chip Modules (MCMs), as shown in Figure 3-17.

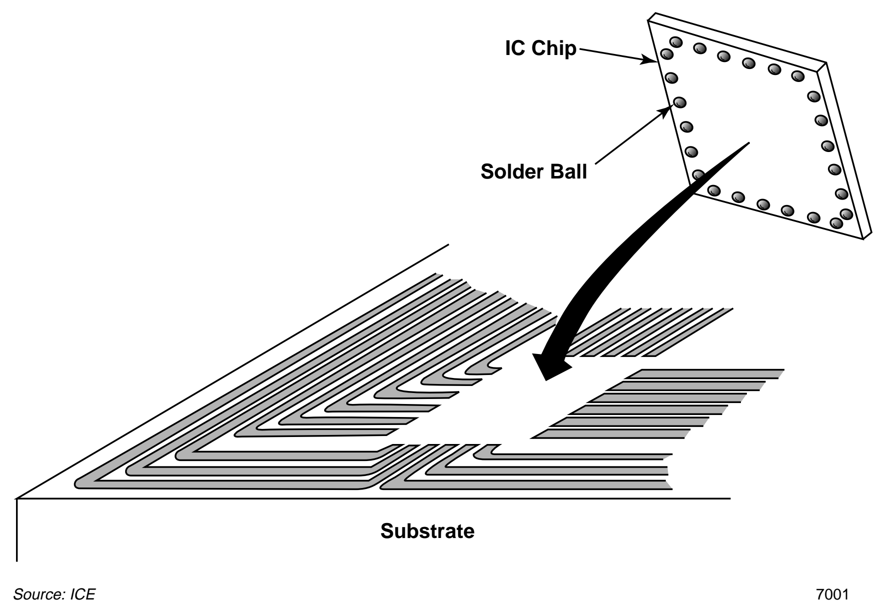


Figure 3-16. Flip-Chip Mounting

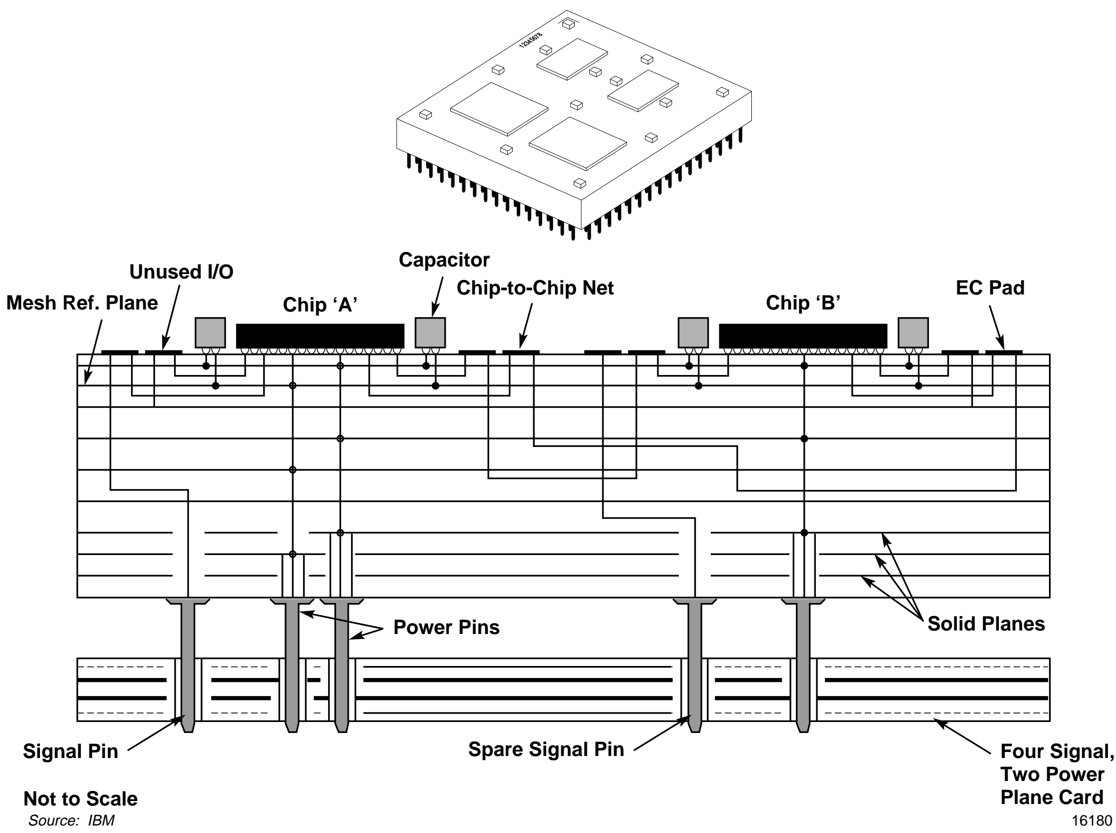


Figure 3-17. IBM MCM

G. TAPE AUTOMATED BONDING (TAB)

Another approach that allows flexibility as well as high pin count is the use of area Tape Automated Bonding (TAB). TAB refers to the use of thin copper foil laminated to a plastic film, then etched (the copper) to form a pattern to match the bond pads on the IC chip and the pattern on the substrate. Figure 3-18 shows the application of area TAB to replace wire bonds in a PGA, but this technique also allows mounting the IC chip directly on an external ceramic or PCB substrate.

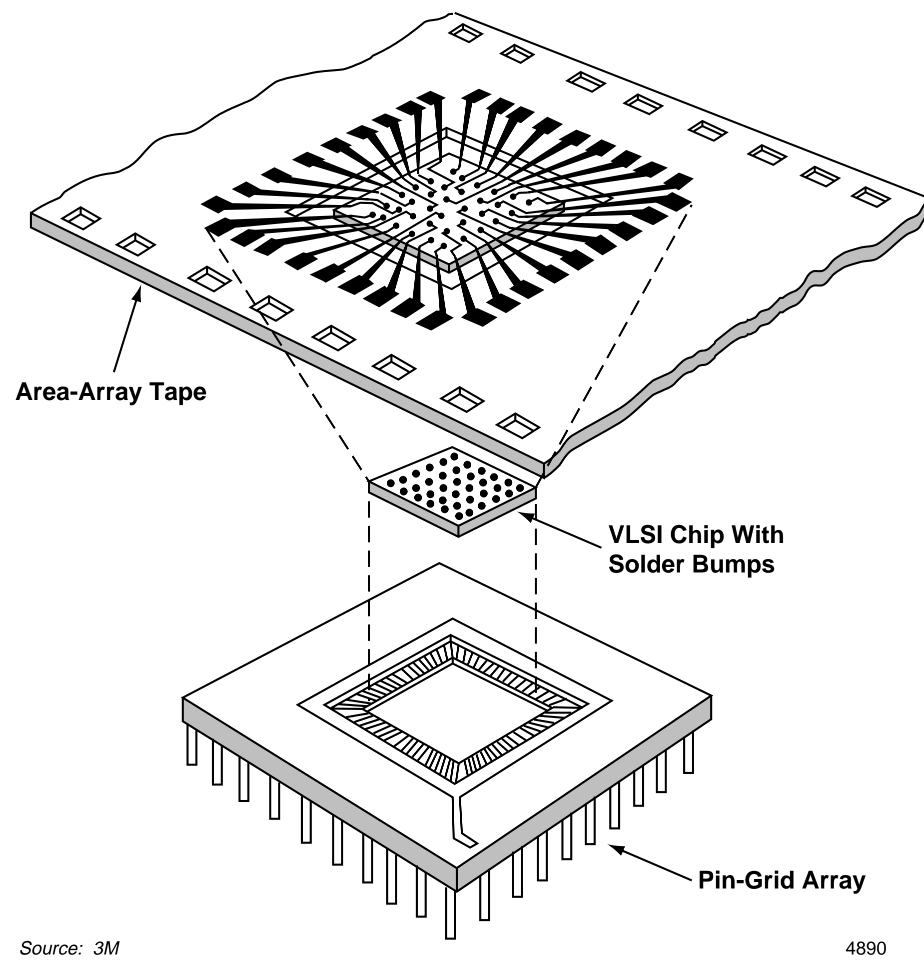


Figure 3-18. Area Array TAB Concept

H. CHIP-ON-BOARD (COB)

IC chips can be mounted directly on the substrate, without a package. Figure 3-19 shows this approach with standard bonding techniques to form a hybrid circuit or MCM and Figure 3-20 shows a Chip On Board (COB) used in an electronic game cartridge.

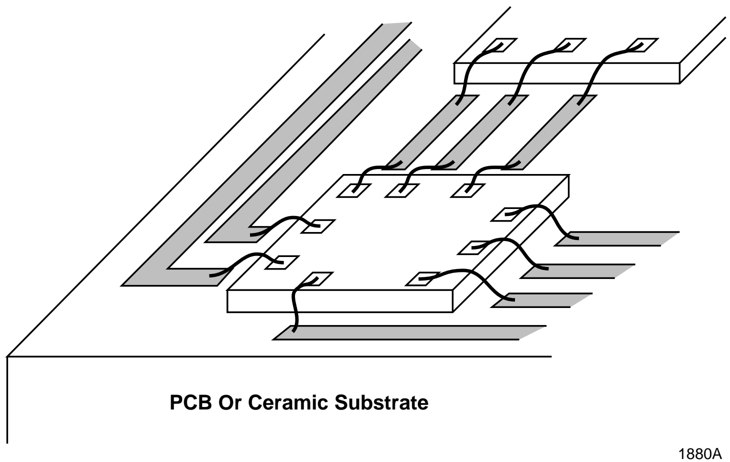


Figure 3-19. Hybrid Technologies Monolithic Chip-and-Wire

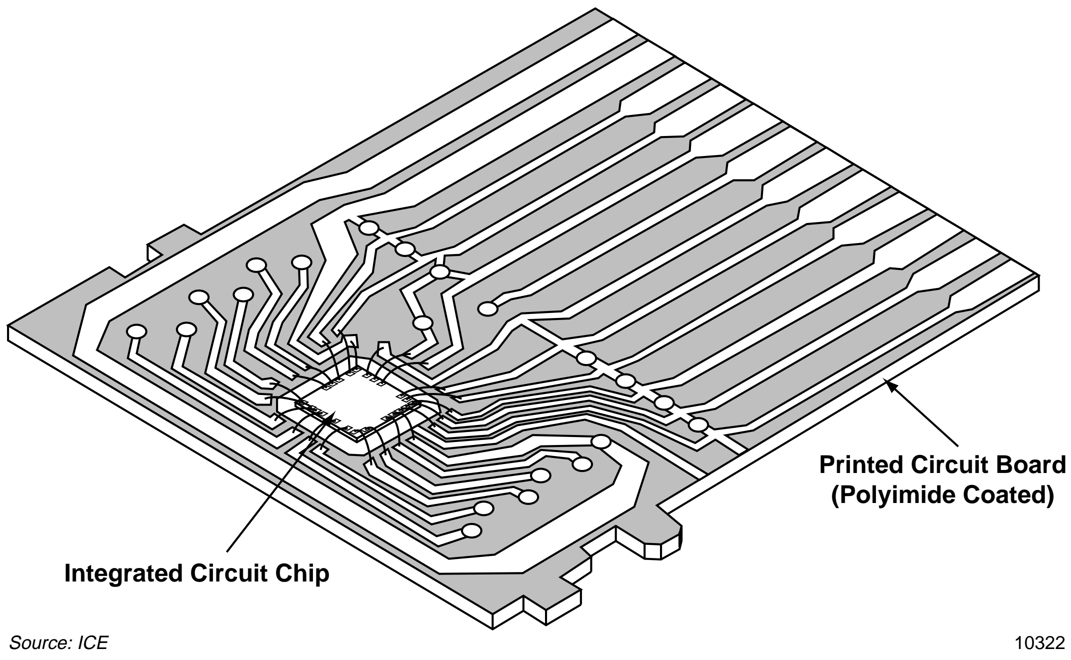


Figure 3-20. Chip-on-Board

I. SILICON SUBSTRATES

Another approach to reducing the thermal expansion problem is to construct MCMs on silicon substrates, then mounting the substrates onto ceramic or normal PCBs. This is shown in Figures 3-21 and 3-22.

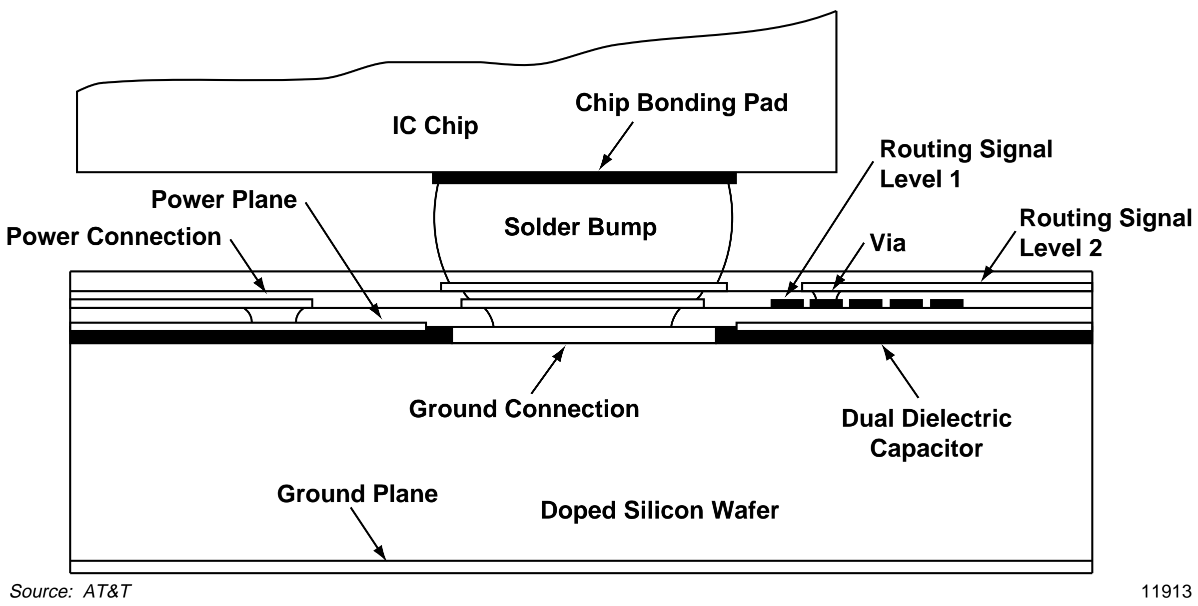


Figure 3-21. Interconnection Substrate and IC Chips

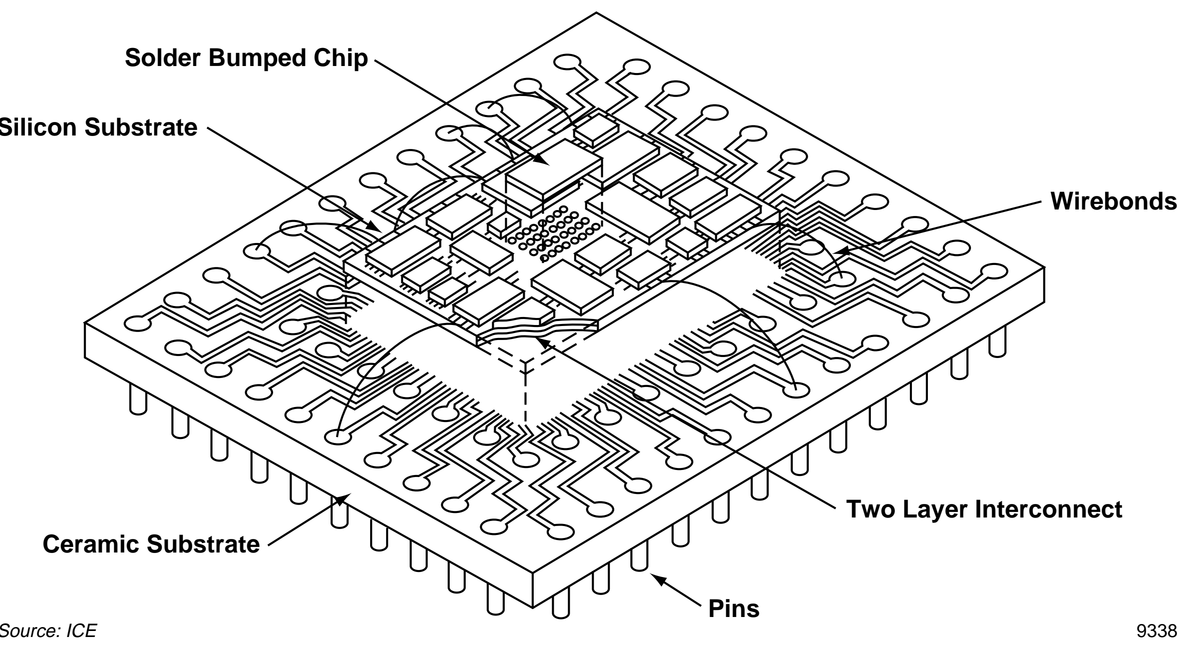


Figure 3-22. Silicon-on-Silicon Packaging Concept

J. BALL GRID ARRAY

Figure 3-23 shows a Ball Grid Array, which combines the high pin count available with the PGA with surface mount board assembly. In this technique the package is made of the same material as the substrate so the solder balls are sufficient to absorb the small thermal mismatch. In addition, the cost should be considerably lower than a standard PGA because the materials are less expensive. This package, or one very similar to it, will find wide use as a replacement for standard PGAs because of cost, size, and board density, as the ball grid can be made to finer pitch as the users become experienced with use of the package. If the pitch is reduced by a factor of two, the board area is reduced by a factor of four. A pitch of 20 mils is not unreasonable, compared to a pitch of 100 mils for the PGA. This is a theoretical size reduction of 25 times.

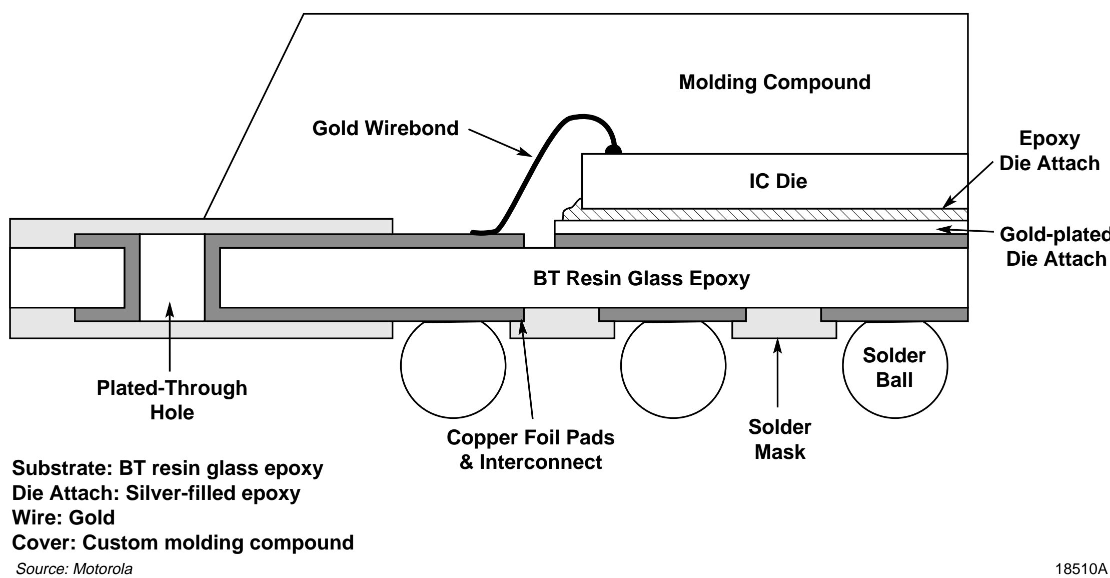


Figure 3-23. OMPAC Ball Grid Array From Motorola

K. SPECIAL PACKAGES

Special packaging is also important for high-volume ICs with special needs. An example of this is shown in Figure 3-24. The package is designed for memory chips where the die size is very large, the pin count is very low, and there are several chips used per system. The package is inexpensive, and its overall size is only slightly larger than the IC chip inside.

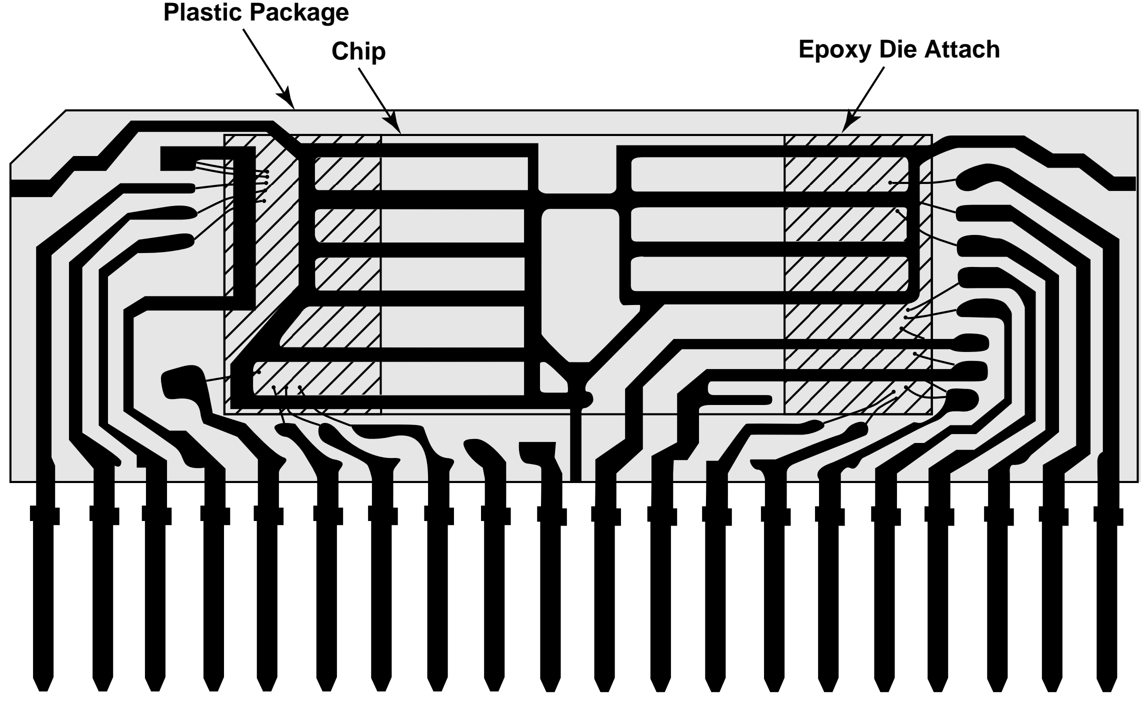


Figure 3-24. X-Ray of Hitachi 4M DRAM ZIP Package

The package in Figure 3-25 is constructed differently than most plastic devices. The IC chip itself is used as a base. The chip is covered with some type of coating and patterned to expose the bonding pads that run along the center. The leadframe is attached to the top of the IC chip and the bonding performed from the chip *up to* the leadframe. This package has the additional advantage of the ground and positive voltage supply terminals running almost the entire length of the chip.

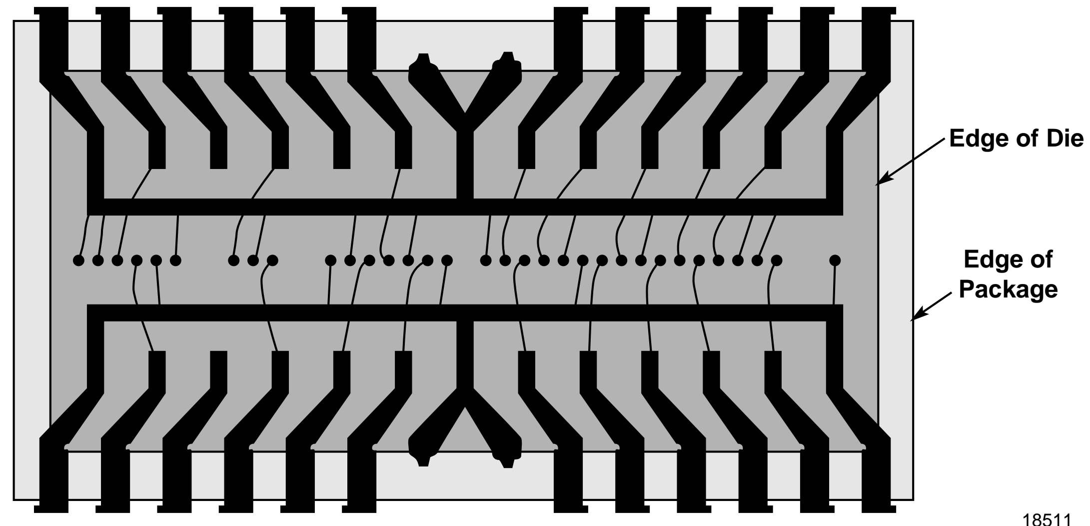


Figure 3-25. 16M DRAM