Source driver Solution for TFT Large Size Display

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INTRODUCTION

TFT LCD (Thin Film Transistor Liquid Crystal Display) is changing the way people look at their computers and TV. The features of low EMI make it, thin, light, space saving, brighter and better for the environment and so many people think that these flat panel display devices are the way forward into the future.

Solomon Systech Limited is one of the world's premier LCD driver suppliers and already has extensive experience and technology with display driver ICs, they have now developed TFT source drivers that match with the application of a large sized TFT LCD for a driving circuit unit. Featured with a high speed RSDS interface, accurate output voltage levels, a charge-sharing feature and TCP design, the source driver is able to exploit the important features of a TFT stable display panel, including good contrast, high frame frequency, a fast response speed and a large viewing angle.

A TFT LCD module consists of a TFT panel, a driving-circuit unit, a backlight system and an assembly unit as shown in Fig 1.

The features of the source driver IC and some information related to the TFT LCD module system will be discussed in this article.

TFT Source Driver Structure

The TFT source driver consists of the circuit blocks of Shifter Register, Data Latch, Level Shifter, Digital to Analog Converter, Output and Repair Buffer, as shown in Fig 2.

The following considerations as outlined below are needed for optimum performance from the source driver.

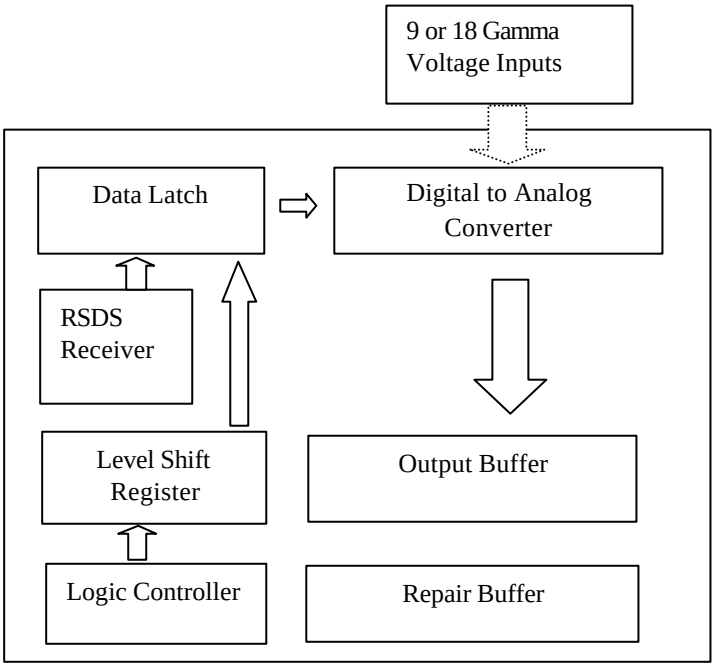

Fig.2 Functional Block diagram of a individual source driver

(1). The power consumption for dynamic mode and static mode under power safe.
(2). The driving capability of the output buffer. The loading per channel is around 50pF to 180pF depending on the size and resolution of the panel.
(3). The timing required for the output to get stable. This is to guarantee the voltage level hold at the source driver output is valid until the gate line is switched off. For example, the SXGA resolution has 1024 gate lines with 75Hz Frame Frequency. The scanning time for a gate line is 1/75/1024 =13us. Thus, the timing required for the output should be less than 13us.
(4). The maximum CLK frequency of the RSDS receiver.

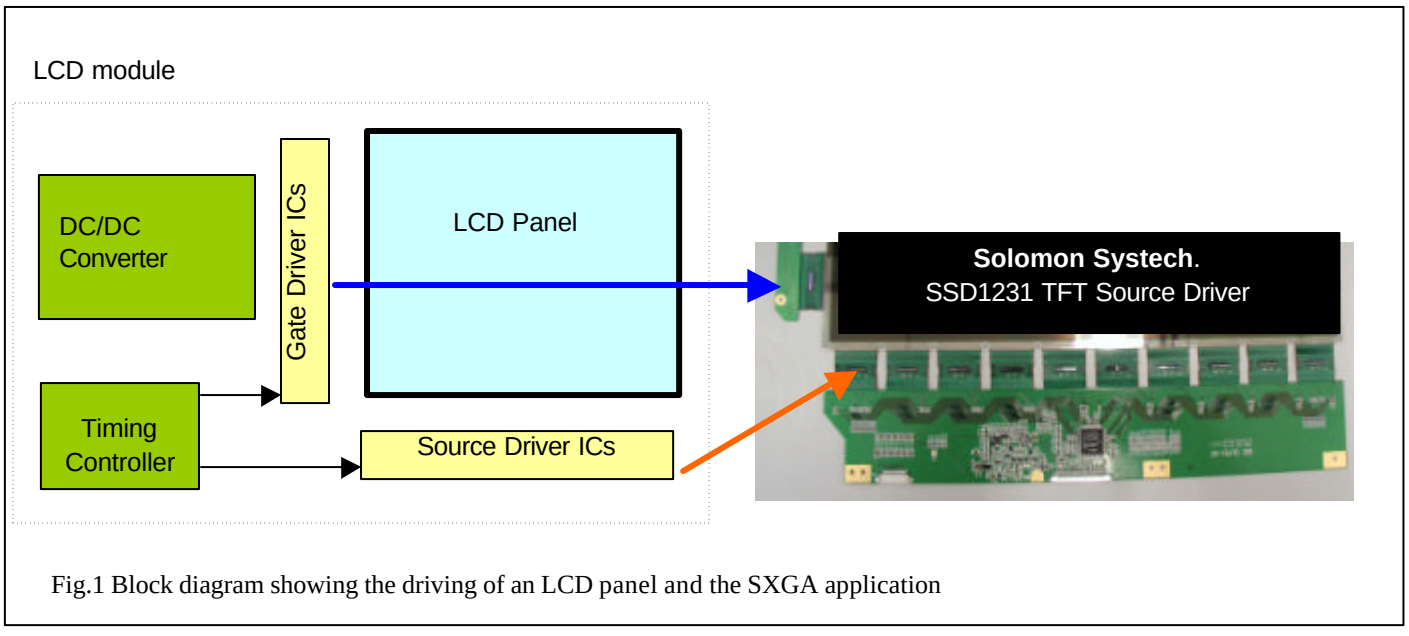

Fig.1 Block diagram showing the driving of an LCD panel and the SXGA application

This will directly affect the application resolution and the frame frequency allowed.
(5) The uniformity of the source driver outputs. The variation among the pins output voltage would affect the display quality.

SSD1211/13/31/33 series TFT source drivers adopt RSDS interface, charge sharing driving algorithm, internal 6bit DAC (for SSD1231/33), internal 8-bit DAC (for SSD1211/13), dot or N-lines inversion and support systems with SVGA, XGA, WXGA, SXGA, UXGA, QXGA for notebook PCs, monitors and LCD TV applications.

Fig 3 is an application example of 17" SXGA panel for PC monitor. The panel display is shown as below with 6-bit DAC accuracy by using SSD1231

Fig. 3a,b SXGA Panel output by using SSD1231 source driver

RSDS interface

Reduced Swing Differential Signaling (RSDS) interface is a type of differential signal protocol that is similar to LVDS (Low Voltage Differential Signal) except in their intended application. By using the RSDS interface, the system can benefit the connection between TCON (Timing Controller) and Source Drivers with higher speeds, reduced interconnect lower power and a lower EMI.

RSDS uses a low voltage differential swing (+/- 200 mV) and a 2:1 Data Mux ratio, resulting in a less complex and lower power consumption receiver structure.
The source drivers can be operated at as high as an 85MHz clock rate with an RSDS interface. Besides its low voltage swing as compared to a TTL interface, the architecture of differential signal pairs will also suppress the EMI generated from the high-speed signal paths.

Color bit mapping is shown in fig 4 below. It supports both a 6-bit and an 8-bit source driver. For a 6-bit interface, the MSB of the data bus signal can be omitted.

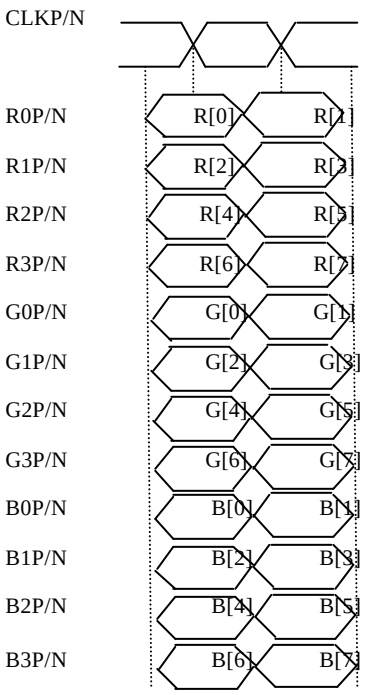

Fig. 4 RSDS Color Bit Mapping

As the RSDS interface transmits data in serial mode with a dual edge signal trigger, the overall bus width only contains 9 pairs of data signals and 1 pair of clock signals, for a total of 20 wires in a 6-bit application. For a traditional 6bit TTL interface, 36 data lines with 2 clock signals are required. For the system with an RSDS interface, a total reduction of a 47.4% bus width can be achieved in the TFT-LCD module.

Charge sharing output driving

As the size of application becomes larger the panel loading will be increased accordingly, the dynamic power consumption will also be increased significantly. This will affect the power budget of the system. Due to this requirement and for the application of a handheld notebook, the charge sharing output driving algorithm is adopted in the Solomon Systech's source drivers in order to reduce power consumption.

As the panel would use the dot or N-Line inversion, the source driver output should have half above the VCOM and half below the VCOM voltage level. Charge sharing works by redistributing the charge stored on the source driver output which can then save half of the dynamic current consumed.

When charge sharing is adopted the output waveform is different from the traditional one. The figures below illustrate this difference. For the output with charge sharing, there is a segment of period maintaining near the VCOM voltage for charge redistribution among all the output pins. After that, the waveform will return to the traditional driving waveform.

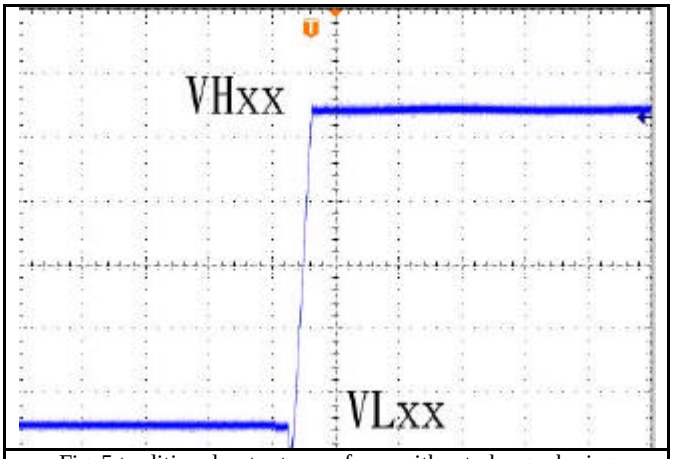

Fig. 5 traditional output waveform without charge sharing

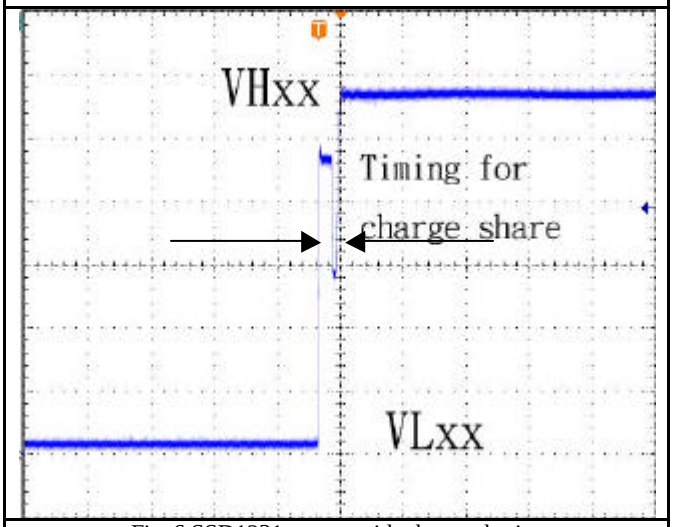

Fig. 6 SSD1231 output with charge sharing

Different from other traditional power saving techniques, charge sharing will not degrade the driving capability of the source driver. It is because the charge sharing is only reused the energy stored in the outputs only while the bias current to the output buffer will be kept the same. Moreover, the timing of the charge sharing is controlled by the horizontal line latch pulse. No extra hardware is required to take care of this. Thus, Solomon Systech's source drivers could have a higher driving capability as well as a lower power consumption.

IC PACKAGE DESIGN

Depending on the application, maximum 9+9 for external gamma input in the TAB package is possible. The SSD1231T TAB provides 5+5 input for simplicity of design and convenience of interconnection. Please refer to figure 7 and figure 8 for detailed TAB drawing and pin assignment.

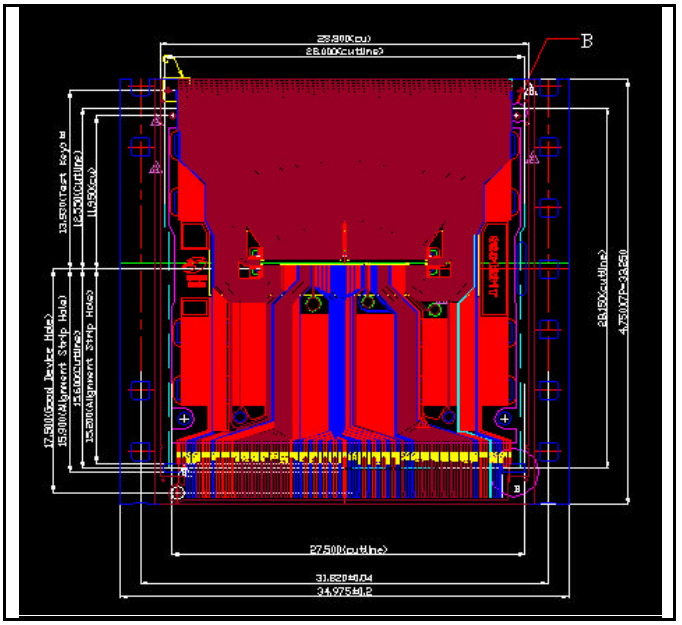

Fig. 7 SSD1231T TAB Package Design

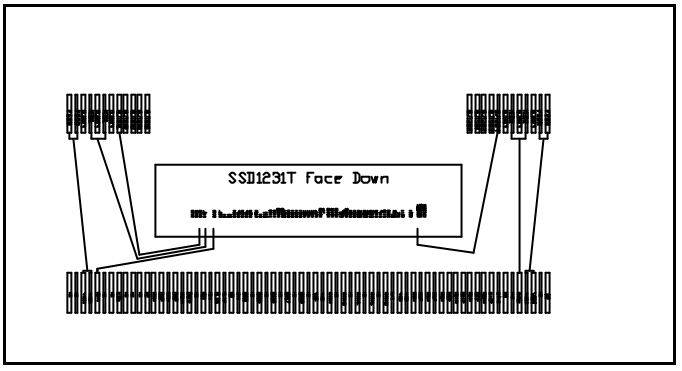

Fig. 8 SSD1231T TAB Layout

The SSD1231T provides 2 test points of source output for easier checking in the production stage and there is a pair of dummy buffers for signal repair in case of any vertical line discontinuity on the panel.

CONCLUSION

The trends of the TFT LCD monitor and TV will go towards a higher resolution, quality and a physically larger panel size. A newly developed series of source drivers from Solomon Systech can accomplish these different applications.

Meanwhile, Solomon Systech is developing a set of source and gate drivers for COG application that will further reduce the physical size and the weight of the TFT-module. Importantly, it will also reduce the materials cost on the monitor / TV system by saving the TAB/COF and PCBs materials.

APPENDIX – Features of TFT source driver series IC

Features	SSD1211	SSD1213	SSD1231	SSD1233
Output channel	384	480	384	480
Display color	8-bit	8-bit	6-bit	6-bit
Logic voltage	2.7-3.6V	2.7-3.6V	2.7-3.6V	2.7-3.6V
HV driving voltage	9.0V to 16V	9V to +16.0V	8V to 12V	8V to 12V
Supported resolution	QVGA,SXGA,UXGA	QVGA,SXGA,UXGA	XGA,QVGA,SXGA	XGA,QVGA,SXGA
Max Clk speed	85MHz	85MHz	85MHz	85Hz
Gamma correction	9+9 input	9+9 input	9+9 input	9+9 input
TCON interface	RSDS	RSDS	RSDS	RSDS
Package	TCP/COF	TCP/COF	TCP/COF	TCP/COF