100 dpi 4-a-Si:H TFTs Active-Matrix Organic Polymer Light-Emitting Display

Yongtaek Hong, *Student Member, IEEE*, Jeong-Yeop Nahm, and Jerzy Kanicki, *Senior Member, IEEE*

***Abstract*—In this paper, we report on 100 dpi four hydrogenated amorphous silicon thin-film transistors (4-a-Si:H TFTs) active-matrix organic polymer light-emitting display (AM-PLED). For this display, we have established the operational limitation of our 4-a-Si:H TFTs pixel electrode circuit by performing *a* load line analysis. Combining this result with the extracted pixel organic polymer light-emitting device (PLED) characteristics, we have found that the change of the AM-PLED pixel operating point, especially of a driving TFT, limits the operational range of AM-PLED pixel. The predicted results are compared with the measured data of 100 dpi monochromatic red light-emitting 4-a-Si:H TFTs AM-PLED. For our AM-PLED, we obtained luminance up to ~ 20 cd/m^2 and Commission Internationale de l'Eclairage color coordinates of (0.67, 0.33), which are calculated from the measured AM-PLED electroluminescence spectrum.**

***Index Terms*—Active-matrix display, amorphous silicon thin-film transistor, current bias-temperature-stress, organic polymer light-emitting devices.**

I. Introduction

ORGANIC light-emitting devices (OLEDs) are being considered as the next-generation flat panel display (FPD) technology for portable display applications. Especially, active-matrix organic light-emitting displays (AM-OLEDs) have attracted considerable attention in possible high-image quality applications, such as laptop and TV displays. Since the OLED brightness directly relates to the current flow through the device, achieving a constant current flow through the OLED is critical to control the AM-OLED brightness uniformity, which can be affected by variations in thin-film transistors (TFTs) threshold voltage and OLEDs turn-on voltage [1]. Therefore, to compensate for the device parameter variations and to provide constant current flow through the OLED, several current-driven AM-OLED pixel configurations have been proposed. Dawson *et al.* [2] suggested a current programmed OLED pixel with four poly-silicon (poly-Si) p-type TFTs, which is limited by charging time at low data currents in high-resolution display applications. To solve this problem, Sony Corporation [3] reported the current-mirror-type pixel electrode circuit with two n-type and two p-type poly-Si TFTs. By increasing the charging current levels with scaled back-to-back current-mirror TFTs, they reduced charging time for low data current levels. In addition, they introduced top-emission OLED structure in their 13 inch SVGA AM-OLED. Another current-mirror type pixel electrode circuit with two n-type and one p-type poly-Si TFTs was reported by Philips Research Laboratories [4]. They used a current-sink-type pixel address method and introduced a pulsed cathode approach to achieve efficient OLED operation, higher charging currents, and improved motion portrayal. We reported current-sink top-cathode and current-source top-anode pixel electrode circuits based on four poly-Si TFTs [5]. By separating the charging and operation current paths, the precharged pixel effect can be removed and the duty ratio of data current can be adjusted for high quality motion images.

As an alternative and competing technology to the poly-Si-based AM-OLED, since 1999 our laboratory has focused on AM-OLED based on hydrogenated amorphous silicon (a-Si:H) TFTs. Initially, we adopted current-source AM-driving schemes based on four a-Si:H TFTs (4-a-Si:H TFTs) and one selection line [6]. This approach had several limitations such as OLED data current saturation and leakage current flow through the OLED at low data current levels. Later, we developed modified a-Si:H TFTs pixel electrode circuits with two selection lines, which effectively addressed these limitations [7]. Pixel electrode circuit simulation and experimental data confirmed that the improved 4-a-Si:H TFTs pixel electrode circuit can fully compensate for TFT threshold voltage shift, consequently providing a constant current flow through the OLEDs [8].

In this paper, we report on 100 dpi monochromatic red light-emitting active-matrix organic polymer light-emitting display (AM-PLED) based on 4-a-Si:H TFTs pixel electrode circuit. The AM-PLED pixel operations are described in Section II. Pixel electrode circuit simulation used for the engineering prototype development is briefly described in Section III. Details of the pixel electrode circuit fabrication are discussed in Section IV. The DC electrical and current bias-temperature-stress characteristics of the fabricated TFTs are described in Section V. Measurement results of the pixel electrode circuit are discussed in Section VI. Analysis of the AM-PLED pixel characteristics is performed in Section VII. Finally, optoelectronic characteristics of the AM-PLED are described in Section VIII.

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Y. Hong is with the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48105 USA.

J.-Y. Nahm was with the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48105 USA. He is now with Cypress Semiconductor, San Jose, CA 95134 USA.

J. Kanicki is with the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48105 USA and also with the Center for Polymers and Organic Solids, University of California, Santa Barbara, CA 93106 USA (e-mail: kanicki@eecs.umich.edu).

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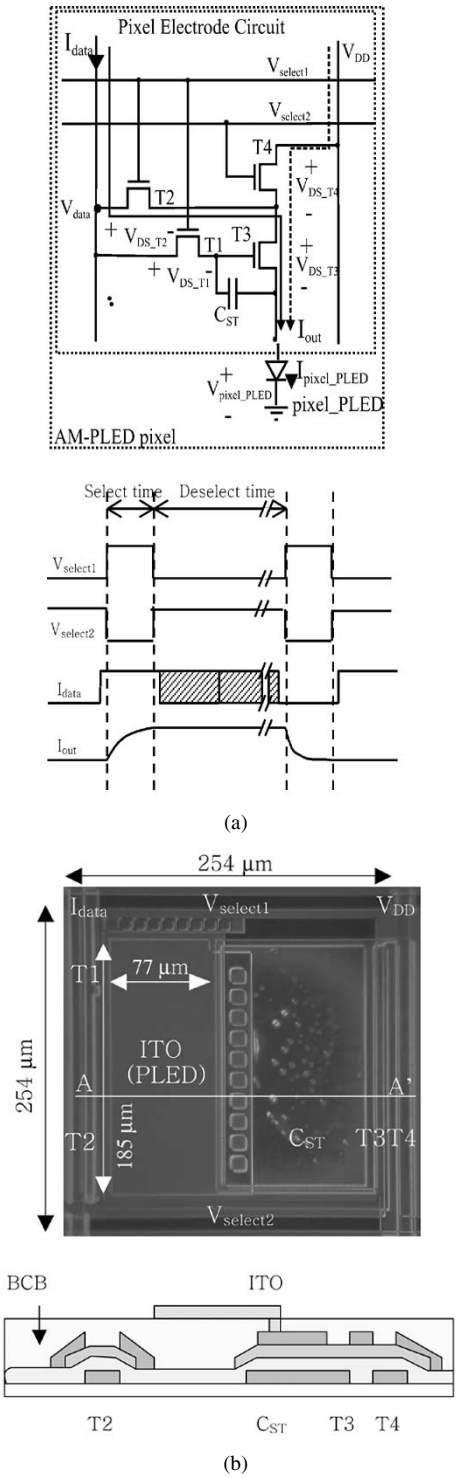

Fig. 1. A 4-a-Si:H TFTs pixel electrode circuit. (a) Schematic circuit configuration and signal waveforms. (b) Top and cross section views of pixel electrode circuit are shown.

II. AM-PLED Pixel Operation

A schematic diagram of 4-a-Si:H TFTs pixel electrode circuit and the signal waveforms are shown in Fig. 1(a). The organic polymer light-emitting device (PLED) diode symbol is also included in Fig. 1(a) to show the PLED connection with the pixel electrode circuit, which is denoted as pixel_PLED. The anode and cathode of pixel_PLED are connected to the source of T3 and ground, respectively, to complete each pixel circuit of the AM-PLED. This is called AM-PLED pixel in this paper to differentiate it from the pixel electrode circuit. In active-matrix displays, all the pixels in each row are selected at a time during a certain period of the frame time (select time), while they are deselected when the pixels in other rows are selected during the rest of the frame time (deselect time). In our AM-PLED pixel, two control signals ($V_{\rm select1}$ and $V_{\rm select2}$) with opposite polarity define the select and deselect time [Fig. 1(a)] and also determine the current flow path to the driving TFT T3 and pixel_PLED by turning on and off the switching TFTs, T1/T2 and T4, respectively. It is also noted that current $(I_{\rm data})$ is applied to the AM-PLED pixel as a data signal during select time, whose value varies according to the display gray-scale levels. Details of operation principle during select and deselect time are separately described in the following sections II-A and B.

A. Select Time Operation

During select time ($V_{\rm select1}$ is high, $V_{\rm select2}$ is low), T1 and T2 are ON, and T4 is OFF [Fig. 1(a)]. The data current flows from the data line $(I_{\rm data})$ to pixel_PLED through T2 and T3 [solid line in Fig. 1(a)], triggering pixel_PLED light-emission and commencing charging of the storage capacitor $(C_{\rm ST})$. The $C_{\rm ST}$ charging process continues until $V_{\rm GS\_T3}$ and $V_{\rm DS\_T3}$ reach specific values that correspond to $I_{\rm DS\_T3}(= I_{\rm data} = I_{\rm out} = I_{\rm pixel\_PLED})$. It is noted that $V_{\rm GS\_T3}$ and $V_{\rm DS\_T3}$ can change from pixel to pixel if there is variation in the pixel_PLED and TFTs threshold voltages, and TFTs mobility for each pixel because $I_{\rm data}$ determines these voltages during select time. These device parameter variations can be caused by the manufacturing and material variations, and AM-PLED pixel aging. When the charging process ends, a specific $V_{\rm GS\_T3}$ value is stored in $C_{\rm ST}$. The charging process should be completed during select time for all $I_{\rm data}$ gray-scale levels. The charged $V_{\rm GS\_T3}$ value is maintained and pixel_PLED continuously emits light until select time ends. In addition, the gate potential of T3 equals the potential $(V_{\rm data})$ of the $I_{\rm data}$ line, i.e., $V_{\rm DS\_T1}$ is negligible, after the charging time, while $V_{\rm DS\_T2}$ is not negligible due to the continuous $I_{\rm data}$ flow through T2 during select time; the $V_{\rm DS\_T2}$ directly depends on $I_{\rm data}$. The AM-PLED pixel configuration and driving conditions, however, do impose the requirement on $V_{\rm DS\_T2}$ that, during select time, T1, T2, and T3 operate in linear, from linear to on set of saturation, and saturation regime, respectively. To ensure that T3 operates in the saturation regime, $V_{\rm DS\_T2}$ should be smaller than $V_{\rm th\_T3}$ for all $I_{\rm data}$ gray-scale levels during select time ($V_{\rm GS\_T3} - V_{\rm th\_T3} \leq V_{\rm DS\_T3} \rightarrow V_{\rm GD\_T3} \leq V_{\rm th\_T3}$, $V_{\rm GD\_T3} = V_{\rm DS\_T2}$). Therefore, the $I_{\rm data}$ value that corresponds to $V_{\rm DS\_T2} = V_{\rm th\_T3}$ will be the $I_{\rm data}$ operational limit that can be applied to our AM-PLED pixel during select time for normal display operation condition.

B. Deselect Time Operation

During deselect time ($V_{\rm select1}$ is low, $V_{\rm select2}$ is high), T1 and T2 are OFF, and T4 is ON. $V_{\rm DD}$ provides current flow to T3 and pixel_PLED through T4. The AM-PLED pixel is designed for T3 to operate in the saturation regime during deselect time. In addition, $V_{\rm GS\_T3}$ does not change assuming that charge variation in $C_{\rm ST}$ is negligible during deselect time. Therefore, for the same $V_{\rm GS\_T3}$ value, $I_{\rm DS\_T3}(= I_{\rm out} = I_{\rm pixel\_PLED})$ will be very close to $I_{\rm data}$, resulting in continuous pixel_PLED

light-emission that corresponds to $I_{\rm data}$. It is noted that, during deselect time, the $V_{\rm DS\_T3}$ value is different from the $V_{\rm DS\_T3}$ established during select time due to the current flow path change during deselect time [dotted line in Fig. 1(a)]. Since the pixel_PLED luminance is proportional to $I_{\rm pixel\_PLED}$, the pixel_PLED luminance will remain unchanged during both select and deselect time. However, if the driving TFT, T3, shows nonideal characteristics in the saturation regime, $I_{\rm pixel\_PLED}$ will be affected by $V_{\rm DS\_T3}$ variation during deselect time, leading to variable pixel_PLED luminance. Additionally, if there is significant leakage current through T1 during deselect time, $I_{\rm pixel\_PLED}$ is affected by the change of the stored charge in $C_{\rm ST}$, resulting in inconsistent pixel_PLED luminance.

As $I_{\rm data}$ increases, the operating point of T3 will move into the linear regime for a given $V_{\rm DD}$ value, leading to $I_{\rm pixel\_PLED}$ deviation from $I_{\rm data}$ and decrease of pixel_PLED luminance during deselect time. Therefore, in addition to the $I_{\rm data}$ operational limit established from select time operation, we can also obtain the $I_{\rm data}$ operational limit that makes T3 operate in the saturation regime ($V_{\rm GS\_T3} - V_{\rm th\_T3} \leq V_{\rm DS\_T3}$) during deselect time. The pixel electrode circuit parameters must be carefully designed to achieve large $I_{\rm data}$ operational limits.

In our initial pixel electrode circuit with one $V_{\rm select}$ line, a diode-connected TFT was used for T4 [6]. In addition, for the AM-PLED pixel simulation, we unintentionally selected the simulation conditions for T4 to operate in deep saturation regime ($V_{\rm DS\_T4} = V_{\rm GS\_T4}$) [7]. Both publications may mislead readers to understand that our AM-PLED is designed for T4 to operate in saturation regime [9]. However, T4 should operate in linear to onset of saturation ($V_{\rm DS\_T4} \leq V_{\rm GS\_T4} - V_{\rm th\_T4}$) regime to obtain a small voltage drop across T4 for a given $I_{\rm data}$. This allows T3 to operate in saturation regime with a large operational range of $V_{\rm DS\_T3}$ for a given $V_{\rm DD}$ value.

III. Pixel Electrode Circuit Simulation

Cadence SPECTRE was initially used to simulate the pixel electrode circuit. The a-Si:H TFT model used in the simulation was previously developed within our group [10]. In the initial simulation, the following parameters were used: TFT mobility (μ) = 0.49 cm^2/Vs in linear region, TFT threshold voltage ($V_{\rm th}$) = 2.55 V, $V_{\rm select1}({\rm high}) = V_{\rm select2}({\rm high}) = 30$ V, $V_{\rm select1}({\rm low}) = V_{\rm select2}({\rm low}) = 0$ V, $V_{\rm DD} = 30$ V, $C_{\rm ST} = 5$ pF, $C_{\rm oled} = 1.5$ pF, TFT parasitic capacitance model parameter: $C_{\rm gso}$(gate-to-source) = $C_{\rm dso}$ (gate-to-drain) = 5 nF/m. Based on the simulation result [8], we designed an engineering prototype AM-PLED with a resolution of 100 dpi (50×50 arrays) that is described in this paper. It is noted that the $V_{\rm th}$ and μ values used in the initial design are different from the experimental data since an improved a-Si TFT process was used to fabricate the AM-PLED.

IV. Pixel Electrode Circuit Fabrication

Fabrication of 100 dpi (50×50 pixels in 0.5×0.5 in^2 display) 4-a-Si:H TFTs pixel electrode circuit consists of six mask process steps. Chromium (Cr, 2000 Å) layer was deposited on the Corning 1737 glass substrates by a DC sputtering method. The Cr gates and selection lines were then patterned by wet-etching (*Mask* #1). Following gate line definition, hydrogenated amorphous silicon nitride (a-SiNx:H) (3000 Å)/a-Si:H (1000 Å)/p-doped a-Si:H (n+ a-Si:H) (300 Å) trilayer was deposited by plasma-enhanced chemical vapor deposition (PECVD) method. Using reactive ion etching (RIE) with a gas mixture of O_2 and CCl_2F_2, we defined the device active islands (*Mask* #2). The gate via was then patterned through the a-SiNx:H layer by wet-etching in buffered hydrofluoric acid (BHF) (*Mask* #3). After the gate via formation, a molybdenum (Mo, 2000 Å) layer was deposited by a DC sputtering method and source/drain (S/D) electrodes and $I_{\rm data}/V_{\rm DD}$ lines were patterned by wet-etching (*Mask* #4). Using S/D metal and photo resist as masks, we performed back-channel-etching by RIE with a gas mixture of O_2 and CCl_2F_2. To reduce the S/D contact resistance via $MoSi_2$ formation, the fabricated circuit was annealed for two hours at 230 °C in nitrogen. We then spun-coated benzocyclobutene (BCB, 1–2 μm) on top of the fabricated pixel electrode circuit to provide a planarized, flat surface for the following indium tin oxide (ITO) and PLED layers. After the BCB layer was coated, the pixel electrode circuit was cured at carefully controlled temperature steps in nitrogen. To make a contact for the ITO layer, via was formed through the cured BCB planarization layer by using RIE with a gas mixture of O_2 and CF_4 (*Mask* #5). After via definition, *in-situ* argon (Ar) back-sputtering was performed on the BCB layer surface to improve the adhesion between ITO and BCB layer. ITO (1000 Å) was deposited by a DC sputtering method and then, PLED ITO anode electrodes are patterned by wet-etching in a solution of nitric acid (HNO_3), hydrochloric acid (HCl), and deionized water (*Mask* #6). The size (W/L) of each TFT is 50/6 μm, 143/6 μm, 172/6 μm, and 189/6 μm for T1, T2, T3, and T4, respectively. The size of the storage capacitor is 100×172 μm^2, which corresponds to about 3.5 pF. The top view and cross section of the fabricated pixel electrode circuit are shown in Fig. 1(b). The aperture ratio (AR) of the pixel is $\sim$22%, which is defined as the ratio of the light-emitting pixel_PLED area (77×185 μm^2) to the whole pixel area (254×254 μm^2).

V. Characteristics of Fabricated a-Si:H TFTs

Fig. 2(a) shows the measured transfer characteristics of the fabricated TFTs with different sizes. We obtained a threshold voltage ($V_{\rm th}$) of 10–11 V, a field-effect mobility (μ) of 0.2–0.3 cm^2/Vs, a subthreshold swing slope of 0.8 dec/V, and a current on/off ratio of larger than 10^6 for $V_{\rm GS}$ from -10 to 30 V. We also performed the current bias-temperature-stress (C-BTS) of the fabricated TFT ($W/L = 60/6$ μm) for different current levels at room temperature (RT) and 80 °C. During C-BTS, the drain and gate electrodes of the TFT were electrically connected (TFT operated in a deep saturation regime) and a constant stress current was applied to the drain electrode. At several selected stress times, the stress was interrupted and $I_{\rm DS} - V_{\rm GS}$ characteristics in saturation regime were immediately measured at a given stress temperature. Fig. 2(b) shows an example of the $I_{\rm DS} - V_{\rm GS}$ characteristics measured during C-BTS at 80 °C. The TFT threshold voltage was then extracted by fitting the experimental $\sqrt{I_{\rm DS}} - V_{\rm GS}$ characteristics to the following relation, using the MOSFET gradual channel

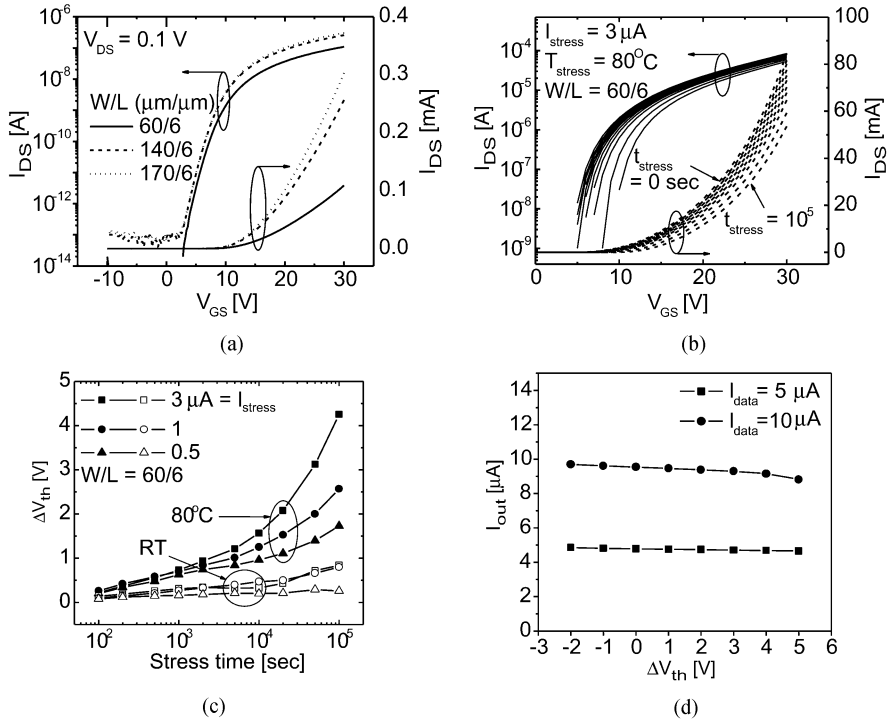

Fig. 2. Measured characteristics of fabricated a-Si:H TFTs. (a) Transfer characteristics at $V_{\rm DS} = 0.1$ V for TFTs with different channel width. (b) Example of $I_{\rm DS} - V_{\rm GS}$ characteristics for current bias-temperature-stress (C-BTS) measurements. (c) Extracted $\Delta V_{\rm th}$ versus stress time at RT and 80 °C. (d) Cadence SPECTRE simulation of pixel electrode circuit for threshold voltage shift of a-Si:H TFTs are shown.

approximation in saturation regime: $I_{\rm DS} \sim (V_{\rm GS} - V_{\rm th})^2$. Fig. 2(c) shows the TFT threshold voltage shifts measured at RT and 80 °C for several stress currents of 0.5, 1, and 3 μA. At RT, the threshold voltage shift was less than 1 V for 3 μA stress current after 10^5 s stress time, while the threshold voltage was shifted by as much as $\sim$5 V at 80 °C for the same C-BTS conditions. The change of the field-effect mobility of TFTs after C-BTS was within $\pm 5\%$ of the initial mobility for all C-BTS conditions. Therefore, based on this data, we can conclude that the threshold voltage shift of TFTs will have the most significant effect on the operation stability of the pixel electrode circuit. If we assume that the amount of the TFT threshold voltage shift in C-BTS is associated with the stress current per TFT gate width for TFTs with the same gate length, $\sim$5 V threshold voltage shift of the driving TFT ($W/L = 172/6$ μm) is expected for a stress current (or a continuous $I_{\rm data}$) of $\sim$9 μA. This stress current level corresponds to a continuous pixel illumination with $L_{\rm pixel} =\sim 45$ cd/m^2 for our red monochromatic AM-PLED, which is estimated from Fig. 5(c). Using Cadence SPECTRE simulation [8], we have shown that our pixel electrode circuit can compensate for the TFTs threshold voltage shift as large as 5 V as shown in Fig. 2(d). The simulation result shows that $I_{\rm out}$ decreases by $\sim$0.1 and $\sim$0.7 μA for $I_{\rm data} =$5 and 10 μA, respectively, which corresponds to $\sim$2% and $\sim$7% reduction of the pixel luminance when each pixel is continuously illuminated at $\sim$25 and 50 $\rm cd/m^2$, respectively. This type of threshold voltage shift and pixel luminance decrease can be considered as the worst case for our pixel electrode circuit. Better compensation can be achieved by the optimization of the pixel electrode circuit design.

VI. Pixel Electrode Circuit Measurements

To analyze the electrical performance of the pixel electrode circuit, we measured the electrical characteristics of the circuit without PLED by applying ground (GND) to the ITO (source of T3), Figs. 1(b) and 3(a). A semiconductor parameter analyzer (HP 4156A) with a pulse generator expander (HP 41 501A) was used to apply $I_{\rm data}$, $V_{\rm DD}$, $V_{\rm select1}$, and $V_{\rm select2}$ to the pixel electrode circuit as shown in Fig. 3(a). It is noted that during this study, for the one pixel electrode circuit analysis, 0–40 V with duty ratio 40% (40 ms select time and 60 ms deselect time) signals were used for $V_{\rm select1}$ and $V_{\rm select2}$ to guarantee that an appropriate data signal is stored during select time after a peak current flows for all the data current levels. Since we applied a constant (not pulsed) current as a data signal, a peak current flow was observed during the select time transition as discussed in Section VII, which increases the data storage settling time during select time. Therefore, if a pulsed current signal is used for our pixel electrode circuit, we believe that we can further reduce the signal duty ratio and this reduction will be sufficient to operate higher resolution AM-PLED. As the number of line increases, charge leakage can be critical during the long frame time. However, our previously reported simulation results [8] showed that an excellent off-current of switching a-Si:H TFT did not cause any significant charge leakage during the frame time for 60Hz, VGA (640$\times$ 480) operation.

In our experiment, we used a combination of an operational amplifier (National Semiconductor LM741C) and an oscilloscope (HP 54 615B) to measure the current flow at the source of T3, which is denoted as $I_{\rm out}$ in Fig. 1(a). The operational amplifier provides virtual GND for the source of T3 and directs the

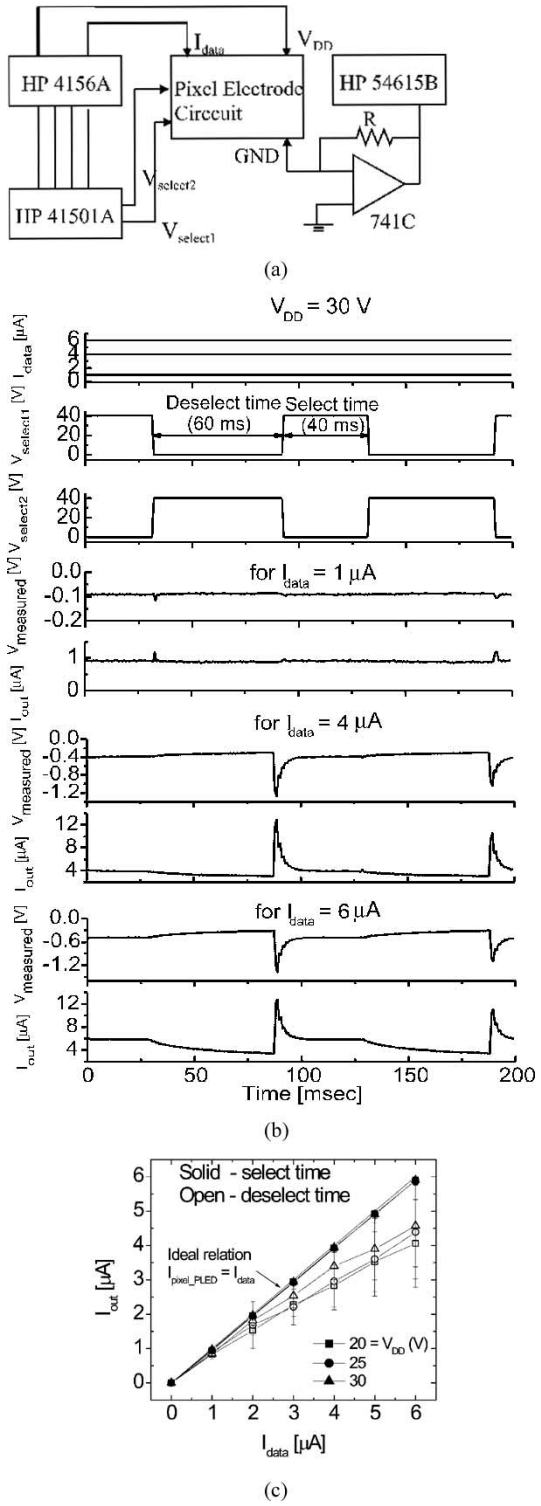

Fig. 3. Pixel electrode circuit measurement results. (a) Measurement setup. (b) Example of measured waveforms for $I_{\rm data}$ = 1, 4, and 6 μA for $V_{\rm DD}$ = 30 V, and $(c) I_{\rm out} - I_{\rm data}$ characteristics for $V_{\rm DD}$ = 20, 25, and 30 V are shown.

current flow from the source of T3 through a 100 kΩ resistor (R). Then, the voltage drop across the resistor was measured ($V_{\rm measured}$) and displayed as a waveform on the oscilloscope display. The current flow ($I_{\rm out}$) at the source of T3 was calculated by $V_{\rm measured}/{\rm R}$. It should be noted that LM741C has an input bias current of 80 nA (typical at RT) and 0.5–0.8 μA (maximum depending on temperature). Therefore, we first measured the voltage drop across R when $I_{\rm data} = 0$ A, which was found to be $\sim +10$ mV. This voltage level can correspond to dc current of $\sim$100 nA flowing into the op amp at zero data current. We added this zero-data-current voltage to the $V_{\rm measured}$ for $I_{\rm data}$ of 1–6 μA to accurately calculate $I_{\rm out}$. An example of measured signal waveforms for $I_{\rm data}$ =1, 4, and 6 μA, when $V_{\rm DD} = 30$ V is shown in Fig. 3(b). At $I_{\rm data} = 1$ μA, $I_{\rm out}$ is close to $I_{\rm data}$ during select and deselect time. However, at $I_{\rm data}$ =4 and 6 μA, $I_{\rm out}$ is close to $I_{\rm data}$ during select time, while $I_{\rm out}$ is lower than $I_{\rm data}$ during deselect time. It is speculated that this $I_{\rm out}$ reduction during deselect time is associated with an operating point change of the pixel electrode circuit. We observed a peak current flow, especially for large $I_{\rm data}$, during select time transitions, which is caused by the precharged pixel effect during the previous frame time. To remove this effect, a current-sink type approach [5] and/or a current driver reset function [11] can be used.

The measured $I_{\rm out} - I_{\rm data}$ characteristics for different $V_{\rm DD}$ values (20, 25, 30 V) are shown in Fig. 3(c), where solid and open symbols represent the $I_{\rm out}$ measured during select and deselect time, respectively. The peak current flow for $I_{\rm out}$ during the select time transition is excluded in Fig. 3(c). For the deselect time $I_{\rm out}$ values, the median values with error bars are plotted to represent the $I_{\rm out}$ change during deselect time. The select time $I_{\rm out}$ values are very close to the $I_{\rm data}$ levels for different $V_{\rm DD}$ values. However, the deselect time $I_{\rm out}$ values deviate from the ideal curve (solid line) at higher $I_{\rm data}$ current levels. This deviation is consistent with the simulation data [8] and corresponds to the pixel electrode circuit operating point change during deselect time, which will be further discussed in Section V. In this study, $V_{\rm DD}$ greater than 30 V is not considered since T4 operates in the saturation regime when $V_{\rm DD} > 30$ V during deselect time due to the high-threshold voltage (10–11 V) of our TFTs. A good linear relation between $I_{\rm out}$ and $I_{\rm data}$ up to $\sim$1, $\sim$2, and $\sim$3 μA has been achieved for $V_{\rm DD}$ =20, 25, and 30 V, respectively.

VII. Pixel Electrode Circuit Load Line Analysis

To further investigate the pixel electrode circuit characteristics, we performed a load line analysis during select and deselect time, based on the measured circuit and TFT characteristics.

A. Select Time Operation

We measured $V_{\rm data}$ at the $I_{\rm data}$ line of the pixel electrode circuit, while applying various $I_{\rm data}$ values during select time. Variation of $V_{\rm data}$ with $I_{\rm data}$ is shown in Fig. 4(a). The measured voltage is related to the required compliance voltage of a current driver when $I_{\rm data}$ is supplied by the current driver. $V_{\rm data}$ rapidly increases as $I_{\rm data}$ increases above 13–14 μA (measured $V_{\rm data} >\sim$ 30 V). This rapid increase of $V_{\rm data}$ comes from the operating point change of T2 from the linear to saturation regime as $I_{\rm data}$ increases. When 40 V is applied to $V_{\rm select1}$ during select time and if $V_{\rm data} > 30$ V, then $V_{\rm GS\_T2} - V_{\rm DS\_T2} < V_{\rm th\_T2}$ (10–11 V). However, the $I_{\rm data}$ operational limit for our

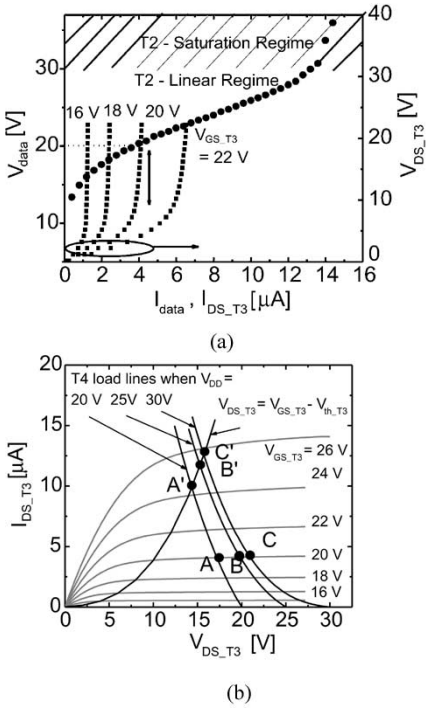

Fig. 4. Load line analysis of pixel electrode circuit. (a) $V_{\rm data} - I_{\rm data}$ and $V_{\rm DS\_T3} - I_{\rm DS\_T3}$ characteristics during select time are shown. $V_{\rm data}$ was measured at $I_{\rm data}$ line during select time. The thick double-headed arrow shows the $I_{\rm data}$ level, where T3 operating point changes from saturation regime to the linear regime ($V_{\rm GS\_T3} - V_{\rm DS-T3} = V_{th\_T3}$) assuming $V_{\rm GS\_T3} = V_{\rm data}$ during select time. (b) $I_{\rm DS\_T3} - V_{\rm DS\_T3}$ characteristics for several $V_{\rm GS\_T3}$ and T4 load lines for $V_{\rm DD} = 20$, 25, and 30 V are shown. The operating points of the pixel electrode circuit change from A, B, and C to A', B', and C' as $I_{\rm data}$ increases.

pixel electrode circuit during select time is determined by the operating point change of T3 from saturation to linear regime according to the increase of $I_{\rm data}$. Since $V_{\rm DS\_T1}$ is negligible at the end of the charging time, it is reasonable to assume that $V_{\rm GS\_T3}$ is charged up to $V_{\rm data}$ during select time ($V_{\rm GS\_T3} = V_{\rm data}$). By plotting $I_{\rm DS\_T3} - V_{\rm DS\_T3}$ characteristics for several $V_{\rm GS\_T3}$ values (22, 20, 18, 16 V) in Fig. 4(a), we estimated the $I_{\rm data}$ operational limit during select time. The T3 operating points change from saturation to linear regime when $V_{\rm GS\_T3} - V_{\rm DS\_T3} = V_{\rm th\_T3}$, i.e., $V_{\rm data} - V_{\rm DS\_T3} = V_{\rm th\_T3}$. For $I_{\rm data} = 3$–4 μA, $V_{\rm data} =\sim 20$ V and $V_{\rm DS\_T3} =\sim 9$ V, the $V_{\rm data} - V_{\rm DS\_T3} =\sim 11$ V $\cong V_{\rm th\_T3}$ [thick double-headed arrow in Fig. 4(a)]. Therefore, based on Fig. 4(a), we can conclude that T3 will operate in the linear regime for $I_{\rm data} > 3$–4 μA. If the T3 operating point moves further into the linear regime during deselect time for $I_{\rm data} > 3$–4 μA, a significant reduction of the deselect time $I_{\rm out}$ in comparison with the select time $I_{\rm out}$ is expected for $I_{\rm data} > 3$–4 μA. This is observed by measuring $I_{\rm out} - I_{\rm data}$ for the pixel electrode circuit as shown in Fig. 3(c).

B. Deselect Time Operation

Fig. 4(b) shows the measured $I_{\rm DS\_T3} - V_{\rm DS\_T3}$ characteristics for several $V_{\rm GS\_T3}$, and the measured T4 load lines for several $V_{\rm DD}$ (20, 25, 30 V). To produce the load lines, we first obtained $I_{\rm DS\_T4} - V_{S\_T4}$ characteristics by sweeping T4 source voltage (V_{S_T4}) for constant T4 drain ($V_{\rm DD}$) and gate ($V_{\rm select2}$ high value) voltages. Then, $I_{\rm DS\_T4} - V_{\rm DS\_T4}$ characteristics were obtained by calculating $V_{\rm DS\_T4} = V_{\rm DD} - V_{S\_T4}$ for each $I_{\rm DS\_T4}$. For a given $I_{\rm data}$, $I_{\rm DS\_T4} = I_{\rm DS\_T3} (= I_{\rm data})$ and $V_{\rm DD} = V_{\rm DS\_T4} + V_{\rm DS\_T3}$ during deselect time. Therefore, we produced T4 load lines by plotting $I_{\rm data}$ versus $V_{\rm DS\_T3} (= V_{\rm DD} - V_{\rm DS\_T4})$. $V_{\rm DD}$ larger than 30 V is not considered in this study since T4 operates in the saturation regime when $V_{\rm DD} >$ 30 V ($V_{\rm GS\_T4} - V_{\rm DS\_T4} < V_{\rm th\_T4}$, 10–11 V). The crossing points A, B, and C in Fig. 3(b) represent the normal operating points for the pixel electrode circuit during deselect time since T4 and T3 operate in the linear and saturation regimes, respectively. However, as $I_{\rm DS\_T3} (= I_{\rm data})$ increases, the operating points move from A, B, and C to A', B', and C' for $V_{\rm DD} = 20$, 25, and 30 V, respectively. The operating points, A', B', and C' represent the current operational limit of the pixel electrode circuit during deselect time, as T3 operates in the linear regime at these points ($V_{\rm DS\_T3} = V_{\rm GS\_T3} - V_{\rm th\_T3}$). From Fig. 3(b), we can obtain the current operational limits of $\sim$10, $\sim$12, and $\sim$13 μA for $V_{\rm DD} = 20$, 25, and 30 V, respectively. It is noted that T3 operates in the saturation regime during deselect time for $I_{\rm data}$ from 3–4 μA to $\sim$13 μA for $V_{\rm DD} = 30$ V, while during select time for the same $I_{\rm data}$ range, T3 operates in linear regime. Therefore, the deselect time $I_{\rm out}$ is expected to be larger than the select time $I_{\rm out}$ if the stored voltage $V_{\rm GS\_T3}$ does not change. However, when we measured the $I_{\rm out} - I_{\rm data}$ characteristics of the pixel electrode circuit, as shown in Fig. 3(c), we observed that the deselect time $I_{\rm out}$ is smaller than the select time $I_{\rm out}$ for $I_{\rm data} > 3$–4 μA. We speculate that the analysis based on the separate TFT characteristics and theoretical ideal conditions might not completely represent the actual pixel electrode circuit behavior since more parasitic capacitance and/or undesired charge/current leakage may be involved in the complicated circuit configuration. Although further investigation in combination with the simulation is needed to explain details of the fabricated pixel electrode circuit operation, the load line analysis performed here enables us to estimate the operational limit of the pixel electrode circuit.

Based on the pixel electrode circuit operation analysis performed in this section, it is found that pixel electrode circuit operating point change limits the pixel electrode circuit performances. Specifically, operating point change of the driving transistor T3 from saturation to the linear regime limits the operating range of the pixel electrode circuit. However, it is noted that the pixel electrode circuit analysis performed in this section excludes the pixel_PLED characteristics. Therefore, to investigate the operational properties and limitations of the AM-PLED pixel, further analysis is needed as discussed in Section VIII.

VIII. AM-PLED Pixel Characteristics

A. Pixel_PLED Optoelectronic Characteristics

To investigate the AM-PLED pixel characteristics, we extracted the optoelectronic characteristics of the pixel_PLED from the typical PLED optoelectronic characteristics. Fig. 5(a) shows the typical PLED current density and luminance versus voltage ($J_{\rm PLED} - L_{\rm PLED} - V_{\rm PLED}$) characteristics. The device structure of a typical red PLED (2.54 $\times$ 2.54 $\rm mm^2$) fabricated in our laboratory on flexible plastic substrates is also included, which consists of a hole injection (HIL) and a light-emissive

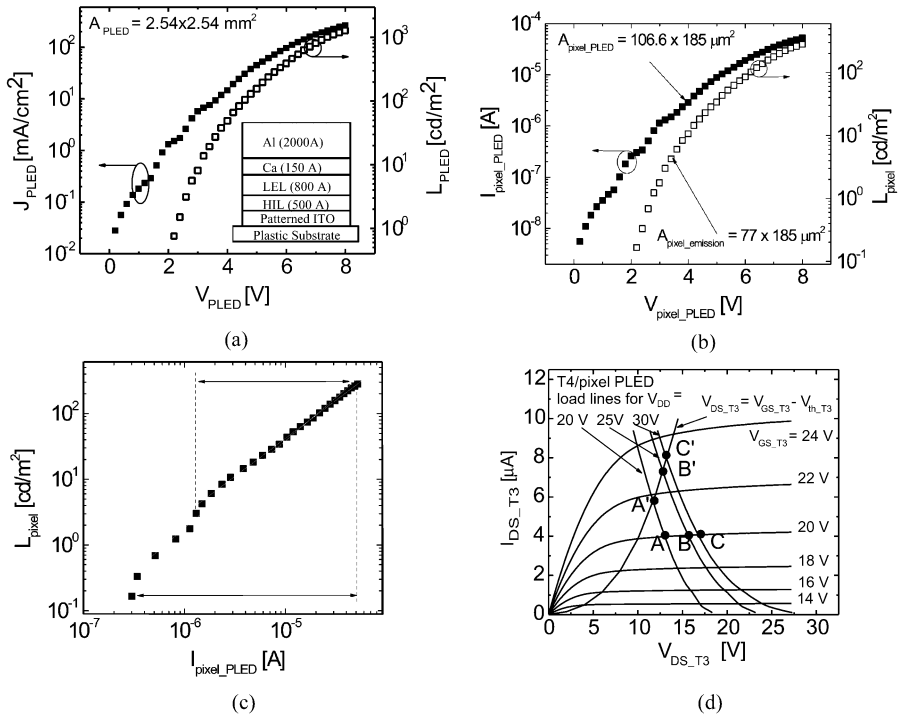

Fig. 5. AM-PLED pixel optoelectronic characteristics. (a) Optoelectrical characteristics of a typical red PLED fabricated in our laboratory on flexible plastic substrates. (b) and (c) Extracted optoelectrical properties of pixel_PLED. (d) $I_{\mathrm{DS\_T3}} - V_{\mathrm{DS\_T3}}$ characteristics for several $V_{\mathrm{GS\_T3}}$ and T4/pixel PLED load lines for $V_{\mathrm{DD}} = 20$, 25, and 30 V are shown. The operating points for AM-PLED pixel change from A, B, and C to A', B', and C' as I_{data} increases.

layer (LEL). Poly (3,4-ethylene dioxythiophene) (PEDOT) doped with poly (styrenesulfonate) (PSS), and red light-emitting poly (fluorene) copolymer [12] have been used for HIL and LEL materials, respectively. A calcium/ aluminum (Ca/Al) bilayer was used for the cathode. The PLED voltage and current density corresponding to 1 cd/m^2 luminance are $\sim$2.5 V and $\sim$0.9 mA/cm^2, respectively. The maximum light-emission and power efficiencies of 0.53 cd/A and 0.27 lm/W are obtained at 1000–1300 and 50 cd/m^2, respectively. From these PLED characteristics, the pixel_PLED optoelectronic characteristics for 100 dpi monochromatic red light-emitting 4-a-Si:H TFTs AM-PLED have been estimated. Assuming that the PLED current density and luminance versus voltage characteristics do not change with the PLED size, which we experimentally verified, we have calculated pixel_PLED$I_{\mathrm{pixel_PLED}} - V_{\mathrm{pixel_PLED}}$ and pixel luminance (L_{pixel}) characteristics by using the following equations:

$$V_{\mathrm{pixel\_PLED}} = V_{\mathrm{PLED}} \tag{1}$$

$$I_{\mathrm{pixel\_PLED}} = J_{\mathrm{PLED}} \times A_{\mathrm{pixel\_PLED}} \tag{2}$$

$$L_{\mathrm{pixel}} = \frac{L_{\mathrm{PLED}} \times A_{\mathrm{pixel\_emission}}}{A_{\mathrm{pixel}}} \tag{3}$$

where $A_{\mathrm{pixel\_PLED}}$, $A_{\mathrm{pixel\_emission}}$, and A_{pixel} are the effective pixel current flowing area (106.6 $\times$185 μm^2), the pixel light-emitting area (77 $\times$ 185 μm^2), and the total pixel area (254 $\times$254 μm^2), respectively. The difference between $A_{\mathrm{pixel\_PLED}}$ and $A_{\mathrm{pixel\_emission}}$ comes from overlap between the pixel_PLED ITO electrode and the T3 source, as shown in Fig. 1(b). The calculated pixel_PLED optoelectronic characteristics are shown in Fig. 5(b) and (c). The extracted $L_{\mathrm{pixel}} - I_{\mathrm{pixel\_PLED}}$ characteristics can be described as the following equation by fitting extracted data in two different $I_{\mathrm{pixel\_PLED}}$ ranges. A slight deviation from the linear relationship was observed at lower luminance levels ($< \sim 2$ cd/m^2) in Fig. 5(c). This deviation comes from a fluctuation in $J_{\mathrm{PLED}} - V_{\mathrm{PLED}}$ measurement at lower voltages (< 2.5 V) due to smaller increase step (0.2 V) for the applied V_{PLED}, as shown in Fig. 5(a)

$$L_{\mathrm{pixel}} \propto I^{\alpha}_{\mathrm{pixel\_PLED}}, \quad (\alpha = 1.2 \pm 0.1).$$

B. AM-PLED Pixel Load Line Analysis

To analyze AM-PLED pixel operation, we have produced load lines for T4 and pixel_PLED during deselect time. Fig. 5(d) shows the measured $I_{\mathrm{DS\_T3}} - V_{\mathrm{DS\_T3}}$ characteristics for several $V_{\mathrm{GS\_T3}}$ and T4/pixel_PLED load lines for several V_{DD} (20, 25, 30 V). To produce the load lines, we used the $I_{\mathrm{pixel\_PLED}} - V_{\mathrm{pixel\_PLED}}$ characteristics and $I_{\mathrm{DS\_T4}} - V_{\mathrm{DS\_T4}}$ characteristics extracted in Section V. For a given I_{data}, $I_{\mathrm{DS\_T4}} = I_{\mathrm{DS\_T3}} = I_{\mathrm{pixel\_PLED}} (= I_{\mathrm{data}})$ and $V_{\mathrm{DD}} = V_{\mathrm{DS\_T4}} + V_{\mathrm{DS\_T3}} + V_{\mathrm{pixel\_PLED}}$ during deselect time. Therefore, we produced T4/pixel PLED load lines by plotting I_{data} versus $V_{\mathrm{DS\_T3}} (V_{\mathrm{DD}} - V_{\mathrm{DS\_T4}} - V_{\mathrm{pixel\_PLED}})$. The crossing points A, B, C and A', B', C' represent the normal operating points and the operational I_{data} range for the AM-PLED pixel. From Fig. 5(d), we can obtain the I_{data} operational limits of $\sim$6, $\sim$7, and $\sim$8 μA for $V_{\mathrm{DD}} = 20$, 25, and 30 V, respectively, which correspond to 23, 27, and 31 cd/m^2 pixel luminance in Fig. 5(c). It is noted that these pixel luminance values were extracted from the red PLED with

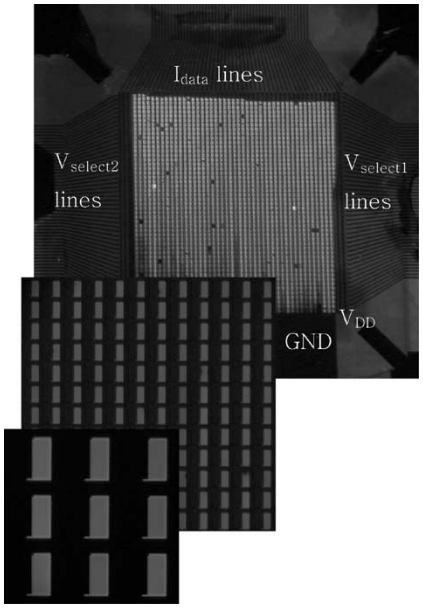

Fig. 6. Top view of illuminated 100 dpi 4-a-Si:H TFTs AM-PLED and magnified images of pixel light emission. The light-emission yield was about 70% for this display.

an emission efficiency of ~ 0.53 cd/A and for AM-PLED with AR of $\sim 22\%$. Therefore, if PLED with higher efficiency is used and/or higher AR AM-PLED is implemented by using top-emission pixel_PLED structure, our pixel electrode circuit can possibly produce much higher pixel luminance. In addition, if we further optimize our pixel electrode circuit design and process, we believe that the AM-PLED pixel $I_{\rm data}$ operational range can be further increased.

IX. 100 DPI 4-A-SI:H TFTS AM-PLED

To demonstrate a-Si:H TFT technology, we have fabricated 100 dpi monochromatic red light-emitting 4-a-Si:H TFTs AM-PLED (0.5×0.5 in^2) with 50×50 pixels. 100 dpi represents the resolution of our AM-PLED since our display has 50 dots (monochromatic pixels) for each 0.5-inch row and column line. On the AM arrays, we deposited PLED active bilayers and a Ca/Al bilayer cathode. The pixel PLED structure is the same as the one shown in Fig. 5(a). In our AM-PLED, all cathode electrodes for each pixel are connected. We removed the PLED active layers from the contact pads with solvent.

For display evaluation, 0–15 mA was applied through $I_{\rm data}$ lines to measure the display luminance at different data current levels. Fig. 6 shows the demonstration of 100 dpi monochromatic red light-emitting 4-a-Si:H TFTs AM-PLED when the data current is 5 mA. The AM-PLED shows a functional pixel yield of $\sim 70\%$. A magnified image of discrete pixel light-emission is also included in Fig. 6.

The optoelectrical characteristics of the display have been measured using an integrating sphere and a calibrated photo-detector connected to a radiometer [13]. We have measured the total luminous flux from the AM-PLED for different $I_{\rm data}$, Fig. 7(a). The AM-PLED luminance was calculated from the measured luminous flux of the display. For a Lambertian emitter, the luminance (L) can be calculated from the measured luminous flux (Φ) by using the following equation:

$$L = \frac{\Phi}{\pi \times A} \tag{4}$$

where A is the area of the light emitter. We have experimentally verified that our AM-PLED is a Lambertian emitter [14]. By considering the pixel light-emission yield of 0.7, the light-emitting display area A is $1.27\,\text{cm} \times 1.27\,\text{cm} \times 0.7 = 1.12 \times 10^{-4}\,\text{m}^2$. The calculated AM-PLED luminance is plotted versus $I_{\rm data}$ in Fig. 7(a). We observed the initial light-emission at the data current of 20 μA, and obtained AM-PLED luminance of up to 20 cd/m^2 at the data current of 15 mA. This experimental curve can be compared with estimated AM-PLED luminance versus display $I_{\rm data}$ characteristics.

From the pixel_PLED optoelectrical characteristics shown in Fig. 5(c), we can estimate the display luminance of our illuminated AM-PLED by assuming that there is no current flow through the pixels without light-emission. First, we can calculate the total display $I_{\rm data}$ required for our AM-PLED (50×50 pixels) with 70% light-emission yield by using the following equation:

$$\text{totaldisplay } I_{\rm data} = I_{\rm pixel\_PLED} \times 50 \times 50 \times 0.7. \tag{5}$$

The 70% illuminated AM-PLED luminance at a given calculated total display $I_{\rm data}$ is equal to $L_{\rm pixel}$ at the corresponding $I_{\rm pixel\_PLED}$. This estimated display luminance is also plotted in Fig. 7(a) versus the total display $I_{\rm data}$. The estimated AM-PLED luminance is larger by about a factor of two in comparison with the AM-PLED luminance calculated from the measured luminous flux. This difference in display performances can be related to the nonuniform pixel light-emission in certain areas of the fabricated display and/or the waveguided light loss through the a-SiN_x:H and BCB layers and thicker glass substrate in comparison with the typical PLEDs on plastic substrates that have been used in this data extraction [14].

We also measured $V_{\rm data}$ at the $I_{\rm data}$ lines of the pixel electrode circuit for various $I_{\rm data}$ during select time, Fig. 1(a). The variation of $V_{\rm data}$ with $I_{\rm data}$ is shown in Fig. 7(b). This measured voltage is related to the required compliance voltage of the current driver that supplies $I_{\rm data}$. For example, to apply $I_{\rm data}$ up to 15 mA for our AM-PLED, the current driver should have a capacity of at least 37 V for the compliance voltage.

In Fig. 7(c), the electroluminescent (EL) spectra of the red light-emitting AM-PLED and PLED are shown. We obtained EL peak positions at 654 and 653 nm, and full-width-half-maximum (FWHM) of 101 and 105 nm, for the AM-PLED and PLED, respectively. From the obtained EL spectra, we also calculated CIE color coordinates [15] for AM-PLED and PLEDs, which are (0.67, 0.33) and (0.67, 0.32), respectively, as shown in the inset of Fig. 7(c). These very similar color coordinates indicate that the PLED EL characteristics can be used to define the CIE color coordinates for the full color AM-PLED.

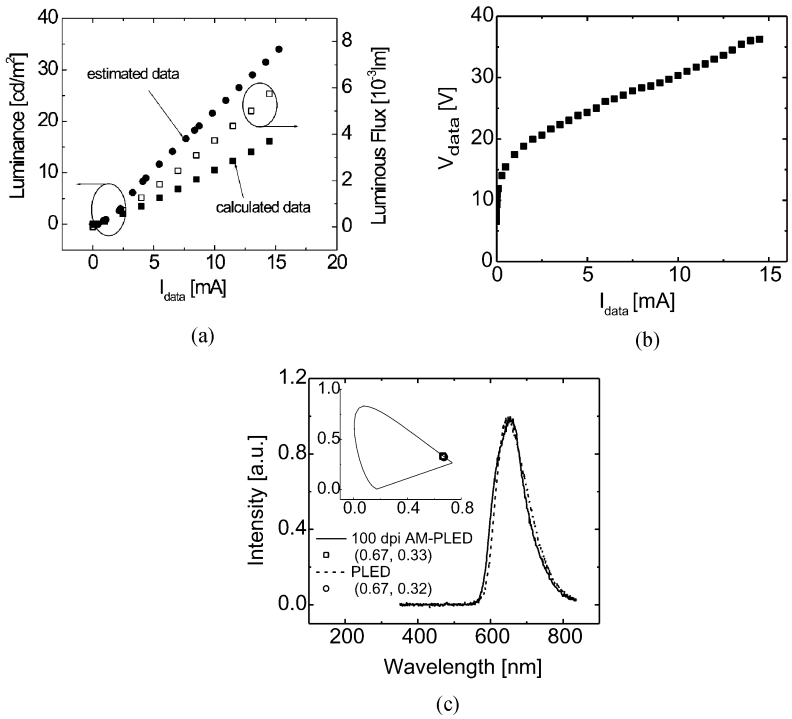

Fig. 7. AM-PLED optoelectronic characteristics. (a) Measured luminous flux, calculated display luminance, and estimated display luminance versus $I_{\rm data}$ characteristics. (b) Measured $V_{\rm data}$ variation for different $I_{\rm data}$ characteristics. (c) PLED and AM-PLED electroluminescent (EL) spectra are shown. The CIE color coordinates of the PLED and AM-PLED are also shown in the inset of this figure.

X. Conclusion

In this paper, we demonstrated that our 4-a-Si:H TFTs pixel electrode circuit can be used for an AM-PLED. From analysis of the display pixel operation properties, we found that the operating point change of a driving TFT (T3) from saturation to the linear regime limits the display operational range to $I_{\rm data} =\sim 8\ \mu$A. This current level will result in the estimated AM-PLED luminance of $\sim$30 cd/m^2, under normal display operation conditions. For our AM-PLED, we measured luminance up to $\sim$20 cd/m^2 and CIE color coordinates of (0.67, 0.33). It should be noted that experimental results described in this paper do not represent the optimum performance that can be expected for the a-Si:H TFTs AM-PLED technology. The display performance can be improved tremendously when a high efficiency pixel_PLED, a high aperture-ratio top-emission pixel_PLED structure and/or optimized pixel electrode circuit design and processes are used in the flat panel display industries. Experimental data described in this paper clearly demonstrate that future a-Si:H TFTs AM-PLED technology can challenge today's poly-Si TFTs AM-PLED technology.

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References

[1] R. M. A. Dawson and M. G. Kane, "Pursuit of active matrix organic light emitting diode displays," in *SID Tech. Dig.*, vol. 32, 2001, pp. 372–375.

[2] R. M. A. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson, W. A. Barrow, E. Dickey, K. Ping, S. Robinson, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, M. H. Lu, and J. C. Sturm, "The impact of the transient response of organic light emitting diodes on the design of active matrix oled displays," in *IEDM Tech. Dig.*, 1998, pp. 875–878.

[3] T. Sasaoka, M. Sekiya, A. Yumoto, J. Yamada, T. Hirano, Y. Iwase, T. Yamada, T. Ishibashi, T. Mori, M. Asano, S. Tamura, and T. Urabe, "A 13.0-inch AM-OLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC)," in *SID Tech. Dig.*, vol. 32, 2001, pp. 384–387.

[4] D. Fish, N. Young, M. Childs, W. Steer, D. George, D. McCulloch, S. Godfrey, M. Trainer, M. Johnson, A. Giraldo, H. Lifka, and I. Hunter, "A comparison of pixel circuits for active matrix polymer/organic LED displays," in *SID Tech. Dig.*, vol. 33, 2002, pp. 968–971.

[5] Y. Hong, R. Hattori, and J. Kanicki, "Novel Poly-Si TFT pixel electrode circuits and current programmed active-matrix driving methods for AMOLEDS," in *SID Tech. Dig.*, vol. 33, 2002, pp. 618–621.

[6] Y. He, R. Hattori, and J. Kanicki, "Current-source a-Si:H thin-film transistor circuit for active-matrix organic light-emitting displays," *IEEE Electron Device Lett.*, vol. 21, pp. 590–592, Dec. 2000.

[7] ——, "Improved a-Si:H TFT pixel electrode circuits for active-matrix organic light-emitting displays," *IEEE Trans. Electron Device*, vol. 48, pp. 1322–1325, July 2001.

[8] J. Kanicki, J.-H. Kim, J. Nahm, Y. He, and R. Hattori, "Amorphous silicon thin-film transistors based active-matrix organic light-emitting displays," in *Proc. Asia Display/IDW '01*, 2001, pp. 315–318.

[9] S. K. Bhowmick and B. Mazhari, "An improved four TFT circuit for active-matrix organic light emitting diode (OLED) display," in *SID Tech. Dig.*, vol. 33, 2002, pp. 606–609.

[10] C.-Y. Chen and J. Kanicki, "High-performance a-Si:H TFT for large-area AMLCDs," in *Proc. 26th Eur. Solid State Dev. Reas. Conf.*, 1996, pp. 1023–1031.

[11] R. Hattori, Y. Kuroki, and J. Kanicki, "Analog-circuit simulation of the current-programmed active-matrix pixel electrode circuits based on Poly-Si TFT for organic light-emitting displays," in *AM-LCD Tech. Dig.*, 2001, pp. 223–226.
[12] Y. Hong and J. Kanicki, "Organic polymer light-emitting devices on flexible plastic substrates for AM-OPLED," in *Proc. Asia Display/IDW'01*, 2001, pp. 1443–1446.
[13] ——, "Integrating sphere CCD-based measurement method for organic light-emitting devices," *Rev. Sci. Instrum.*, vol. 74, no. 7, pp. 3572–3575, 2003.
[14] S. Lee, A. Badano, and J. Kanicki, "Monte Carlo modeling of organic polymer light-emitting devices on flexible plastic substrates," *Proc. SPIE*, vol. 4800, pp. 156–163, 2002.
[15] J. W. T. Walsh, *Photometry*. London, U.K.: Constable & Company Ltd., 1958.

Yongtaek Hong (S'94) was born in Busan, South Korea, in 1971. He received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2003, on active-matrix polymer light-emitting display based on a-Si:H TFT technology.

Since 2003, he has been with Advanced Research Laboratories, Eastman Kodak Company, Rochester, NY, as a Senior Research Scientist. He is working on back-plane technology development for robust, flexible flat-panel displays, and digital radiography applications.

Dr. Hong is a Member of SID and The International Society for Optical Engineers (SPIE).

Jeong-Yeop Nahm received the B.S. and M.S. degrees in electronic engineering from Korea University, Seoul, Korea, in 1991 and 1994, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2000. His Ph.D. thesis topic was on active-matrix armorphous silicon thin-film transistors for flat-panel displays.

Since 2001, he has been with the Technology Development Department, Cypress Semiconductor, San Jose, CA, where he is engaged in process and device simulation for deep submicron CMOS technologies.

Jerzy Kanicki (M'99–A'99–SM'00) received the Ph.D. degree in sciences (D.Sc.) from the Free University of Brussels (Universite Libre de Bruxeles), Brussels, Belgium, in 1982. His dissertation research work involved the "Optical, electrical, and photovoltaic properties of undoped and doped transpolyacetylene."

He subsequently joined the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member working on hydrogenated amorphous silicon devices for the photovoltaic and flat-panel display applications. In 1994, he moved from IBM Research Division to the University of Michigan, Ann Arbor, as a Professor in the Department of Electrical Engineering and Computer Science (EECS). He is the author and coauthor of over 200 publications in journals and conference proceedings. He has edited two books and three conference proceedings. At present, his research interests within the Electrical and Computer Engineering (ECE) Division of EECS include organic and molecular electronics, thin-film transistors and circuits, and flat-panel displays technology including organic light-emitting devices.

Dr. Kanicki served as Organizing Chairman and/or Co-Chairman of the Amorphous Insulating Thin Films Symposia (Boston, MA, 1992; Strasbourg, France, 1994; Osaka, Japan, 1995) and the 1988 International Conference on Hydrogenated Amorphous Silicon Devices and Technology, Yorktown Heights, NY. He received several IBM External Honors Prizes in 1989, 1990, and 1993. He is a Member of SID, the American Chemical Society (ACS), the American Physical Society (APS), and MRS.