# Operational Amplifier Stability
## Part 7 of 15: When Does $R_O$ Become $Z_O$?

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A funny thing happened on the way to writing about "There must be six ways to leave your capacitive load stable." http://www.analogzone.com/acqt0704.pdf We chose a CMOS operational amplifier with a "rail-to-rail" output and measured the $R_{OUT}$, where there was no loop gain, at high frequency, to determine $R_O$. From this measurement we predicted a second pole location in the amplifier's "modified Aol plot" due to a 1 µF capacitive load. To our surprise our Tina SPICE simulation for this modified Aol plot was off by a factor of x5! This error was way outside of the acceptable bounds of any of our past first-order analysis and thereby launched a detailed investigation of op amp output impedance.

Here in Part 7 we focus on op amp open-loop output impedance, $Z_O$, for the two most common output topologies for small signal op amps. For traditional bipolar emitter-follower op amp output stages $Z_O$ is well behaved and predominantly resistive ($R_O$) throughout the unity-gain bandwidth. However, for many CMOS rail-to-rail output op amps $Z_O$ is both capacitive and resistive, within the unity-gain bandwidth of the amplifier.

We will not, in this Part, analyze the bipolar topology known as *all npn output*, which is most commonly used in power op amps (capable of operating in a linear region with high output currents from 50 mA to greater than 10 A).

Our expanded knowledge of output impedance will be critical to our correct prediction of modified Aol plots and an essential tool in our network synthesis techniques for stable op amp circuits.

## $Z_O$ for Bipolar Emitter-Follower Output Op Amps

A classical bipolar output stage of emitter-follower topology is shown in Fig. 7.1. With this type of output stage, $R_O$ (small-signal, open-loop output resistance) is usually the dominant portion of $Z_O$ (small-signal, open-loop output impedance). As well, $R_O$ is usually constant for a given dc current load. We will examine some rules-of-thumb for emitter-follower $R_O$ and then use these rules of thumb to predict $R_O$ for various values of dc output current. We will then check our predictions using Tina SPICE simulations.

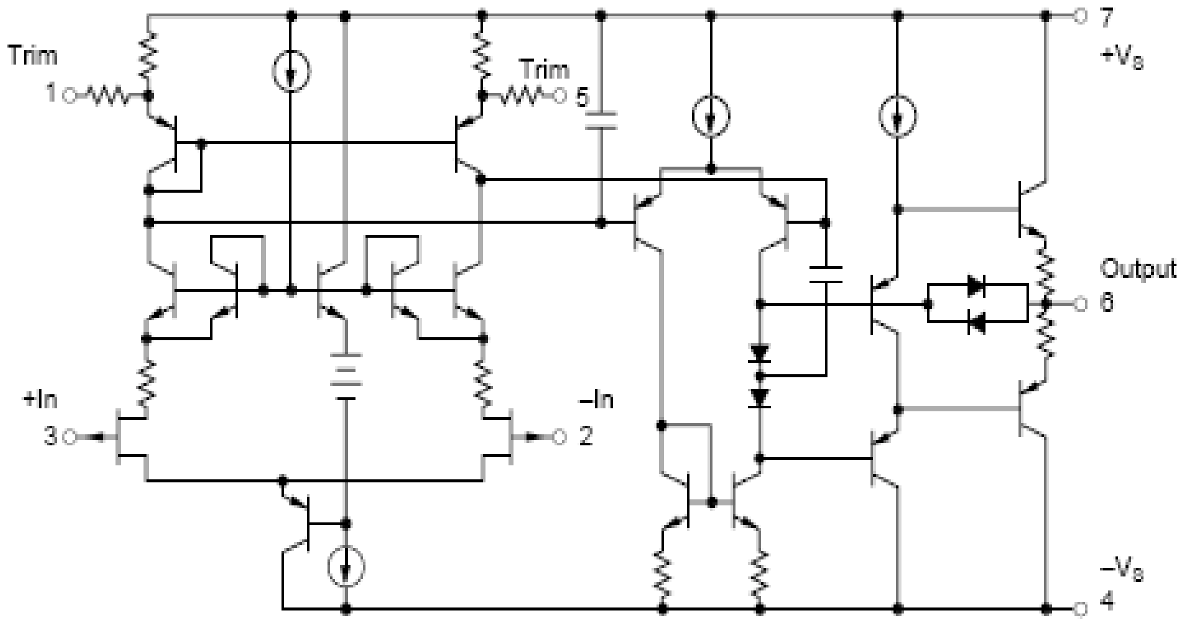



**Fig. 7.1: Typical Emitter-Follower, Bipolar Output Op Amp**

A typical emitter-follower, bipolar output op amp's specifications are shown in Fig. 7.2. This topology often yields low noise, low drift input specifications with the input bias currents in the nA-region (eg 10 nA). Some bipolar op amps use JFETs in the input stages to reduce input bias currents down to the low pA-range. The common-mode input range will usually be about 2 V from either supply. The output voltage swing is typically restricted to within 2 V or more of either supply rail and these op amps commonly get the best performance from using dual supplies (eg ±5 V to ±15 V).

**OPA227**
**High Precision, Low Noise Bipolar Operational Amplifier**

| | | | |
|---|---|---|---|
| **Input Specs** | | **AC Specs** | |
| Offset Voltage | 75uV max | Open Loop Gain, RL = 10k | 160dB typ |
| Offset Drift | 0.6uV/C | Open Loop Gain, RL = 600 | 160dB typ |
| Input Voltage Range | (V-)+2V to (V+)-2V | Gain Bandwidth Product | 8 MHz |
| Common-Mode Rejection Ratio | 138dB typ | Slew Rate | 2.3V/us |
| Input Bias Current | 10nA max | Overload Recovery Time | 1.3us |
| | | Total Harmonic Distortion + Noise | 0.00005%, f=1kHz |
| | | Setling Time, 0.01% | |
| **Noise** | | **Supply Specs** | |
| Input Voltage Noise | 90nVpp, f=0.1Hz to 10Hz | Specified Voltage Range | +/-5V to +/-15V |
| Input Voltage Noise Density | 3nV/rt-Hz @1kHz | Quiescent Current | +/-3.8A max |
| Input Current Noise Density | 0.4pA/rt-Hz | Over Temperature | +/-4.2A max |
| **Output Specs** | | **Temperature & Package** | |
| Vsat @ Iout = 1.2mA | 2V max | Operating Range | -40C to +85C |
| Vsat @ Iout = 19mA | 3.5V max | Package options | SO-8, DIP-8, DIP-14, SO-14 |
| Iout Short Circuit | +/-45mA | | |

**Fig. 7.2: Example Specifications: Emitter-Follower, Bipolar Output Op Amp**

A simplified model for the classic emitter-follower, bipolar op amp uses two GM (current gain) stages followed by a transistor voltage-follower output (see Fig. 7.3). $Z_O$, the open-loop output impedance, is dominated by $R_O$, open-loop output resistance, and is constant over the unity-gain bandwidth.

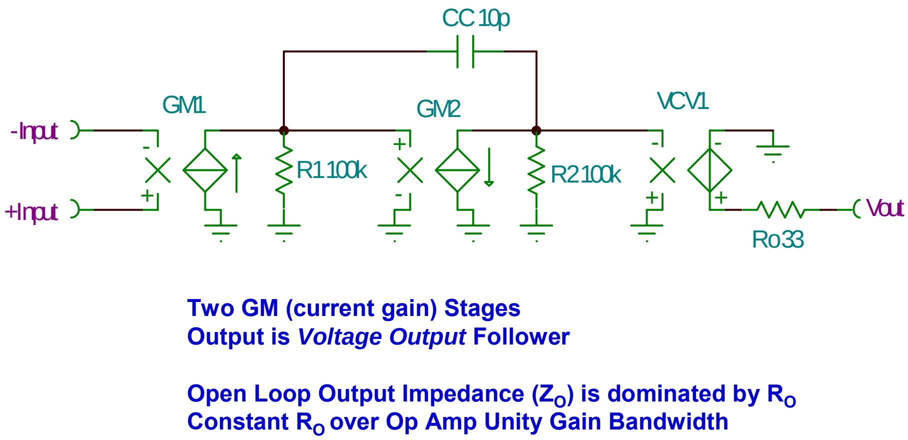



**Fig. 7.3: Two-Stage Simplified Model: Emitter-Follower, Bipolar Output Op Amp**

For most amplifiers the Class-AB bias current in the output stage (with no load) is about half of the quiescent current for the entire amplifier. For bipolar transistors $R_O$ is proportional to 1/gm, where gm is the current transfer ratio or current gain. Since gm is proportional to collector current $I_C$ then we see that $R_O$ is inversely proportional to $I_C$. As $I_C$ increases from no-load to full-load output current $R_O$ will decrease. This might imply that if we pull extremely high currents that $R_O$ would go to zero. However, due to the physics of the transistor and the internal drive and bias arrangement this is not the case. We will measure $R_O$ at the highest useable load current and define it as $R_X$. We will then measure $R_O$ at no load current and derive a constant, $K_Z$, for the given op amp circuitry that will enable us to predict what $R_O$ does with any load current. From Fig. 7.4 we clearly see how the term emitter-follower output describes the path to the output pin of the op amp from the front end gm stages.

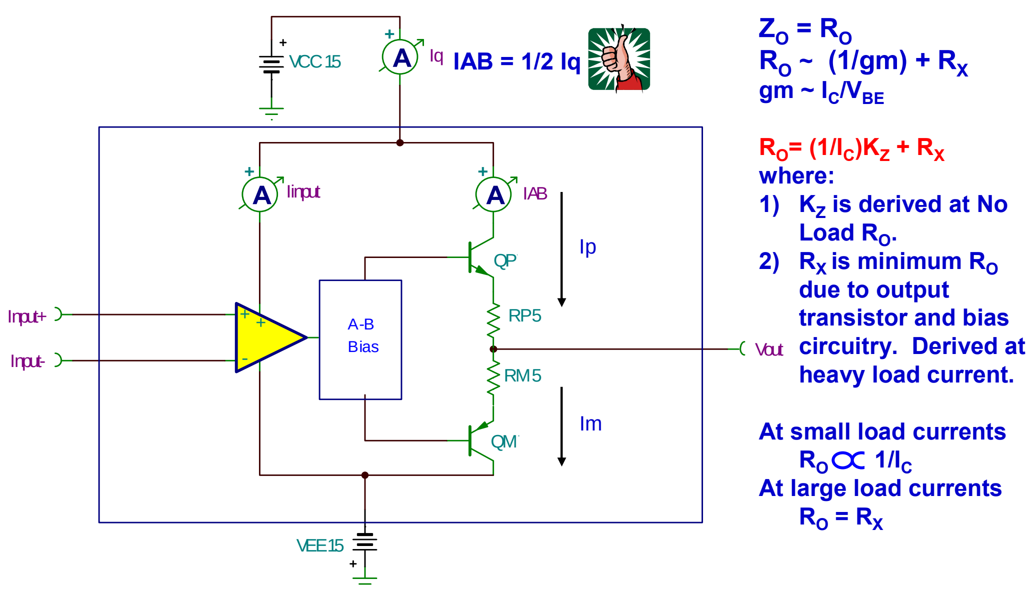



**Fig. 7.4: $Z_O$ Definition: Emitter-Follower, Bipolar Output Op Amp**

Fig. 7.5 details our emitter-follower $Z_O$ model with a constant value $R_X$, measured at full load current, and a series current-dependent resistor, with the transfer function of $K_Z \div I_C$. Since we have a push (pnp transistor) output stage and a pull (npn transistor) output stage our $Z_O$ model includes equivalent $R_O$ models for each stage. The effective small-signal ac output impedance looking back into the output pin will be the parallel combination of the push and pull output stages. Remember that for our small-signal ac model of $Z_O$ both power supplies, VCC and VEE, will appear as an ac short.

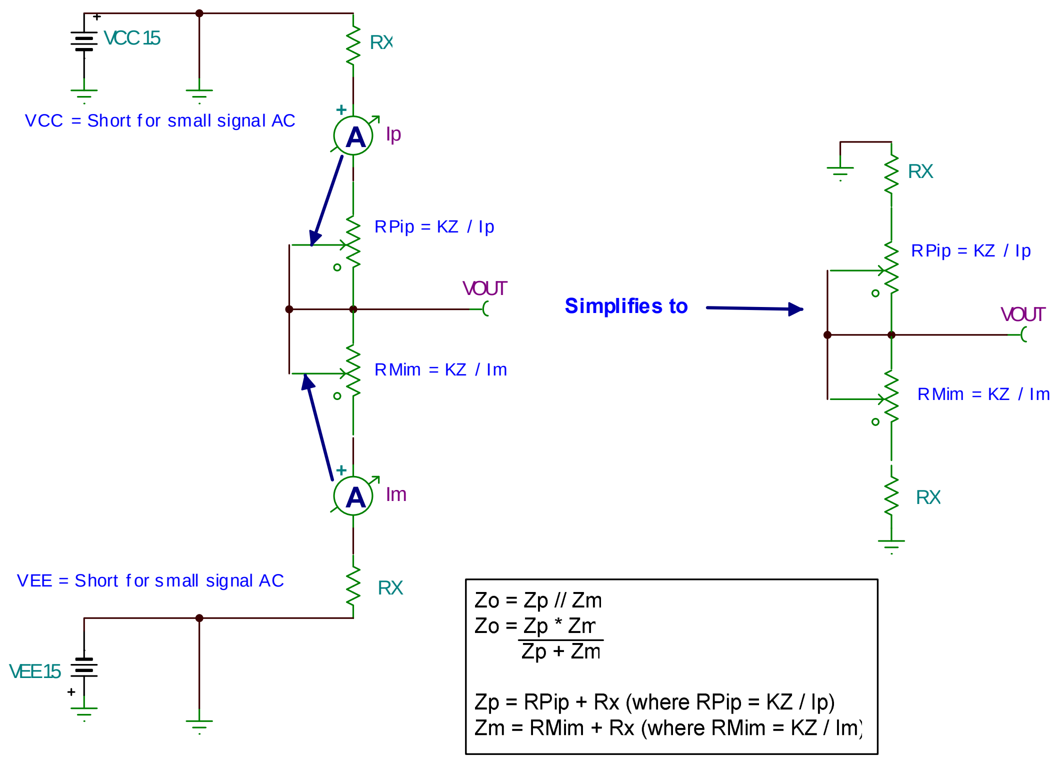



Fig. 7.5: $Z_O$ Model: Emitter-Follower, Bipolar Output Op Amp

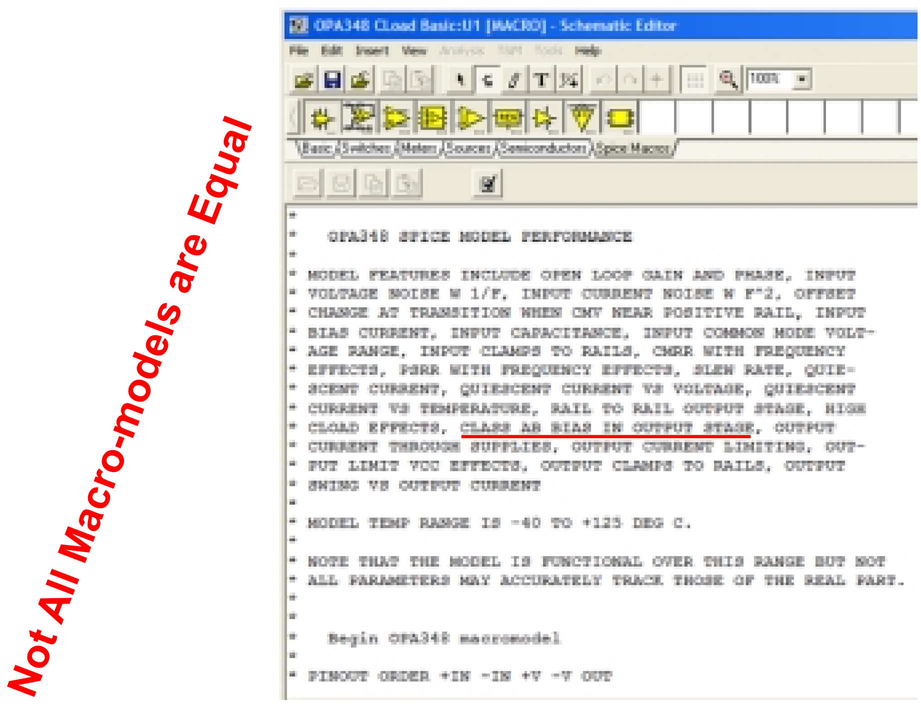



Fig. 7.6: Not All SPICE Op Amp Models Are Equal!

Not all SPICE macro-models for op amps are equal (Fig. 7.6). As such, any simulations we do to investigate output impedance, $Z_O$, must be done on macro-models which correctly model the output with real devices and proper Class-AB bias circuitry which accurately models the actual device. It is not often clear from a given manufacturer if this is adequately modeled. Most SPICE models for precision op amps developed by the Burr-Brown division of Texas Instruments, over the last 4 years, were built by W K Sands of Analog & RF Models (http://www.home.earthlink.net/%7Ewksands/). These SPICE models of the op amp are extremely good representations of the actual silicon op amp and as shown above will include a detailed list of features including proper modeling of the output stage as well as the Class-AB bias circuitry.

Since we were not able to find a bipolar emitter-follower op amp macro-model with accurate Class-AB biasing and real transistor outputs for an accurate analysis of real world behavior we built our own for evaluation purposes.

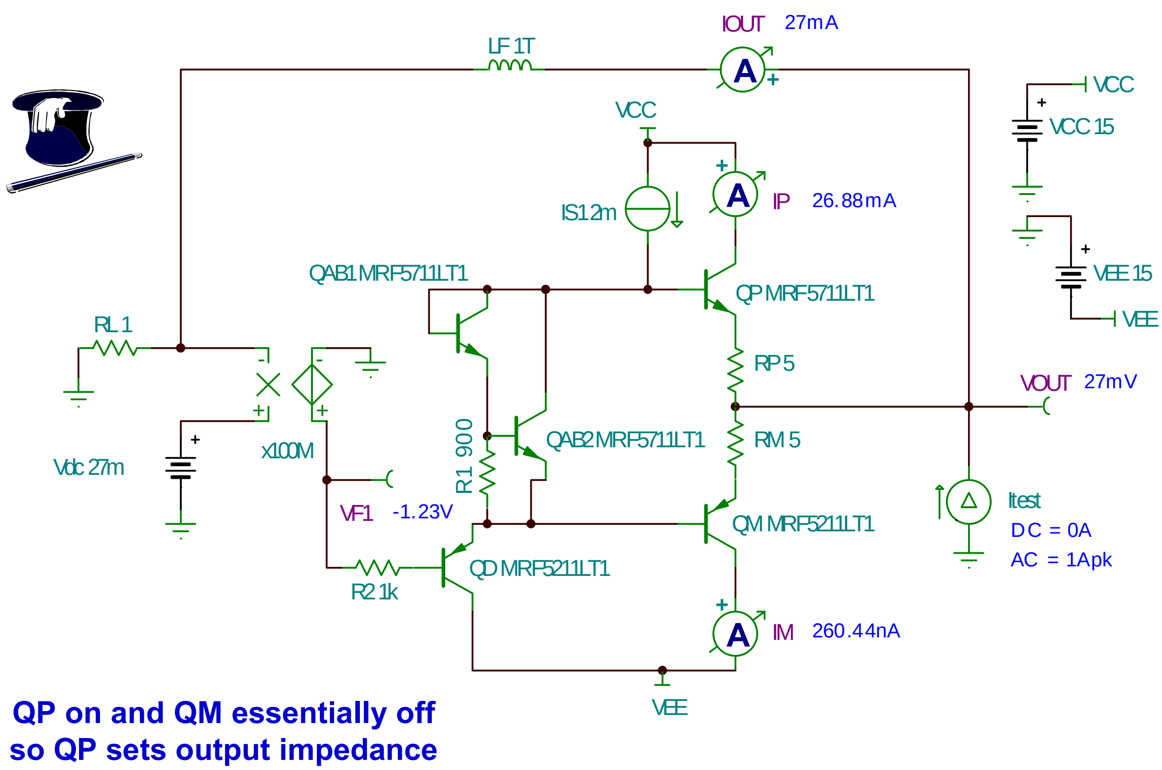



**Fig. 7.7: $Z_O$, Heavy Load $I_{OUT}$ = +27mA**

In Fig. 7.7 we see an ideal front end implemented with a voltage-controlled-voltage source with open loop gain of 160dB (x100E6). The output transistors, QP and QM, are biased on with a simplified Class-AB bias circuit. For our op amp we set the maximum output current at 27 mA and therefore to find our $R_O$ parameter $R_X$ we will test with a load current of +27mA. A simple $Z_O$ test circuit in Tina SPICE is easy to build through the use of an *input resistor* RL and a feedback inductor LF. At dc the inductor is a short and RL, combined with the applied voltage, Vdc, sets the dc load current as shown. With our ideal 1 TH (1E12 henry) inductor we have a dc closed-loop path so SPICE can find an operating point, but for any ac frequency of interest we have an open circuit. Now if we excite our circuit with a 1 A, ac source, Itest, then $V_{OUT}$ becomes $Z_O$ after a math conversion from dB. Notice for this heavy load ($I_{OUT}$ =+27 mA) that QM is essentially off and QP is on and dominates the output impedance.

We see (Fig. 7.8) our measured results for $Z_O$ with $I_{OUT}$ = +27 mA out of our bipolar emitter-follower output op amp. The initial SPICE results will be plotted in *linear-dB*. If we choose logarithmic on the y-axis this will result directly in ohms for $Z_O$. The logarithmic scale on the y axis will become handy when we look at other $Z_O$ plots that are not constant over the frequency bandwidth (ie CMOS RRO).

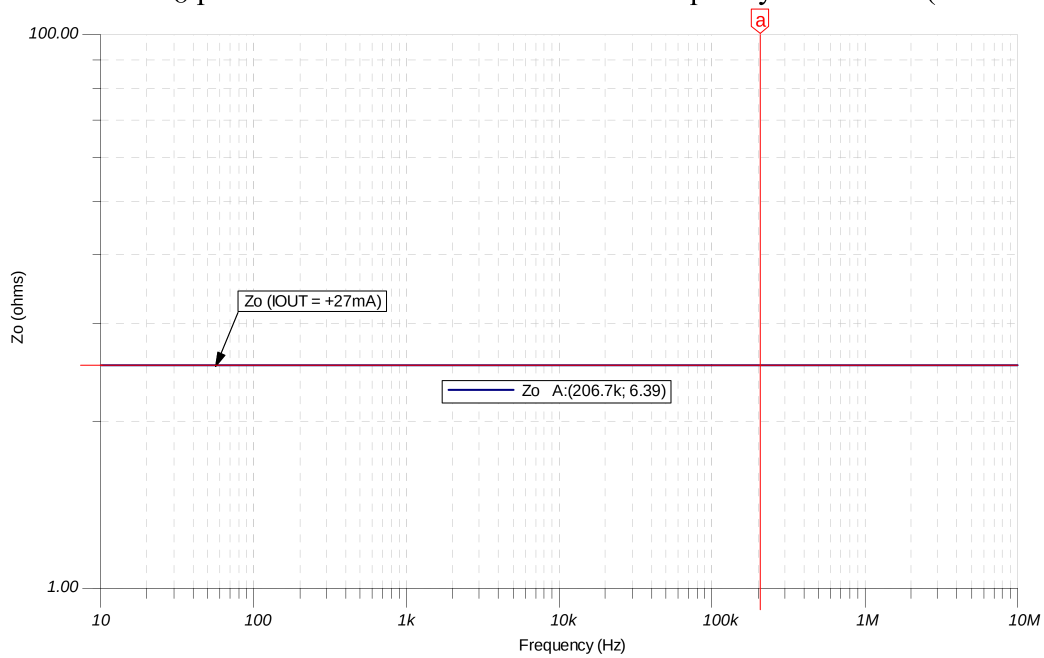



**Fig. 7.8: $Z_O$ AC Plot, Heavy Load, $I_{OUT}$ = +27mA**

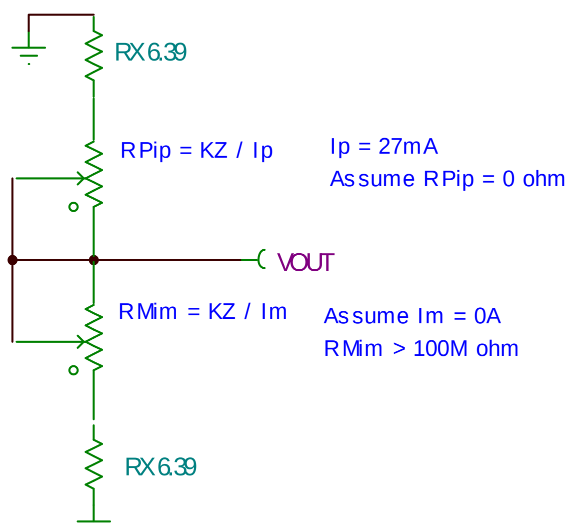



**Fig. 7.9: Heavy-Load $Z_O$ Model**

In our equivalent heavy-load $Z_O$ model for $I_{OUT}$ = +27 mA (Fig. 7.9) $R_X$ was measured to be 6.39 Ω. We will assume that the output transistors (QP and QM) used are close in characteristics and therefore assign $R_X$ the same value for each. If we wanted we could re-run our analysis and measure $R_X$ for $I_{OUT}$ = -27 mA. The results would be close enough for us to ignore the difference. From this model we assume RMim will be high impedance and therefore have no measurable effect on $R_O$. Also we assume RPip will be much smaller than $R_X$.

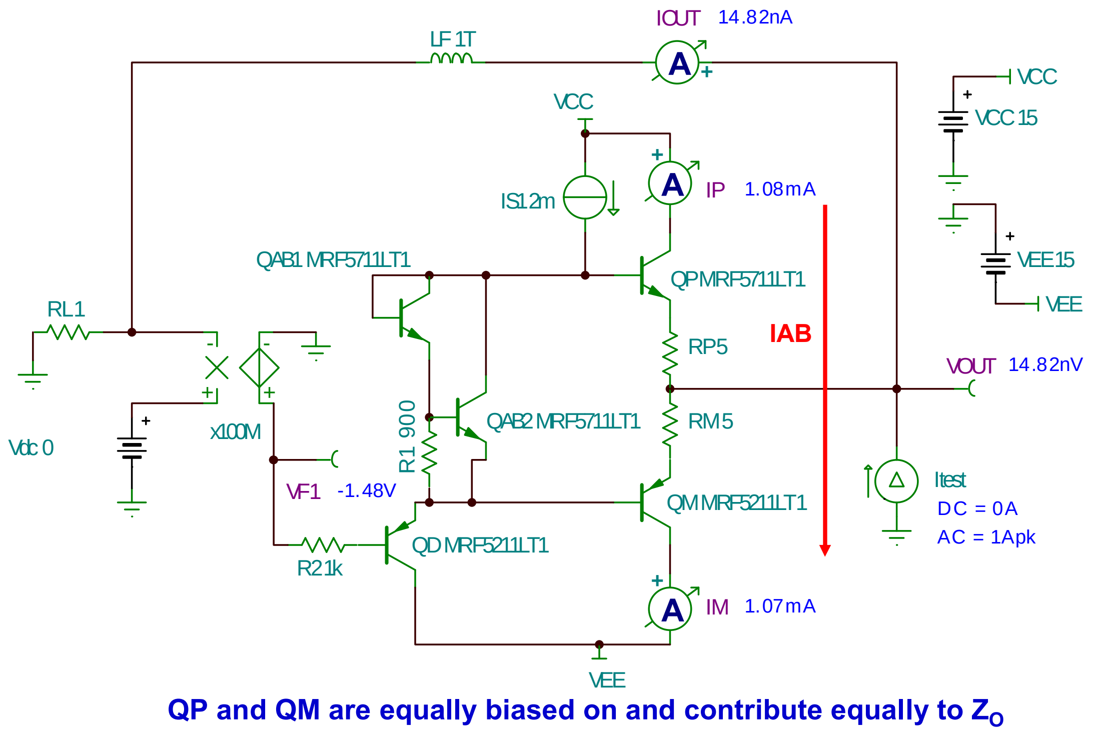



**Fig. 7.10: $Z_O$, No Load, $I_{OUT}$ = 0mA**

The no-load condition for our Class-AB bias emitter-follower (Fig. 7.10) has the bias current, $I_{AB}$, set to 1.08 mA. We see that both output transistors, QP and QM, are on and both contribute equally to $Z_O$. The no-load $Z_O$ is measured as 14.8 Ω (Fig. 7.11) which, with the heavy-load value for $Z_O$ (with a result for $R_X$) allows us to complete our small-signal $Z_O$ model by computing the constant $K_Z$.

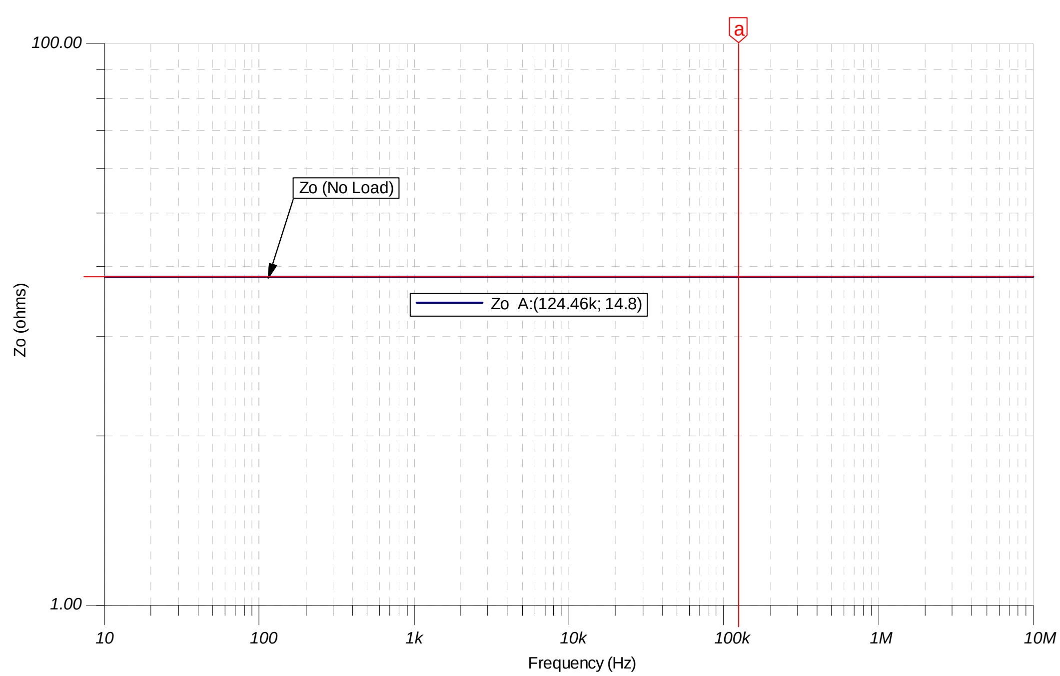



**Fig. 7.11: $Z_O$ Ac Plot, No Load, $I_{OUT}$ = 0 mA**

In Fig. 7.12 we use our emitter-follower $Z_O$ model for the no-load condition. With results from the heavy-load condition fill in values for $R_X$. Derive $K_Z$ based on $Z_O$ at no load assuming that the characteristics of both QP and QM are similar. The derivation (in Fig. 7.12) finds $K_Z$ to be 0.0250668.

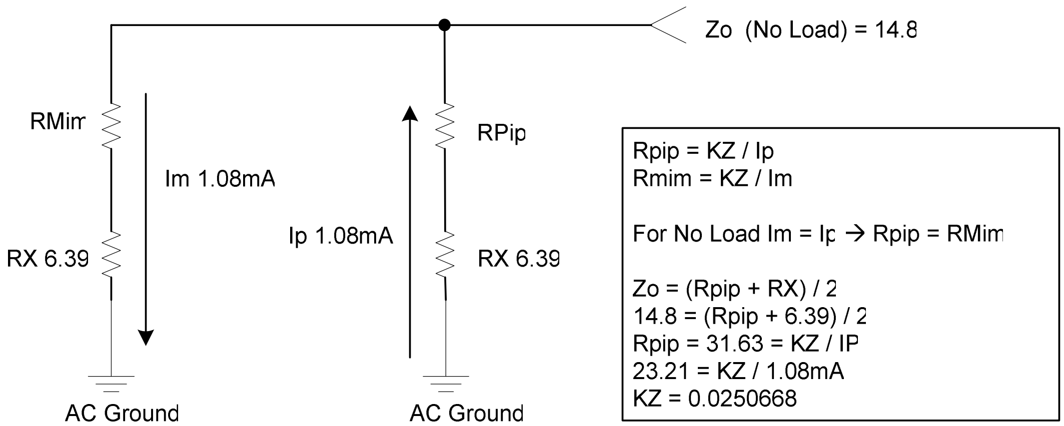
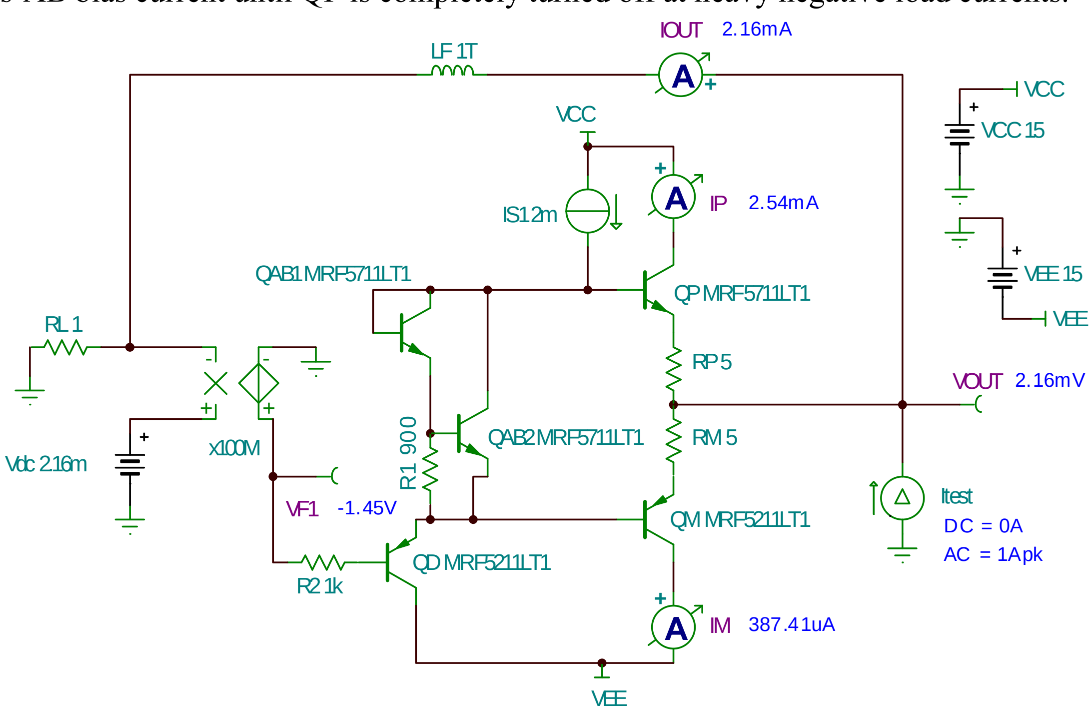



**Fig. 7.12: No-Load $Z_O$ Model**

So now let's test our emitter-follower $Z_O$ model. We will use a dc current out of QP of 2.54 mA (about 2 x $I_{AB}$ -- twice the Class-AB bias current.) This should turn off QM and force $Z_O$ to be dominated by the $R_O$ due to QP and (Fig. 7.13) we see this is approximately true. This is a good illustration as how real world Class-AB bias schemes work. As load current increases positively the entire Class-AB bias current begins to shift into QP. As the load current goes negative, QM begins to receive the entire Class-AB bias current until QP is completely turned off at heavy negative load currents.




**Both QP and QM on and contribute to $Z_O$ but QP dominates due to lowest impedance**

**Fig. 7.13: $Z_O$, Light Load, $I_{OUT}$ = +2x$I_{AB}$ (2.16 mA)**

In our emitter-follower light-load $Z_O$ model (Fig. 7.14) we use our known values of $R_X$ and $K_Z$ to compute the equivalent $Z_O$ we expect and then run our Tina SPICE simulation (results in Fig. 7.15). We expected $Z_O$ at light load to be 13.2326 Ω with Tina SPICE measuring 12.85 Ω. This is close enough to use for any analysis we are interested in. If we took the time to investigate we would find that QP and QM do not have exactly the same characteristics.

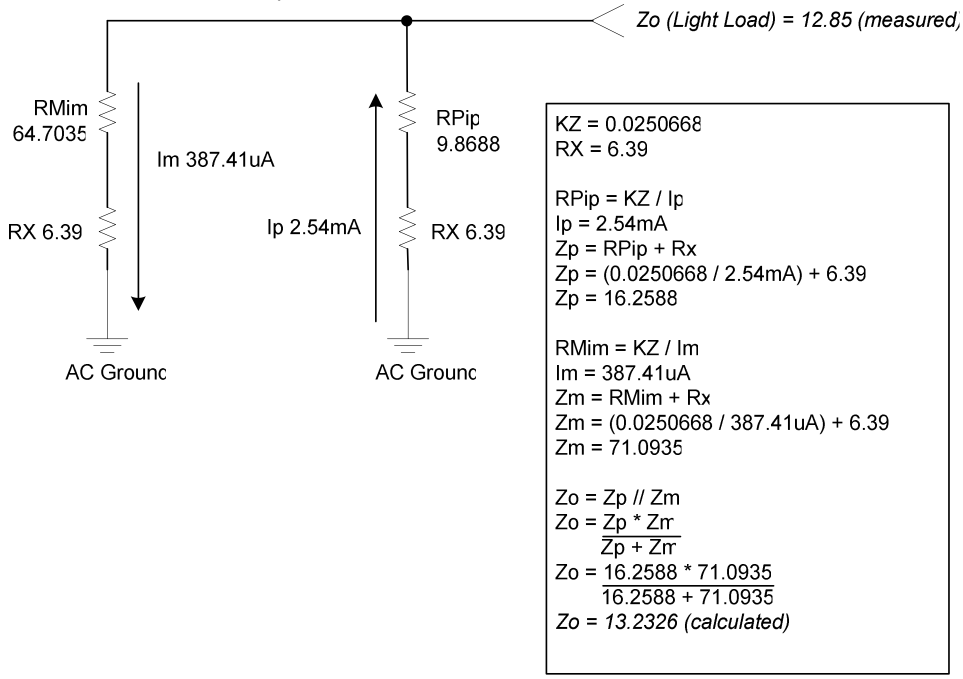



**Fig. 7.14: Light-Load $Z_O$ Model**

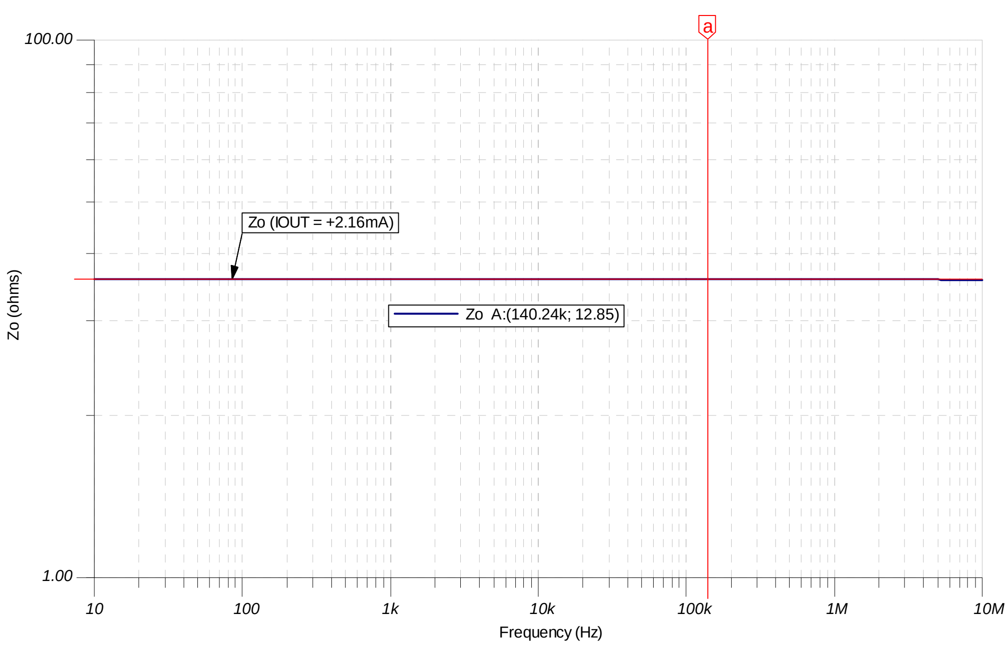



**Fig. 7.15: $Z_O$ Ac Plot, Light Load, $I_{OUT}$ = +2.16 mA**

Now our complete set of curves for emitter-follower $Z_O$ can be constructed (see Fig. 7.16) where $Z_O$ is dominated by $R_O$, constant over the unity-gain bandwidth of the op amp, and $R_O$ goes down with increasing load currents. Notice that $Z_O$ was plotted for both source and sink currents at light load and heavy load with no significant difference in source or sink $Z_O$. These key curves for $Z_O$ should be included in every bipolar emitter follower op amp data sheet.

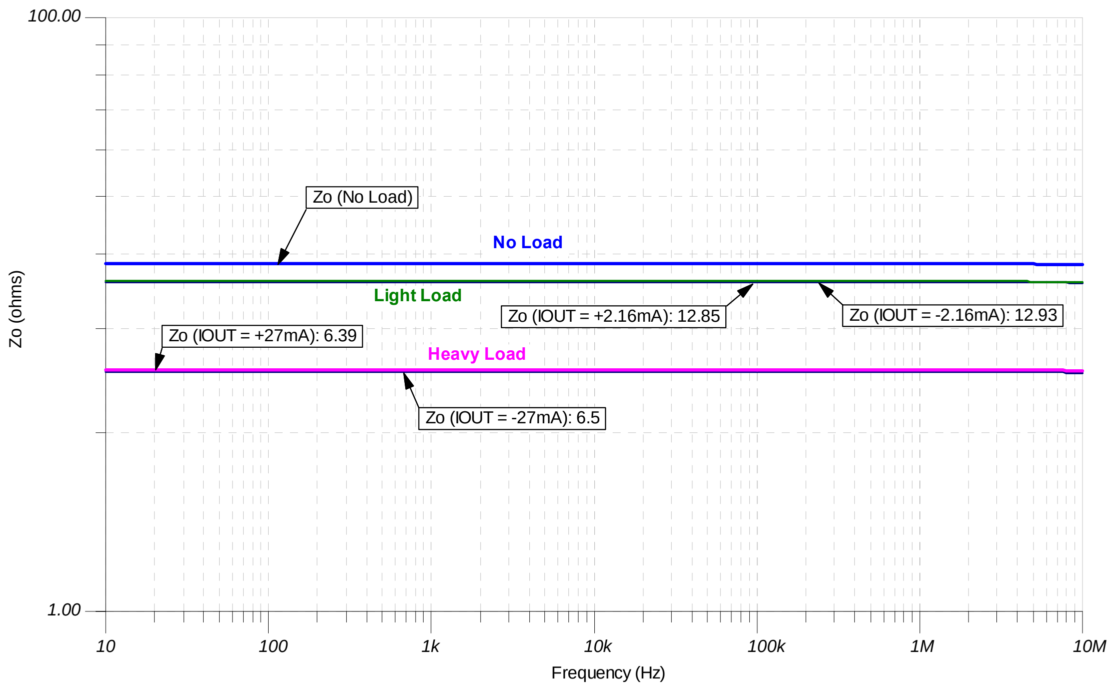
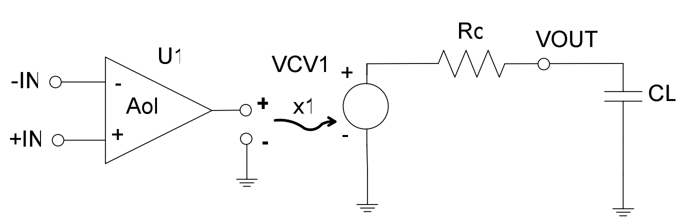



**Fig. 7.16: Complete $Z_O$ Curves: Bipolar Emitter-Follower**

## $Z_O$ And Capacitive Loads For Bipolar, Emitter-Follower Output Op Amps




$$fp2 = \frac{1}{2*\pi*CL*RO}$$

**U1: Op Amp DC and AC Aol Function**
**VCV1: x1 Voltage-Controlled-Voltage-Source**
**Ro: Open Loop AC Small Signal Output Resistance**
**CL modifies Aol Curve.**

**Fig. 7.17: Bipolar Emitter-Follower $Z_O$ and Capacitive Loads**

For capacitance loads on the output of emitter-follower stages we will use the model in Fig. 7.17. We are either given in a data sheet, or can measure, the op amp's Aol curve with no capacitive load. $R_O$ will react with CL and form a second pole, fp2, in the op amp's unloaded Aol curve.

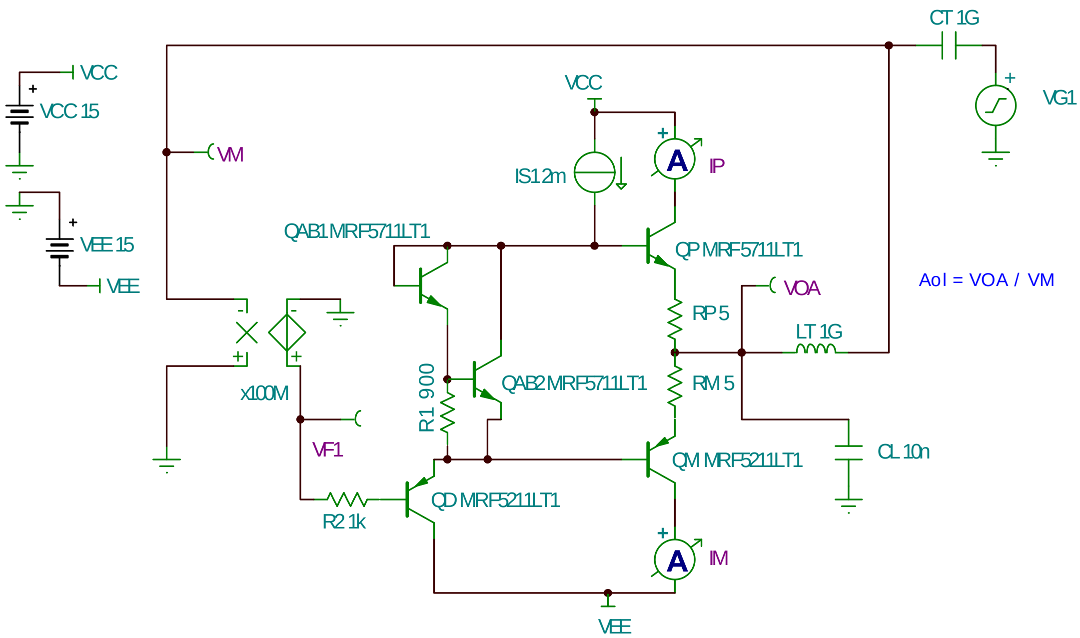



**Fig. 7.18: Tina SPICE Circuit for Modified Aol Measurement**

We will load our emitter-follower bipolar op amp with many different capacitive loads and test it for the location of the additional pole, fp2, due to $R_O$ and CL. Fig. 7.18 uses LT (as a short-circuit) to establish a dc operating point. At any ac frequency of interest LT is open-circuit so we can look at a modified Aol curve. CT is open for dc and a short for any ac frequency of interest and connects the ac test source, VG1, into circuit. By inspection we see that Aol = VOA ÷ VM.

The resultant modified Aol curves due to several different capacitive loads are shown in Fig. 7.19.

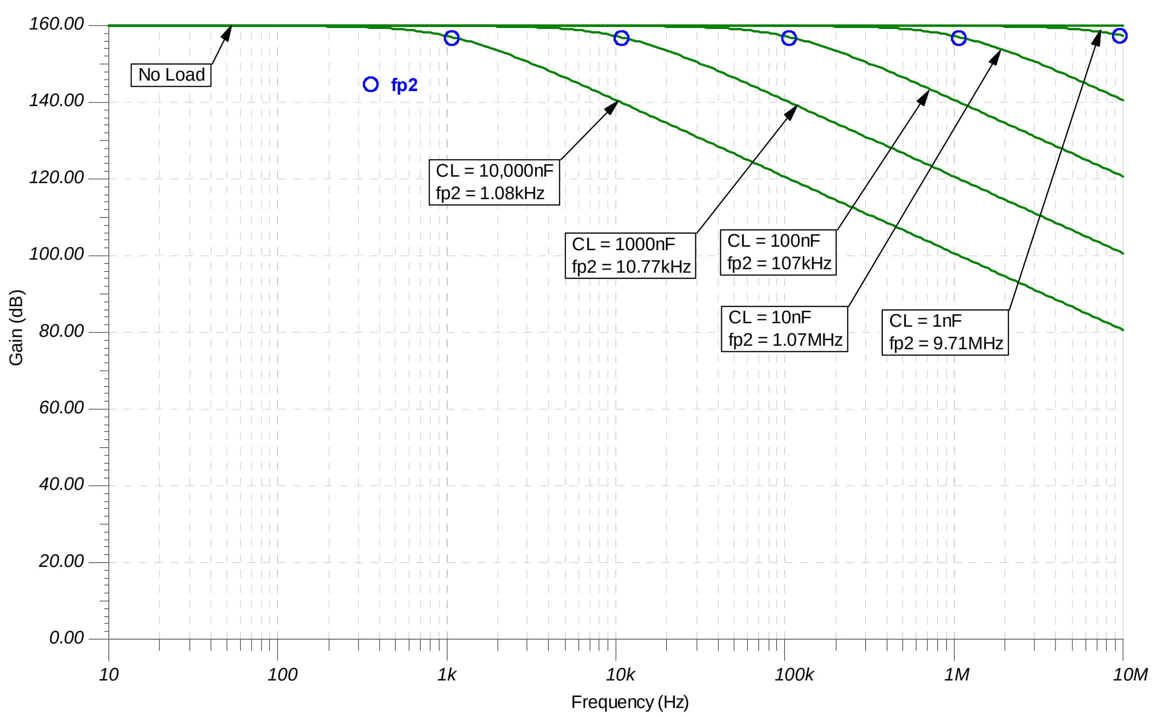



**Fig. 7.19: Modified Aol Curves for Different Values of CL**

Our predicted locations of the pole, fp2, due to $R_O$ and CL, in the modified Aol curve are detailed in Fig. 7.20. Also shown are the actual Tina SPICE measured locations for each respective fp2. For use in stability synthesis techniques there is no significant error between actual and predicted values for fp2.

| **RL** | No Load | | |
|---|---|---|---|
| **Ro** | 14.8 | | |
| | | **Predicted** | **Actual** |
| **CL** | **CL** | **fp2** | **fp2** |
| | (farads) | (Hz) | (Hz) |
| 1nF | 1.00E-09 | 10753712 | 9710000 |
| 10nF | 1.00E-08 | 1075371 | 1070000 |
| 100nF | 1.00E-07 | 107537 | 107000 |
| 1000nF | 1.00E-06 | 10754 | 10770 |
| 10,000nF | 1.00E-05 | 1075 | 1080 |

**Fig. 7.20: fp2 Locations For Different CL: Predicted And Actual**

## $Z_O$ Summary For Bipolar Emitter-Follower Output Op Amps

A summary of the key characteristics of $Z_O$ for a bipolar emitter-follower op amp (Fig. 7.21) show that within the unity-gain bandwidth it is dominated by $R_O$ and is constant with frequency. As dc output load current increases, $R_O$ decreases, making $R_O$ inversely proportional to $I_{OUT}$. Capacitive loads, CL, interact with $R_O$ to form a second pole in the original op amp Aol curve which we can use to help synthesize the proper closed-loop compensation for good stability. $R_O$ does change with process and temperature, but a good rule-of-thumb including those changes is 0.65* $R_O$typ at -55°C to 1.5* $R_O$typ at 125°C, where $R_O$typ is at 25°C. There are always exceptions to the rules-of-thumb we have developed for open-loop output impedance of bipolar emitter-follower op amps. The most complete and accurate data for $Z_O$ should be obtained from the op amp manufacturer or measured.

- **$Z_O$ is Dominated by $R_O$**
- **$Z_O$ is Constant over Op Amp Unity Gain Bandwidth**

- **$Z_O$ is Inversely Proportional to $I_{OUT}$**
- **$R_O$ and CL form a Second Pole to create a Modified Aol**
- **$R_O$ Change with Process and Temperature:**
  - ✓ **$R_O$ @ -55C = 0.65 * $R_O$typ (i.e. 65 ohms)**
  - ✓ **$R_O$ @ 25C = $R_O$typ (i.e. 100 ohms)**
  - ✓ **$R_O$ @ +125C = 1.5 * $R_O$typ (i.e. 150 ohms)**
- **Use $R_O$typ for Stability Synthesis**
  - ✓ **Decade Rules-of-Thumb will provide Design Margin**

**Fig. 7.21: $Z_O$ Summary For Bipolar Emitter-Follower**

## $Z_O$ For CMOS RRO (Rail-to-Rail Output) Op Amps

A typical CMOS RRO op amp topology is shown in Fig. 7.22. With this type of output stage $R_O$ (small-signal, open-loop output resistance) is usually the dominant portion of $Z_O$ (small-signal, open-loop output impedance) at high frequencies. $R_O$ is inversely proportional to dc load current at most currents. However, at light load currents $R_O$ is proportional to dc load currents. At mid and low frequencies $Z_O$ is usually capacitive. The op amp's Aol curve will be affected at low frequencies due to RL (resistive load on output) interacting with the capacitive portion of $Z_O$.

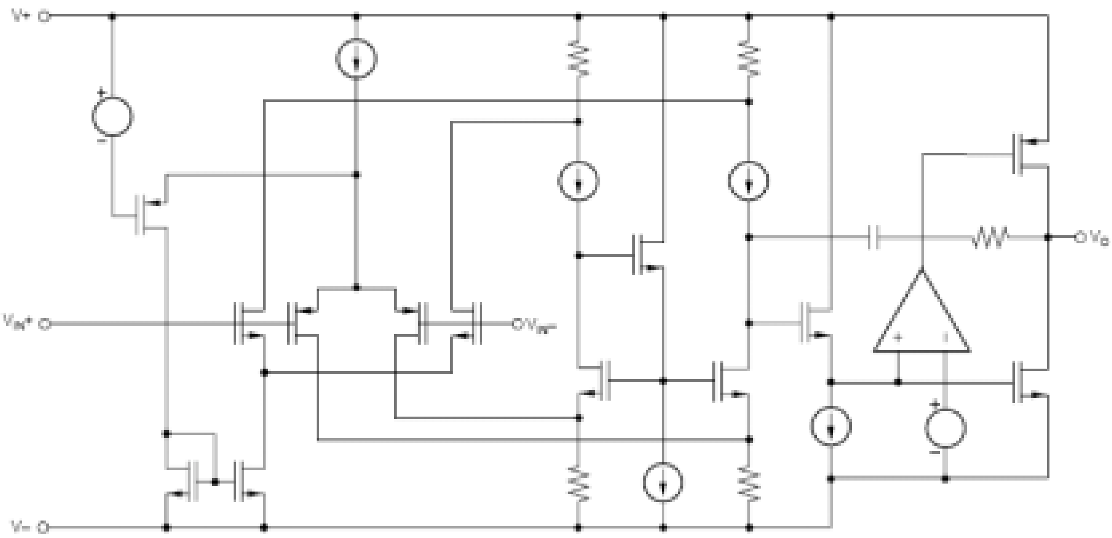



**Fig. 7.22: Typical CMOS RRO Op Amp**

Specifications of an example OPA348 CMOS RRO op amp (also RRI --rail-to-rail input) are listed in Fig. 7.23. The CMOS RRIO (rail-to-rail input/output) topology is ideal for single-supply applications with close swing to the rail on both the input and output, low quiescent current, and low input bias currents. Noise, however, will usually be considerably higher than bipolar emitter–follower op amps.

**OPA348**
**1MHz, 45uA, CMOS, RRIO Operational Amplifier**

| | | | |
|---|---|---|---|
| **Input Specs** | | **AC Specs** | |
| Offset Voltage | 5mV max | Open Loop Gain, RL = 100k | 108dB typ |
| Offset Drift | 4uV/C | Open Loop Gain, RL = 5k | 98dB typ |
| Input Voltage Range | (V-)-0.2V to (V+)+0.2V | Gain Bandwidth Product | 1 MHz |
| Common-Mode Rejection Ratio | 82dB typ | Slew Rate | 0.5V/us |
| Input Bias Current | 10pA max | Overload Recovery Time | 1.6us |
| | | Total Harmonic Distortion + Noise | 0.0023%, f=1kHz |
| | | Setling Time, 0.01% | |
| **Noise** | | **Supply Specs** | |
| Input Voltage Noise | 10uVpp, f=0.1Hz to 10Hz | Specified Voltage Range | 2.5V to 5.5V |
| Input Voltage Noise Density | 35nV/rt-Hz @1kHz | Quiescent Current | 65uA max |
| Input Current Noise Density | 4fA/rt-Hz | Over Temperature | 75uA max |
| **Output Specs** | | **Temperature & Package** | |
| Vsat @ Iout = 27uA | 25mV max | Operating Range | -40C to +125C |
| Vsat @ Iout = 540uA | 125mV max | Package options | SOT23-5, SO-8, SC70-5 |
| Vsat @ Iout = 5mA | 1V max | | |
| Iout Short Circuit | 10mA | | |

**Fig. 7.23: Example Specifications: CMOS RRIO Op Amp**

Fig. 7.24 is a simplified model for a CMOS RRO op amp using a voltage output differential front end which controls a current source, GM2. GM2 drives RO, developing a voltage which controls GMO, the output current source. Capacitor CO feeds back into the RO/GM2 node. From this simplified model we observe that at high frequencies $Z_O = R_O$. As we go from high frequency towards medium and low frequencies we expect to see the effects of CO and will therefore look for $Z_O$ to be capacitive.

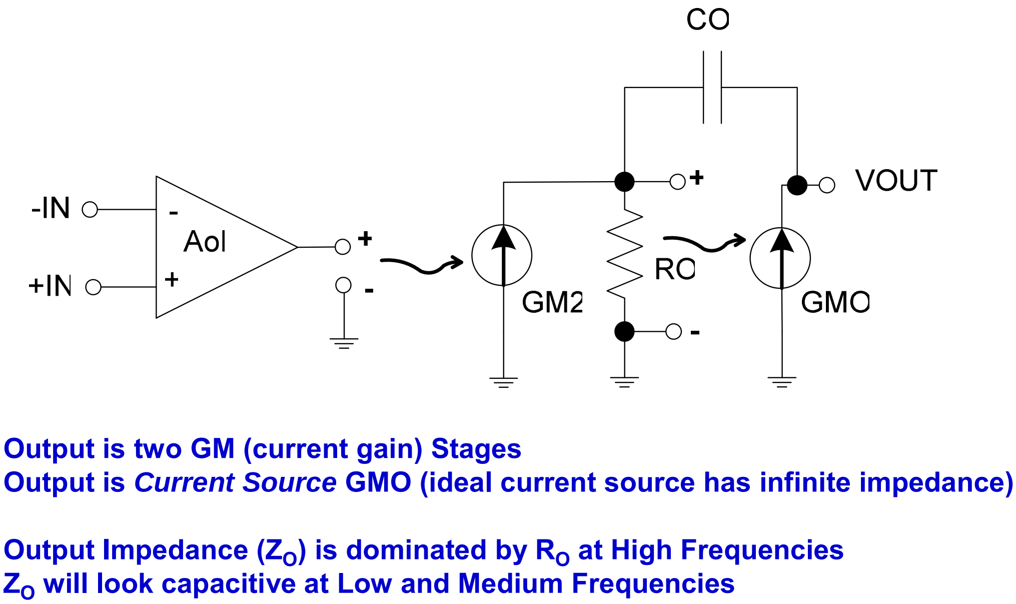



**Fig. 7.24: Simplified Model: CMOS RRO Op Amp**

In most CMOS RRO amplifiers (Fig. 7.25) the Class-AB bias current in the output stage (with no load) is about half of the quiescent current for the entire amplifier. At high frequencies $Z_O = R_O$ and proportional to gm (current transfer ration for MOSFET). But, for MOSFETs, gm is inversely proportional to the square-root of $I_D$ (drain current).

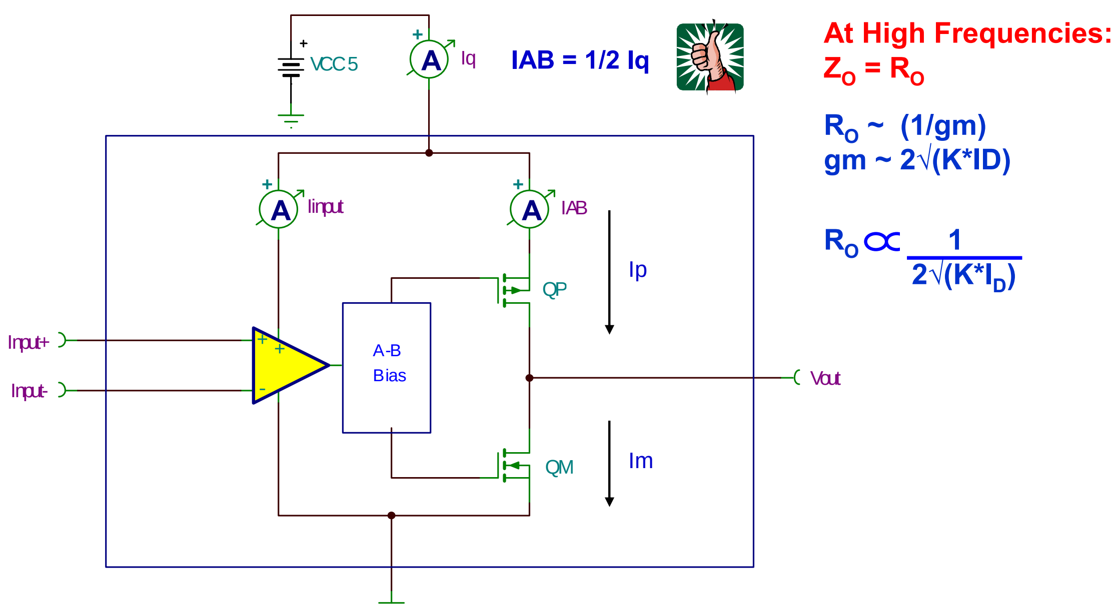



**Fig. 7.25: $Z_O$ Definition: CMOS RRO Op Amp**

Fig. 7.26 details our CMOS RRO $R_O$ model consisting of current-controlled resistors for each half of the push (QP) and pull (QM) output MOSFETs. Each of these resistors, RPip and RMim, are proportional to the square root of the $I_D$ flowing through each respective MOSFET. When looking back into the output terminal of the op amp these two current-controlled resistors appear in parallel for a net value of $R_O$. The equation for the parallel combination of these resistances creates a mathematical equation which yields an unexpected transfer function. For small increases in $I_{OUT}$, $R_O$ will increase until one of the output MOSFETS gets completely turned off and out of Class-AB bias mode.

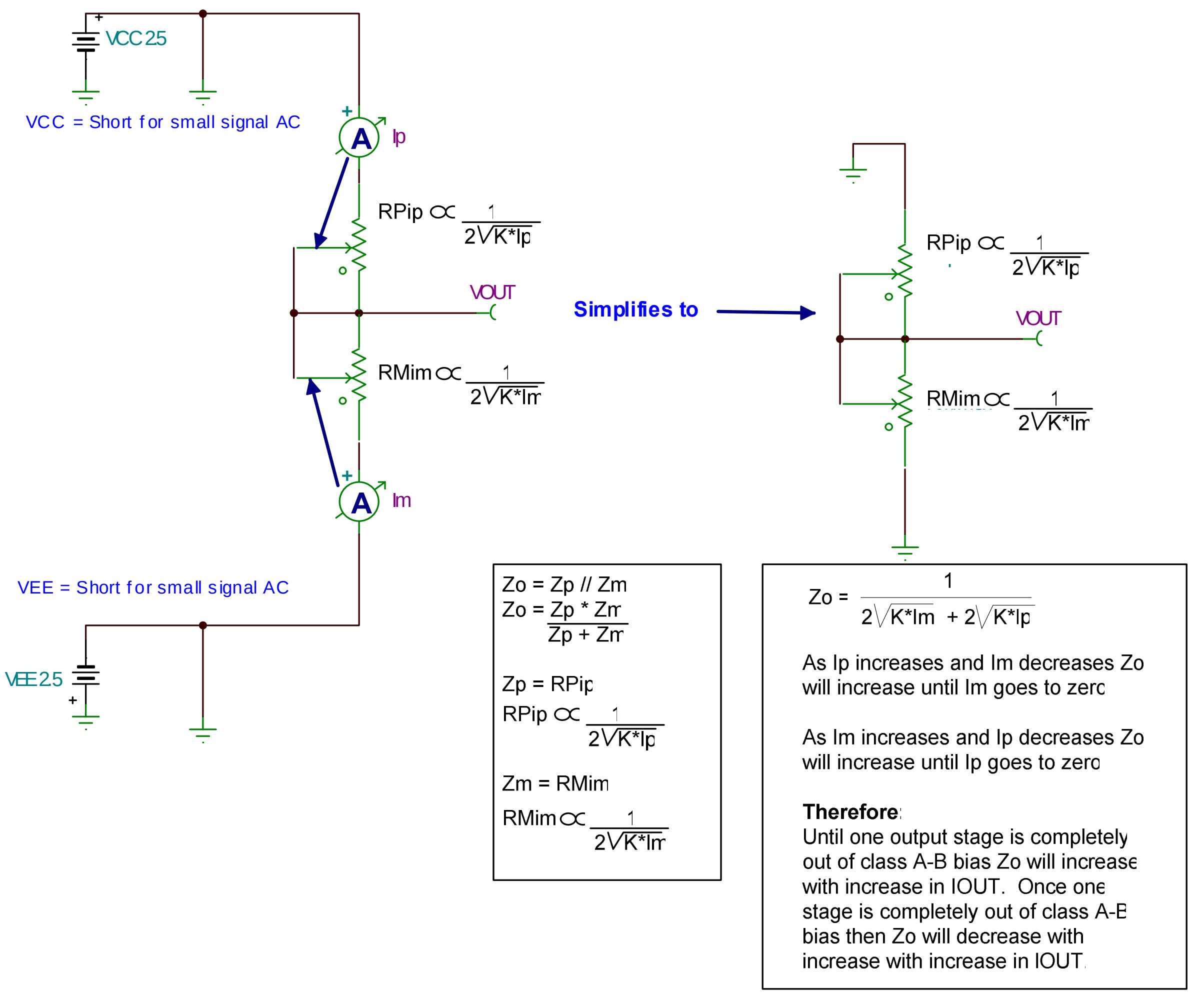



**Fig. 7.26: $R_O$ Model: CMOS RRO Op Amp**

| CMOS RRO Ro Calculator | | | | | |
|---|---|---|---|---|---|
| | | | | | |
| K= | 0.071 | | | | |
| | | | | | |
| *Ip* | **Rp** | *Im* | **Rm** | **Ro** | |
| 2.2000E-05 | 4.0006E+02 | 2.2000E-05 | 4.0006E+02 | 2.0003E+02 | |
| 1.1000E-05 | 5.6578E+02 | 3.3000E-05 | 3.2665E+02 | 2.0709E+02 | |
| 5.5000E-07 | 2.5302E+03 | 4.3450E-05 | 2.8467E+02 | 2.5588E+02 | |
| 5.5000E-08 | 8.0013E+03 | 4.3950E-05 | 2.8305E+02 | 2.7338E+02 | |
| 5.5000E-09 | 2.5302E+04 | 4.3990E-05 | 2.8292E+02 | 2.7979E+02 | |
| ***1.0000E-12*** | ***1.8765E+06*** | ***4.4000E-05*** | ***2.8289E+02*** | ***2.8285E+02*** | ***Ro Max*** |
| 1.0000E-12 | 1.8765E+06 | 8.8000E-05 | 2.0003E+02 | 2.0001E+02 | |
| 1.0000E-12 | 1.8765E+06 | 1.7600E-04 | 1.4144E+02 | 1.4143E+02 | |
| 1.0000E-12 | 1.8765E+06 | 3.5200E-04 | 1.0002E+02 | 1.0001E+02 | |

**Fig. 7.27: Example Of $R_O$ Increasing/Decreasing Characteristic**

The example calculation (Fig. 7.27) shows the unique relationship of $R_O$ for small changes in $I_{OUT}$. We see a 200 Ω $R_O$ when both devices have equal current flowing through QP and QM (22 µA) in the Class-AB bias mode. As Im increases, indicating $I_{OUT}$ is increasing in output current sunk, QP receives less and less current until it is essentially turned off at Im = 44 µA. It is at this point that we see $R_O$ at a maximum ($R_O$ Max = 282.25 Ω). For higher $I_{OUT}$ currents $R_O$ will decrease.

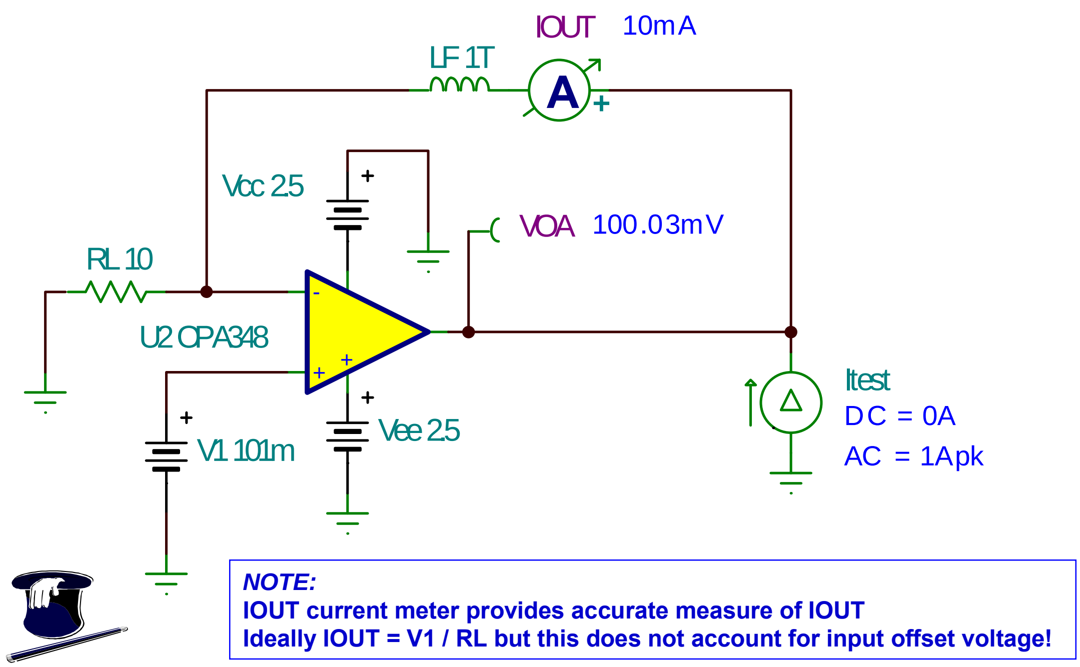



**Fig. 7.28: $Z_O$, Heavy Load, $I_{OUT}$ = +10 mA**

The OPA348 chosen to investigate CMOS RRO $Z_O$ has an extremely accurate SPICE macro-model and the $Z_O$ characteristics were confirmed through lab bench testing. Tina SPICE allows us a convenient way to look at the characteristics of $Z_O$ with our first $Z_O$ measurement at the maximum load current of 10 mA. The current meter, IOUT, in our test circuit (Fig. 7.28) ensures that we control the dc value of $I_{OUT}$ to be exactly 10mA. Simply dividing V1 by RL does not exactly account for the input offset voltage characteristics of the op amp, which may add an unacceptable error.

The ac plot of $Z_O$ for $I_{OUT}$ of 10 mA (Fig. 7.29) has a high-frequency $R_O$ component of 34.79 Ω and $Z_O$ is clearly capacitive for frequencies lower than about 10 kHz. We expect at this output current for $R_O$ to be the lowest we will see since QM is entirely off, and QP is conducting all the output stage current.

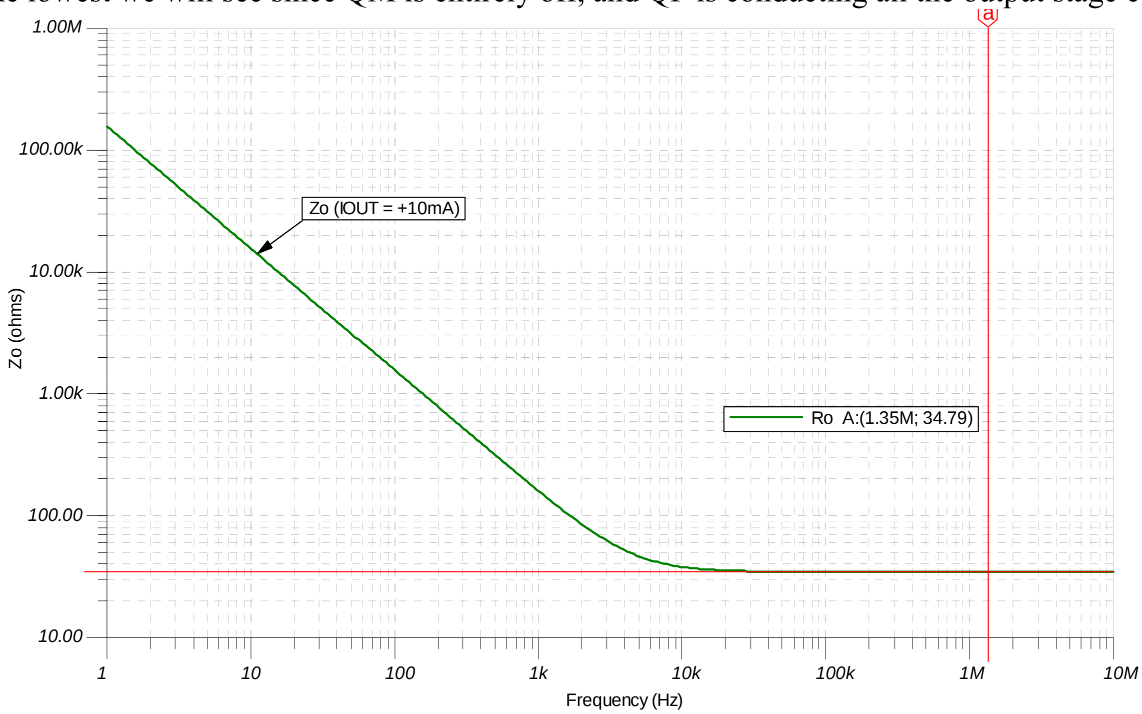



**Fig. 7.29: $Z_O$ Ac Plot, Heavy Load, $I_{OUT}$ = +10 mA**

Our heavy-load $R_O$ model (Fig. 7.30) confirms that at this output current $R_O$ should be the lowest since QM is entirely off and QP has all output stage current flowing through it.

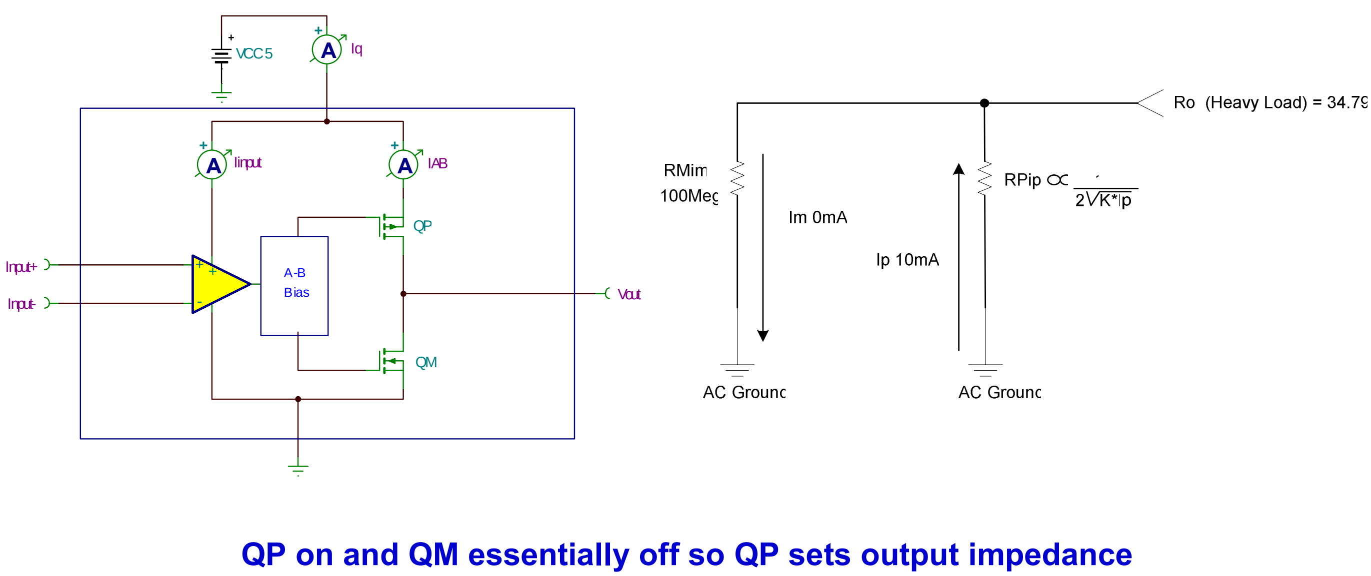



**Fig. 7.30: Heavy-Load $R_O$ Model**

Our no-load $Z_O$ curve will be computed using the circuit in Fig. 7.31. From our rule-of-thumb for $I_Q$ Vs $I_{AB}$ we would guess that since $I_Q = 45\ \mu A$, then $I_{AB} = 22.5\ \mu A$ for the OPA348. Our error current of 483.65 fA should not contribute any significant error for our no load $Z_O$ curve.

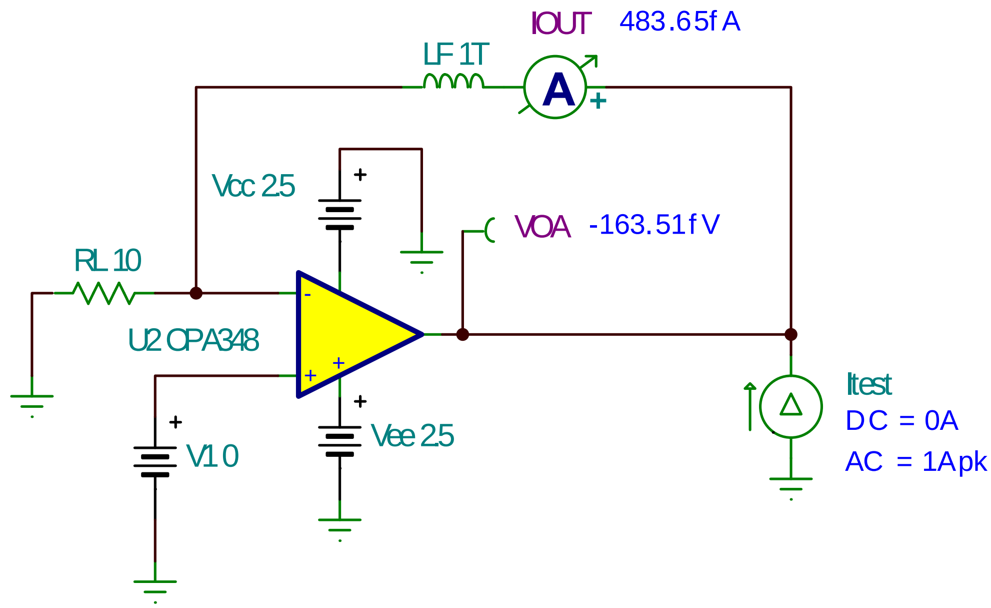



**Fig. 7.31: $Z_O$, No Load, $I_{OUT}$ = 0 mA**

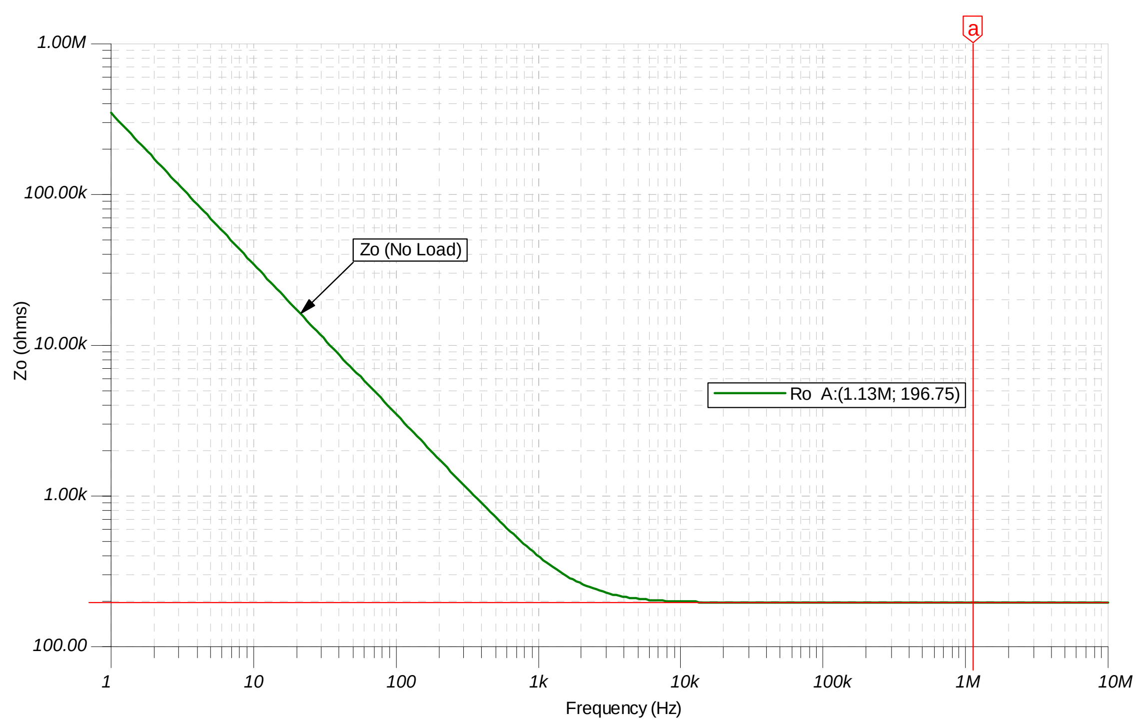
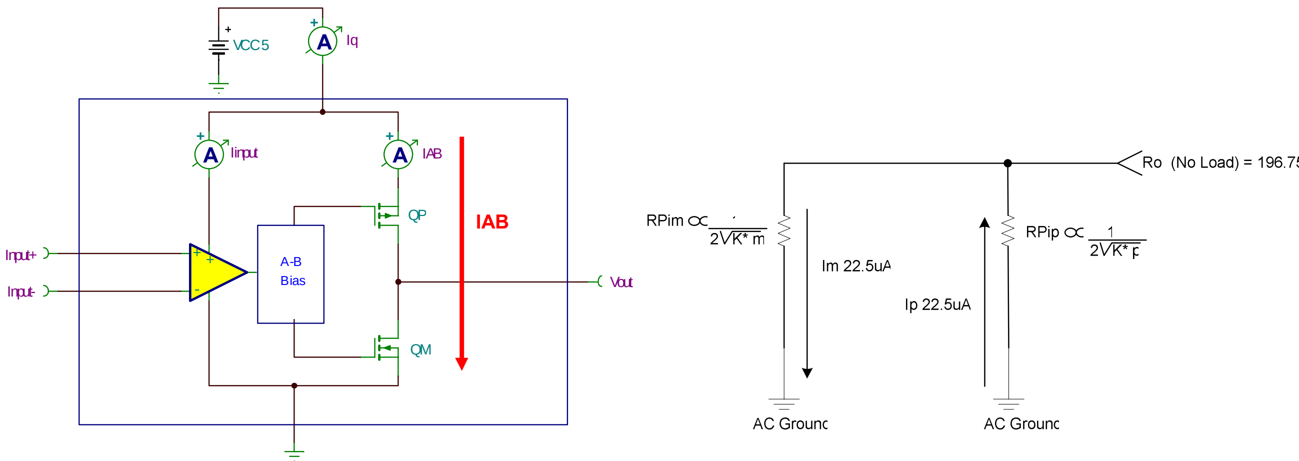



**Fig. 7.32: $Z_O$ Ac Plot, No Load, $I_{OUT}$ = 0 mA**

For $I_{OUT}$ of 0 mA (Fig. 7.32) $Z_O$ has a high-frequency $R_O$ component of 196.75 Ω. $Z_O$ is clearly capacitive for frequencies lower than about 3 kHz.




**QP and QM are equally biased on and contribute equally to $R_O$**

**Fig. 7.33: No-Load $R_O$ Model**

Our no-load $R_O$ model (Fig. 7.33) shows that inside the OPA348 both output devices, QP and QM, are contributing equally to $R_O$. It also shows an assumed Class-AB bias current of 22.5 µA.

We now know what $Z_O$ is for heavy load and no load. The other key curve we are interested in is light load where $R_O$ becomes biggest but we do not know exactly where this operating point is, not being able to see inside the bias stage, so we need to find this point before we compute an ac transfer curve (Fig. 7.34). Running the analysis/calculate ac nodal voltages analysis continuously, as shown, we vary the value of V1 and get an instant update on VOA -- an rms reading. Setting IG1 to 1 A, ac generator, and f = 1 MHz (well inside the frequency area where $R_O$ dominates $Z_O$). Finding a value for V1 that yields maximum VOA we can use it to run our ac transfer curves. With VOA an rms reading it includes any dc component which, for our current levels, would be down in the 7.35 µVrms region -- insignificant when compared to VOA in the 254.56 Vrms region. We expect for this light load that the ac magnitude value for $R_O$ will be 254.56 Vrms ÷ 0.707 Arms = 360 Ω (for sine waves).

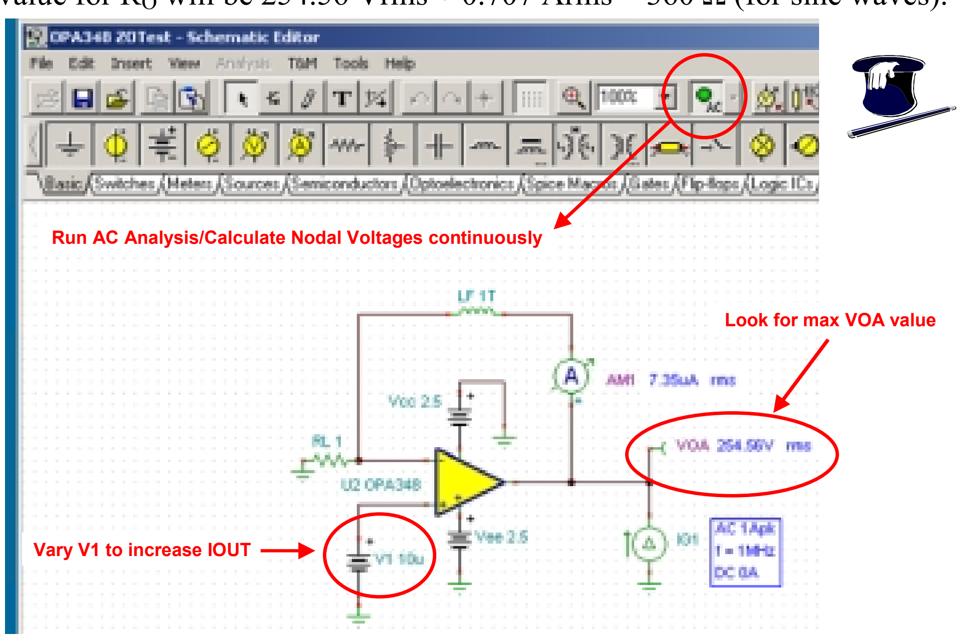



**Fig. 7.34: Light-Load Search For Max $R_O$**

Our $Z_O$ light-load test circuit is shown Fig. 7.35.

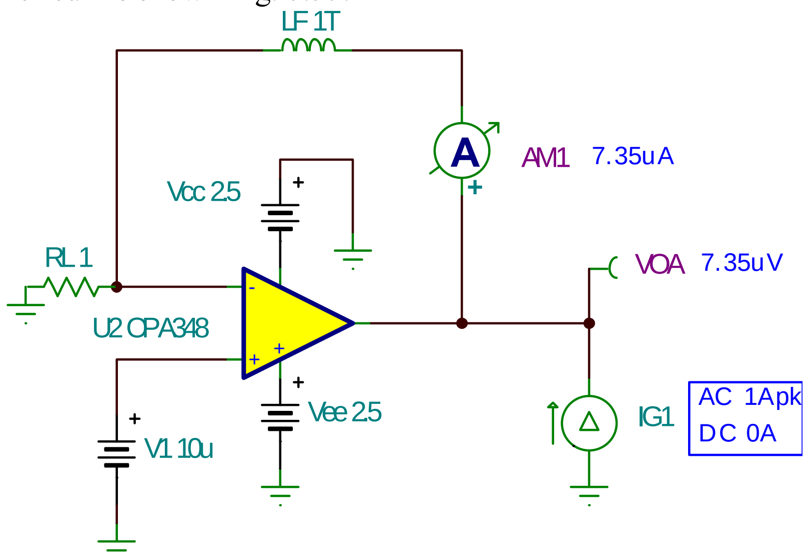



**Fig. 7.35: $Z_O$, Light Load, $I_{OUT}$ = +7.35 µA**

Results of our $Z_O$ light-load ac transfer function analysis are in Fig. 7.36. We see an $R_O$ value of 360 Ω which is what we had predicted and, below about 3 kHz, $Z_O$ is capacitive.

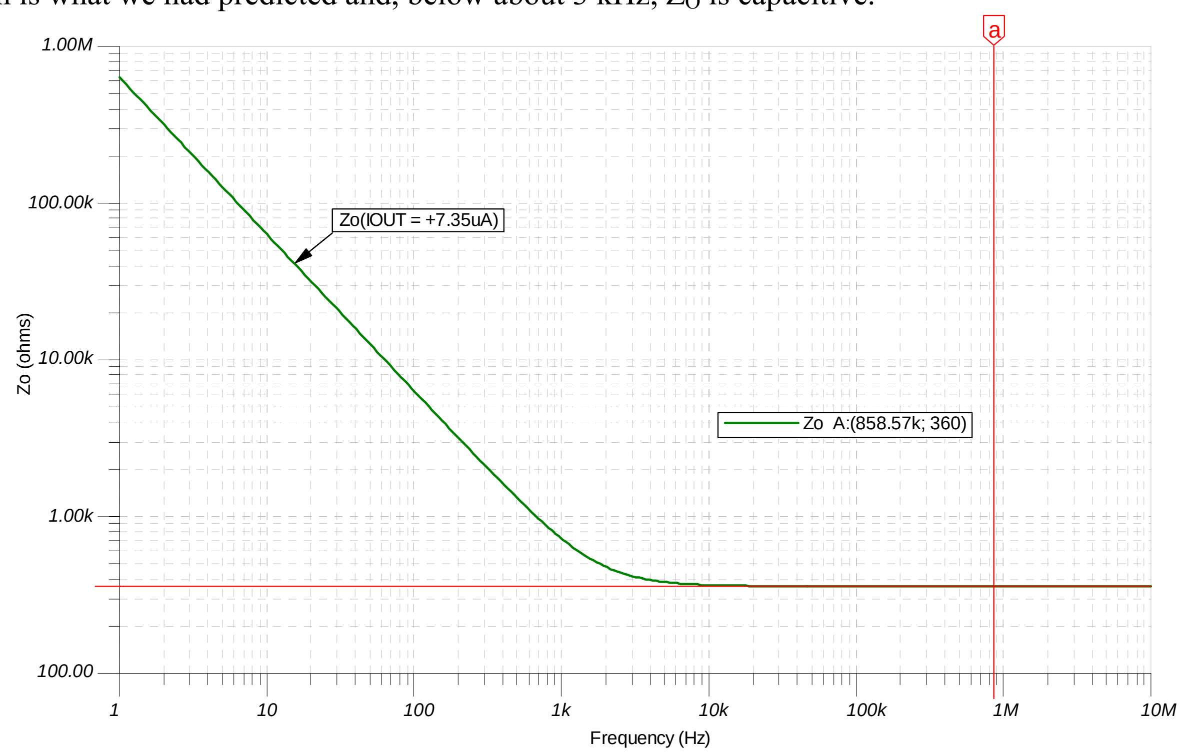
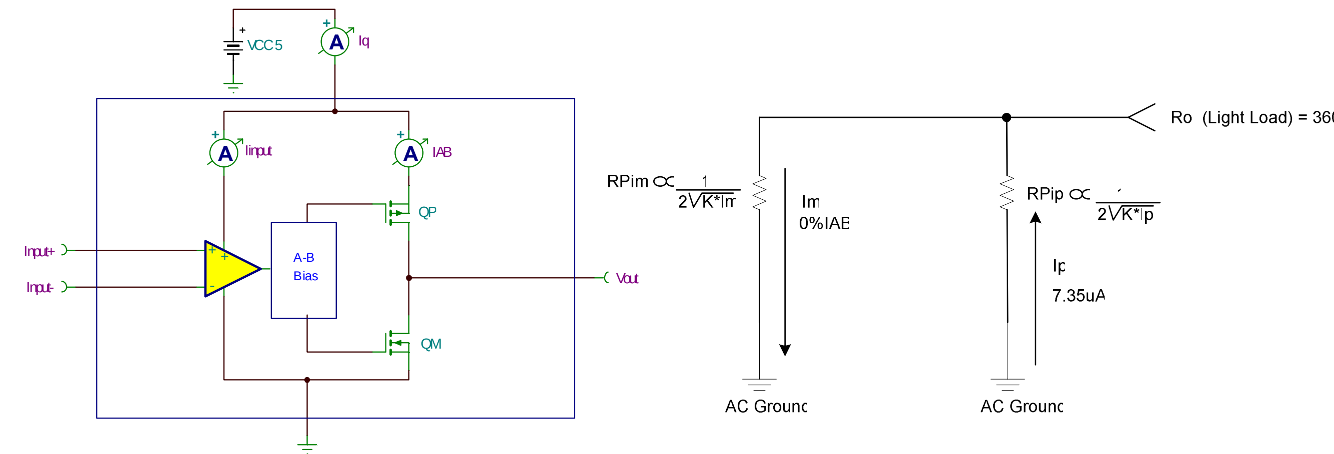



**Fig. 7.36: $Z_O$ Ac Plot, Light Load, $I_{OUT}$ = +7.35 µA**

For our light load model (see Fig. 7.37) we see that QP is on and QM is just off and so QP will set the value of $R_O$ since it will be the lowest impedance. We also see that our original assumption of Class-AB bias being 22.5 µA is probably not correct since it only took 7.35 µA of load current to turn off QM. IAB is probably not much greater than 7.35 µA.




**QP on and QM just off so QP dominates due to lowest impedance**

**Fig. 7.37: Light-Load $Z_O$ Model**

Our complete set of key $Z_O$ curves for OPA348 (Fig. 7.38) show our interest in:

- $I_{OUT}$ = +7.35 µA ($R_O$ = 360 Ω → $R_O$ max)
- $I_{OUT}$ = no load ($R_O$ = 196.75 Ω → $R_O$ no load)
- $I_{OUT}$ = +87.4 µA ($R_O$ = 198.85 Ω) $I_{OUT}$ at which $R_O$ about equals $R_O$ no load
- $I_{OUT}$ > 87.4 µA result in $R_O$ < $R_O$ no load
- $I_{OUT}$ = +10 mA ($R_O$ = 34.79 Ω)

The remaining curves verify that operating conditions in between will also give results which fall in between. In addition, $Z_O$ curves were taken for negative values of $I_{OUT}$ and were so close to laying on the positive values that they were omitted for clarity. These curves should be in all data sheets.

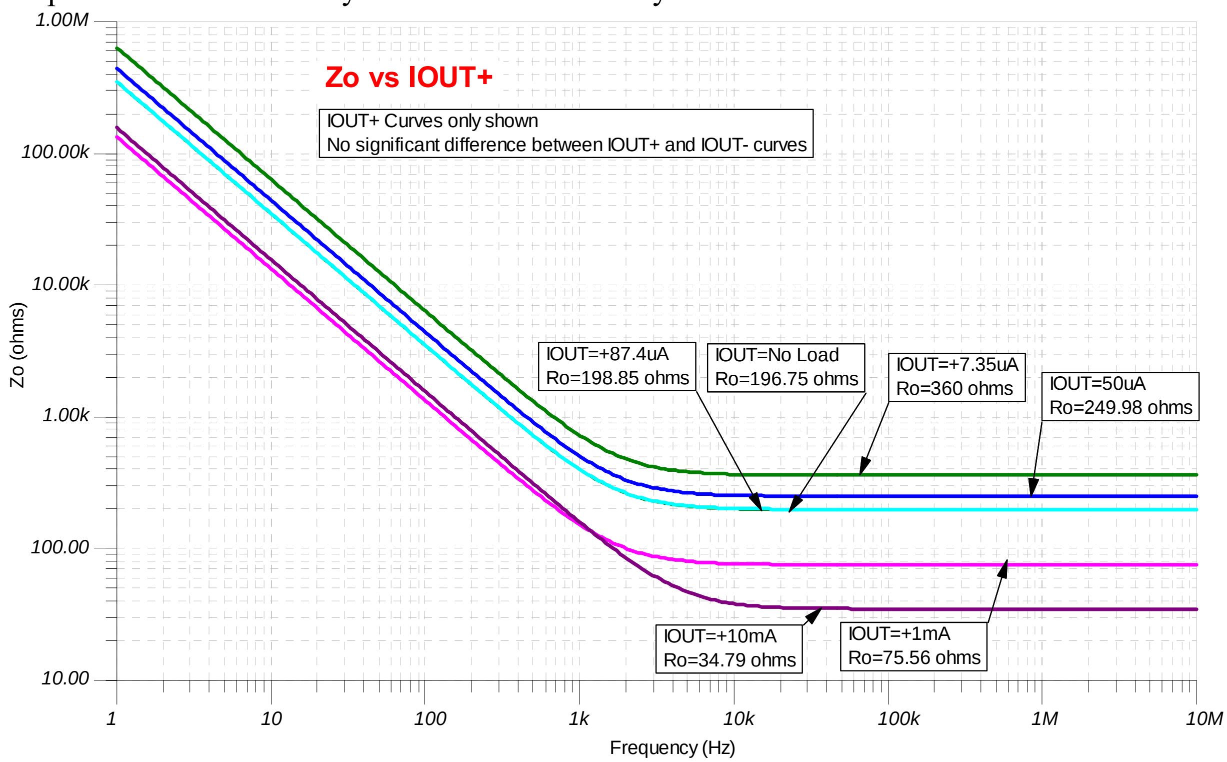



**Fig. 7.38: Complete $Z_O$ Curves: CMOS RRO**

For an equivalent $Z_O$ model for CMOS RRO op amps we analyze the breakpoint, fz, on our $Z_O$ curves (see Fig. 7.39 for heavy and no loads). This, with $R_O$, allows us to determine a value for CO.

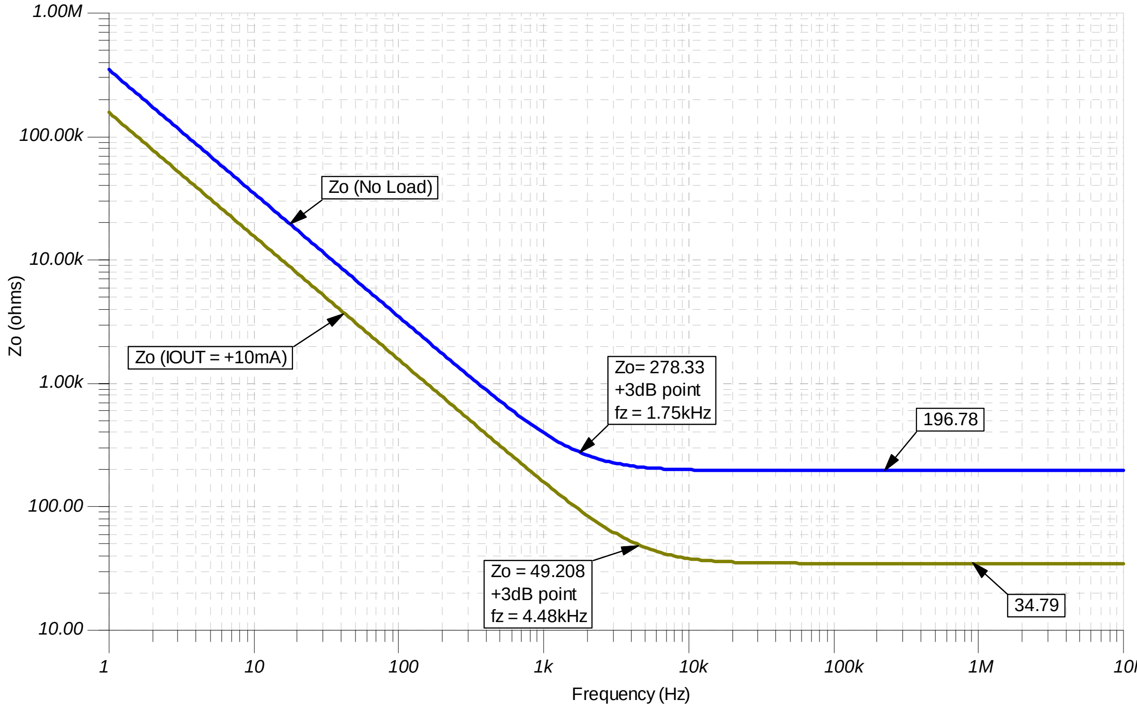
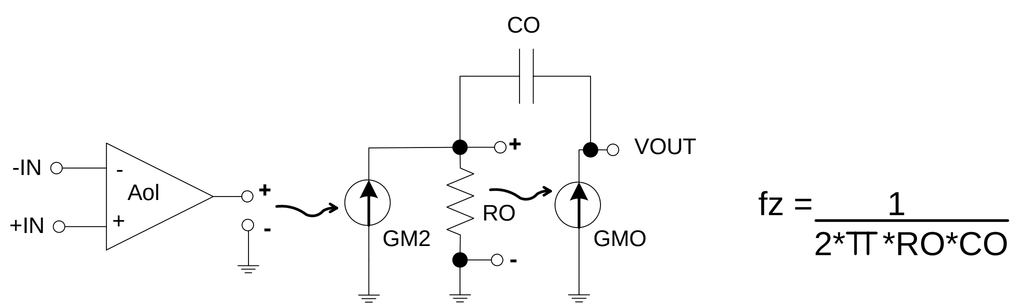



**Fig. 7.39: fz Breakpoints On $Z_O$ Curves**

From our $Z_O$ plots we now complete our model at $I_{OUT}$ no load and heavy load (10 mA) -- Fig. 7.40.

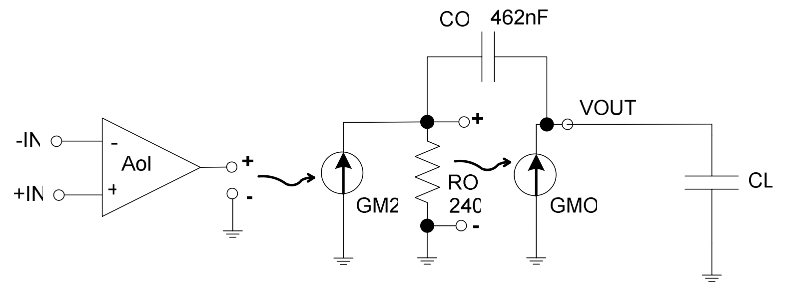



| | fz | RO | CO |
|---|---|---|---|
| No Load | 1.75kHz | 196.78 ohms | 0.4622uF |
| Heavy Load | 4.48kHz | 34.79 ohms | 1.0211uF |

**Fig. 7.40: $Z_O$ Complete Model Calculations**

## $Z_O$ And Capacitive Loads For CMOS RRO Op Amps

For creating modified Aol curves from the original op amp Aol, when we are driving capacitive loads, the load capacitor, CL, will be in series with our $Z_O$ model capacitor, CO. Remember that capacitors in series are like resistors in parallel. And so, if CL < CO, CL will dominated and then if CL > CO, CO will dominate. The modified Aol curve second pole, fp2, will depend directly on $R_O$ and Ceq, the equivalent capacitance due to CO and CL. Fig. 7.41 illustrates these key points.




$$fp2 = \frac{1}{2*\pi*Ceq*RO}$$

CL<462nF CL dominates: Ceq $\approx$ CL
CL>462nF CO dominates: Ceq $\approx$ CO

$$\text{where: } Ceq = \frac{CO * CL}{CO + CL}$$

remember:
1) capacitors in series are like resistors in parallel
2) XC = 1/sC
3) XCeq = 1/sCO +1/sCL
4) Ceq = 1/XCeq

**Fig. 7.41: Modified Aol fp2 Calculations**

In our test circuit to plot modified Aol curves due to capacitive loading on the CMOS RRO op amp, OPA348 (Fig. 7.42) the ac loop is opened by LT, but a short for the dc operating point calculation. CT is open for dc but short for any ac frequency of interest. The modified Aol curve will be VOA ÷ VM.

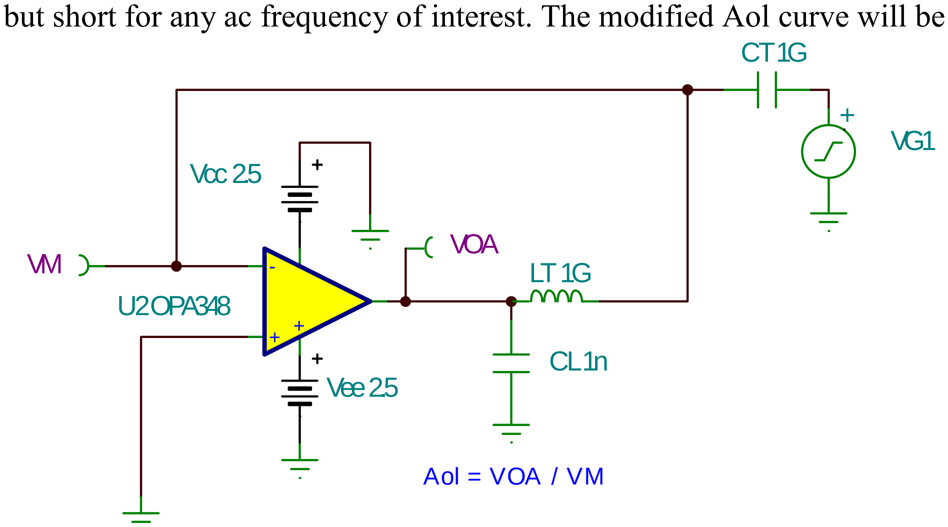



**Fig. 7.42: Modified Aol Test Circuit**

Our actual modified Aol curves for CL from no load to 10,000 nF are seen in Fig. 7.43. The respective locations of fp2 were measured as noted.

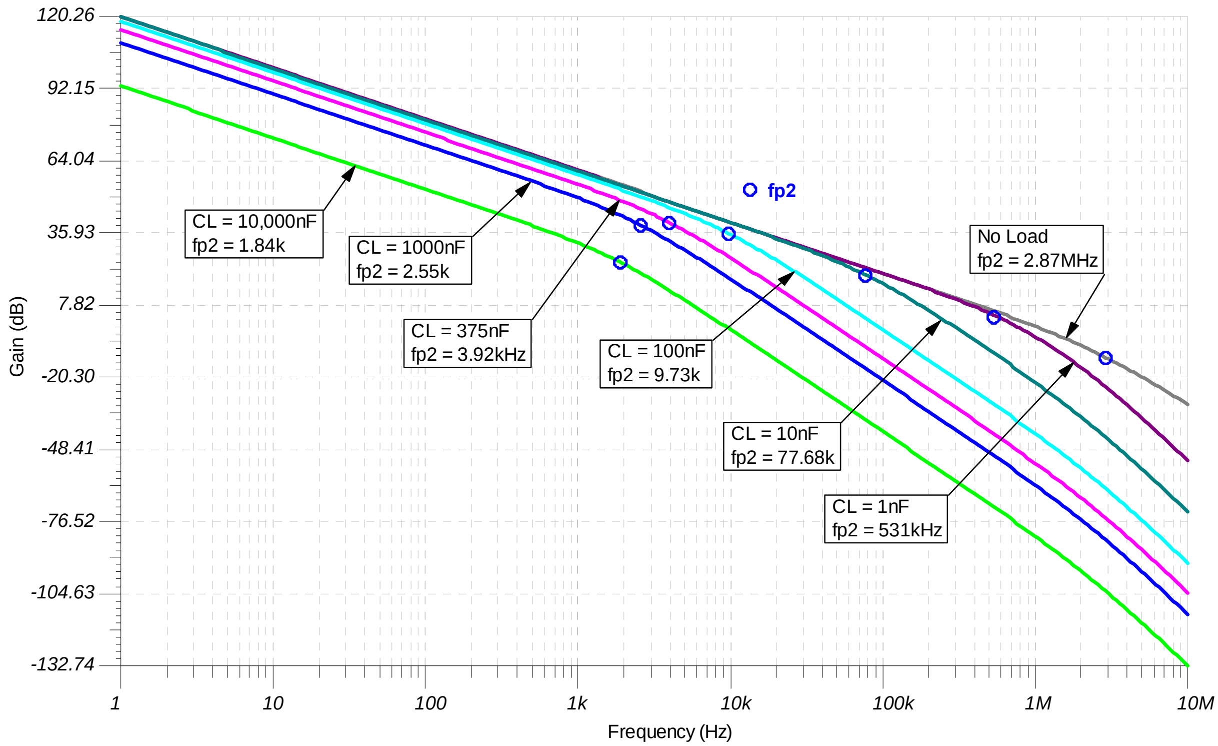



**Fig. 7.43: Modified Aol Curves Due To CL**

Now the measured values of fp2 were compared to the predicted values form our $Z_O$ model (Fig. 7.44). Results are very good, giving us the confidence to use our $Z_O$ model to predict actual modified Aol plots. Note the 1 nF load predicted was off quite a bit due to the fact that we did not include the effect of the OPA348 Aol's second high-frequency pole at 2.87 MHz. The other fp2 locations due to CL were at least a decade away and so the OPA348 Aol second pole has no effect on our predictions.

| | | | | | |
|---|---|---|---|---|---|
| **RO** | 196.78 | | | | |
| **CO** | 4.62E-07 | | | | |
| **RL** | No Load | | | | |
| | | | | **Predicted** | **Actual** |
| **CL** | **CL** | **CO** | **Ceq** | **fp2** | **fp2** |
| | (farads) | (farads) | (farads) | (Hz) | (Hz) |
| No load | No Load | 4.62E-07 | | | 2870000 |
| 1nF | 1.00E-09 | 4.62E-07 | 9.98E-10 | 810546 | *531000 |
| 10nF | 1.00E-08 | 4.62E-07 | 9.79E-09 | 82630 | 77680 |
| 100nF | 1.00E-07 | 4.62E-07 | 8.22E-08 | 9838 | 9730 |
| 375nF | 3.75E-07 | 4.62E-07 | 2.07E-07 | 3907 | 3920 |
| 1000nF | 1.00E-06 | 4.62E-07 | 3.16E-07 | 2559 | 2550 |
| 10,000nF | 1.00E-05 | 4.62E-07 | 4.42E-07 | 1831 | 1840 |

*Actual reflects effect of Op Amp Aol second pole

**Fig. 7.44: Modified Aol fp2 Comparison: Predicted Vs Actual**

## Low Frequency Effects of RL on CMOS RRO Op AMP Aol

Just when we thought we were done with CMOS RRO op amps… CMOS RRO op amps also exhibit another Aol phenomena at low frequencies. The interaction of CO with RL creates a high-pass filter which tends to flatten the low-frequency portion of the Aol curve as shown in Fig. 7.45.

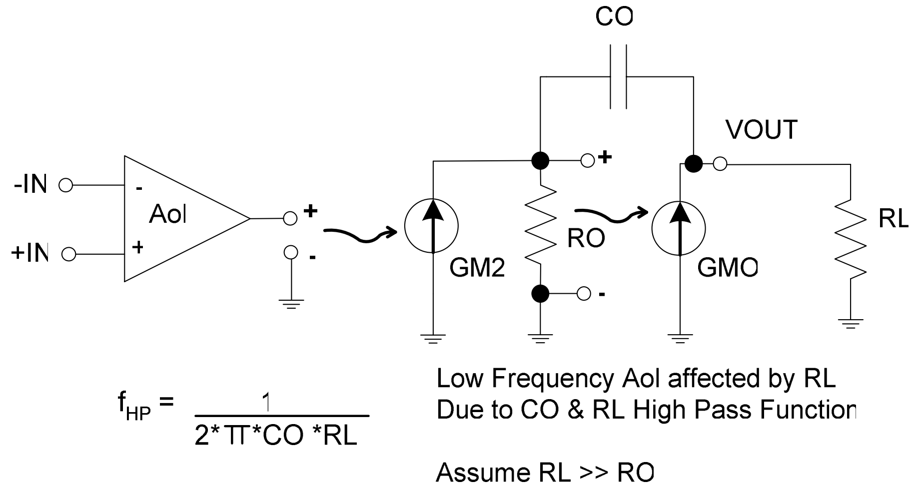



**Fig. 7.45: Aol Low-Frequency Effects of RL**

In our test circuit (Fig. 7.46) the effects of changing RL on the Aol curve can be analyzed.

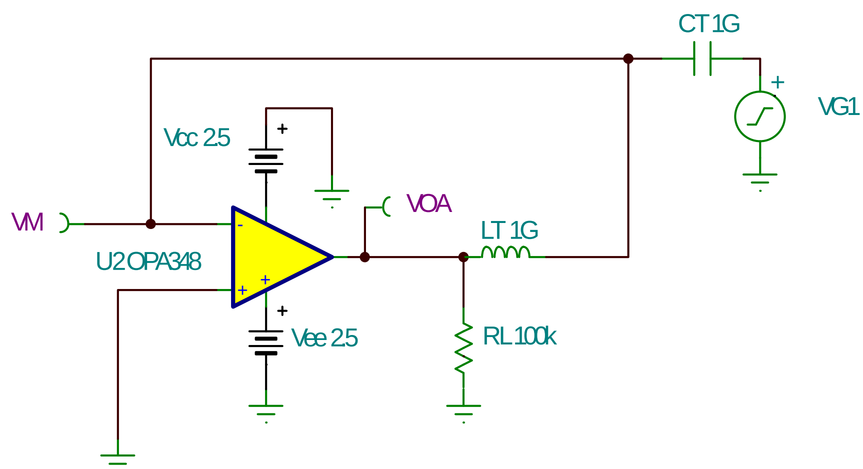



**Fig. 7.46: Aol Low-Frequency Effects Of RL Test Circuit**

Fig. 7.47 shows the low-frequency Aol effects due to resistive loading of no load, 100 kΩ and 5 kΩ.

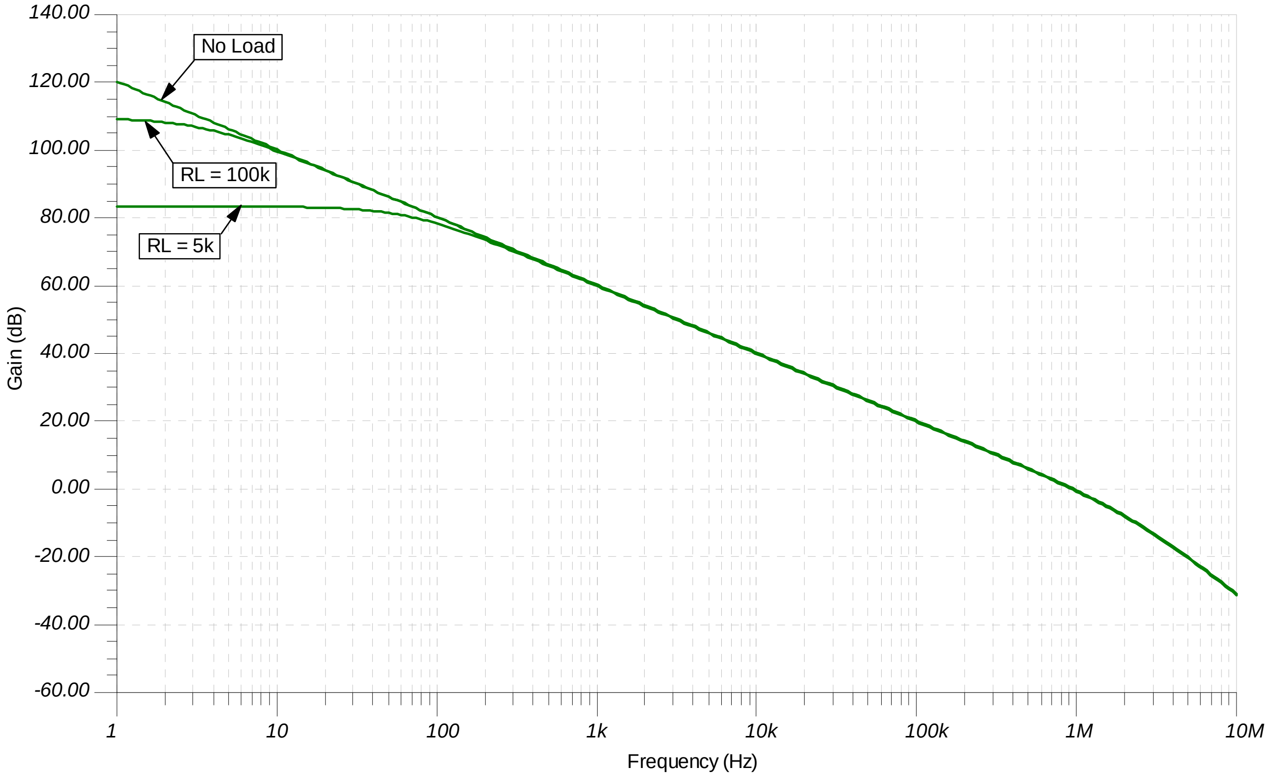



**Fig. 7.47: Ac Plot Of RL Effects On Low-Frequency Portion Of Aol**

A clever test circuit (Fig. 7.48) will allow us to see clearly the effects of CO and RL on the low-frequency portion of the CMOS RRO Aol curve. Vaol represents the unloaded, unmodified Aol curve. VHP is the high-pass filter function created by CO and RL and VOA is the modified Aol curve caused by passing the unmodified Aol curve thought the filter.

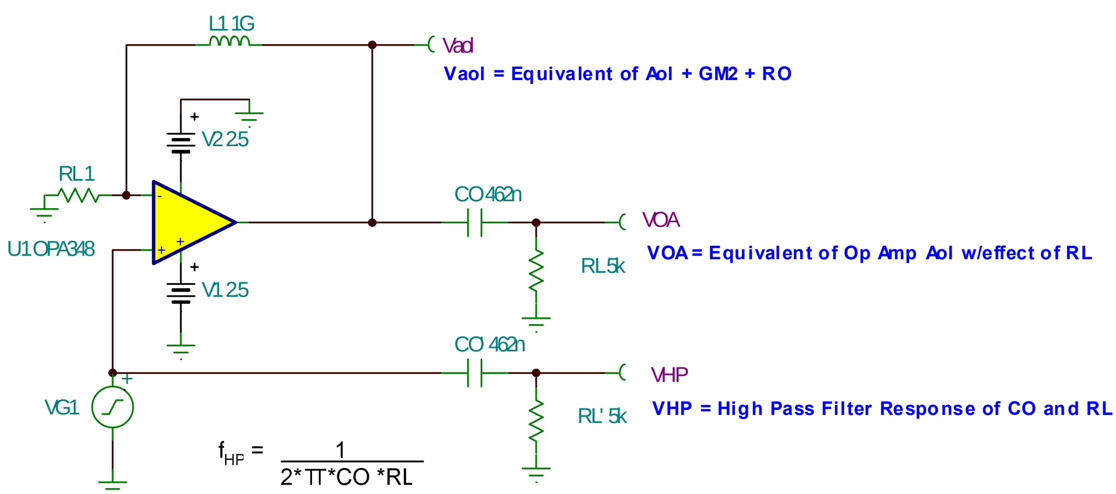



**Fig. 7.48: Equivalent Circuit To Evaluate RL Effects On Aol**

For RL = 5 kΩ our resultant ac curves (Fig. 7.49) show the unmodified Aol curve, Vaol, the high-pass filter effect due to CO and RL, and the net transfer function, modified Aol curve VOA due to passing Vaol through VHP. Since addition on a Bode plot is equivalent to linear multiplication we can easily add Vaol to VHP to see the resultant VOA curve.

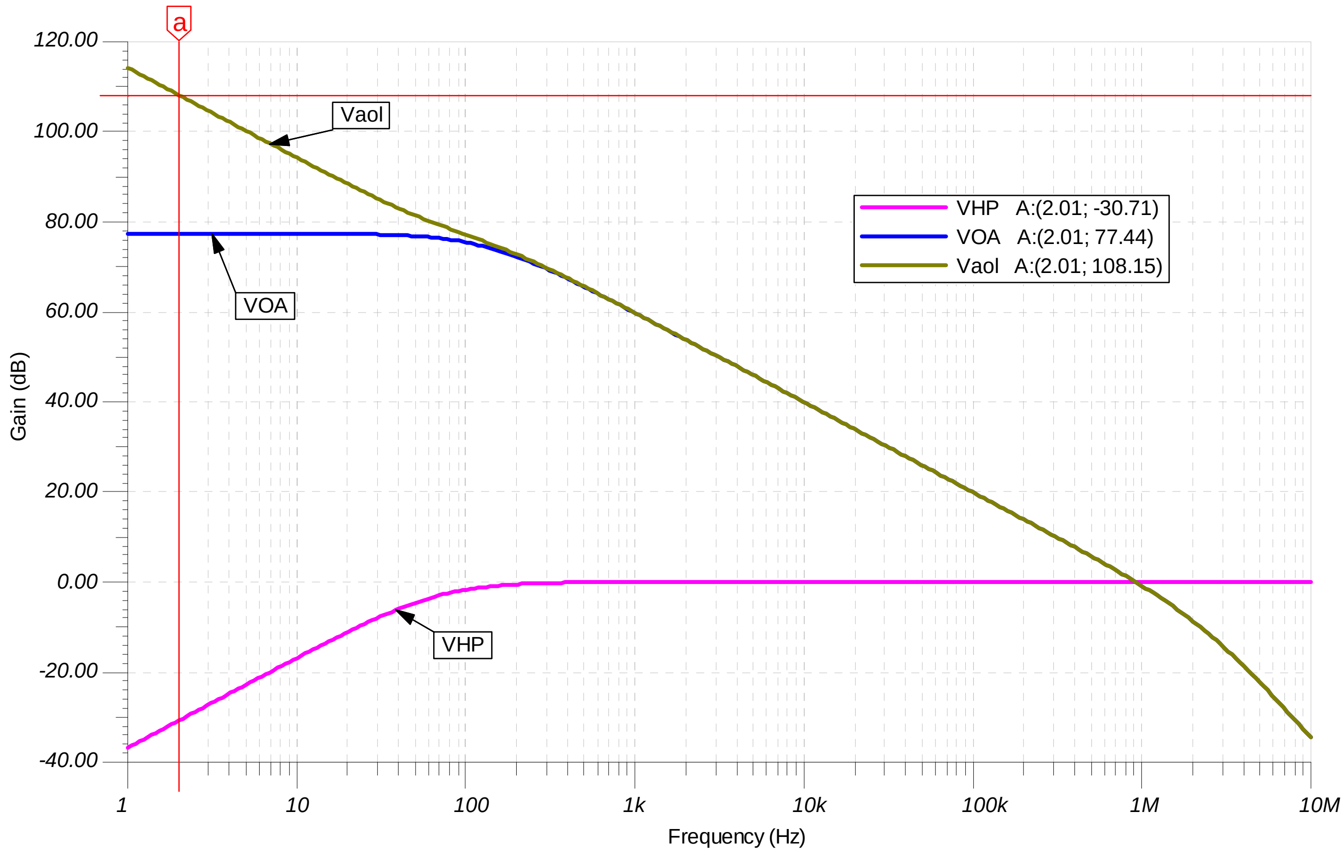



**Fig. 7.49: Equivalent Circuit Plots To Evaluate RL Effects On Aol**

## $Z_O$ Summary for CMOS RRO Op Amps

Fig. 7.50 summarizes the key characteristics of $Z_O$ for CMOS RRO op amps. At high frequencies $Z_O$ is dominated by $R_O$. For most loads, as dc output load current increases $R_O$ decreases making $R_O$ inversely proportional to $I_{OUT}$. However, for low values of $I_{OUT}$, $R_O$ is proportional to $I_{OUT}$. $Z_O$ is capacitive, CO, at mid to low frequencies. If capacitive loads, CL, are connected to a CMOS RRO output then $R_O$ and CO will interact with CL to create a modified Aol curve which contains an additional pole, fp2, from the original Aol curve. The low-frequency portion of the Aol curve is affected by resistive loads, RL, interacting with CO, forming a high-pass filter and flattening the Aol curve in the mid- to low-frequency region. $R_O$ does change with process and temperature and a good rule-of-thumb including these changes is 0. 5*$R_O$typ at -55°C to 2*$R_O$typ at 125°C, where $R_O$typ is at 25°C. There are always exceptions to the rules-of-thumb we have developed for open-loop output impedance of CMOS RRO op amps. The most complete and accurate data for $Z_O$ should be obtained from the op amp manufacturer, or measured.

- **$Z_O$ is Dominated by $R_O$ at High Frequencies**
- **$R_O$ is Inversely Proportional to $I_{OUT}$ for Most Values of $I_{OUT}$**
- **$R_O$ is Proportional to $I_{OUT}$ for Very Small Values of $I_{OUT}$**
- **$Z_O$ is Capacitive (CO) at Mid to Low Frequencies**
- **$R_O$, $C_O$, and CL form a Second Pole to create a Modified Aol**
- **RL and $C_O$ change the Low Frequency Portion of Aol**
- **$R_O$ Change with Process and Temperature:**
  - ✓ **$R_O$ @ -55C = 0.5 * $R_O$typ (i.e. 50 ohms)**
  - ✓ **$R_O$ @ 25C = $R_O$typ (i.e. 100 ohms)**
  - ✓ **$R_O$ @ +125C = 2 * $R_O$typ (i.e. 200 ohms)**
- **Use $R_O$typ for Stability Synthesis**
  - ✓ **Decade Rules-of-Thumb will provide Design Margin**

**Fig. 7.50: $Z_O$ Summary For CMOS RRO**


## Acknowledgements

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*Burr-Brown Products from Texas Instruments*
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Tony Larson, Senior Analog IC Design Engineer
Rod Burt, Senior Analog IC Design Manager

*Analog & RF Models*
Bill Sands, Consultant. http://www.home.earthlink.net/%7Ewksands/

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Holt, Charles A *Electronic Circuits.* John Wiley & Sons. New York. 1978


## About The Author


After earning a BSEE from the University of Arizona, Tim Green has worked as an analog and mixed-signal board/system level design engineer for over 23 years, including brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, and CCD cameras. Tim's recent experience includes analog & mixed-signal semiconductor strategic marketing. He is currently the Linear Applications Engineering Manager at Burr-Brown, a division of Texas Instruments, in Tucson, AZ and focuses on instrumentation amplifiers and digitally-programmable analog conditioning ICs. He can be contacted at green_tim@ti.com