SECTION 1

SINGLE-SUPPLY AMPLIFIERS

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SINGLE-SUPPLY AMPLIFIERS
Adolfo Garcia

Over the last several years, single-supply operation has become an increasingly important requirement as systems get smaller, cheaper, and more portable. Portable systems rely on batteries, and total circuit power consumption is an important and often dominant design issue, and in some instances, more important than cost. This makes low-voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of “doing more with less” in their amplifier designs.

SINGLE-SUPPLY AMPLIFIERS

- **Single Supply Offers:**
  - **Lower Power**
  - **Battery Operated Portable Equipment**
  - **Simplifies Power Supply Requirements**

- **But Watch Out for:**
  - **Signal-swings limited, therefore more sensitive to errors caused by offset voltage, bias current, finite open-loop gain, noise, etc.**
  - **More likely to have noisy power supply because of sharing with digital circuits**
  - **DC coupled, multi-stage single-supply circuits can get very tricky!**
  - **Rail-to-rail op amps needed to maximize signal swings**

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1mV are less than a 0.04 LSB error source in a 12-bit, 10V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1mV represents a 0.8LSB error in a 5V FS system, and 1.6LSB error in a 2.5V FS system.

Furthermore, amplifier bias currents, now flowing in larger source resistances to keep current drain from the battery low, can generate offset errors equal to or greater than the amplifier’s own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers having open-loop gains in the millions typically operate on dual supplies: for example, the OP07 family types. However, many single-supply/rail-to-rail amplifiers for precision applications

typically have open-loop gains between 25,000 and 30,000 under light loading (>10kohm). Selected devices, like the OPX13 family, do have high open-loop gains (i.e., >1V/µV).

Many trade-offs are possible in the design of a single-supply amplifier: speed versus power, noise versus power, precision versus speed and power, etc. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. System noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low-power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0V) is very convenient, as there is equal supply headroom in each direction, and 0V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0V input.

"RAIL-TO-RAIL" AMPLIFIERS

- **What exactly is “rail-to-rail”**
- **Does the input common mode range (for guaranteed CMMR) include: 0V, +Vs, both, or neither?**
- **Output Voltage Swing (how close to the rails can you get under load?)**
- **Where is “ground”?**
- **Complementary bipolar processes make rail-to-rail inputs and outputs feasible (within some fundamental physical limitations)**
- **Implications for precision single-supply instrumentation amps**

Early single-supply "zero-in, zero-out" amplifiers were designed on bipolar processes which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much poorer performance than the NPNs. Fully complementary processes are now required for the new-breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs do not use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose collector-emitter saturation voltage or drain-source channel on-resistance determine output signal swing with the load current.

The characteristics of a single-supply amplifier input stage (common-mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low-voltage applications. Rail-to-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or at the amplifier's positive supply. Amplifiers having a minimum of 60dB common-mode rejection over the entire input common-mode voltage range from 0V to the positive supply (V_{POS}) are good candidates. It is not necessary that amplifiers maintain common-mode rejection for signals beyond the supply voltages: what is required is that they do not self-destruct for momentary overvoltage conditions. Furthermore, amplifiers that have offset voltages less than 1mV and offset voltage drifts less than 2µV/°C are also very good candidates for precision applications. Since *input* signal dynamic range and SNR are equally if not more important than *output* dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5µVp-p in the 0.1Hz to 10Hz band.

Since the need for rail-to-rail amplifier output stages is driven by the need to maintain wide dynamic range in low-supply voltage applications, a single-supply/rail-to-rail amplifier should have output voltage swings which are within at least 100mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current, but the voltage swing of a good output stage should maintain its rated swing for loads down to 10kohm. The smaller the V_{OL} and the larger the V_{OH}, the better. System parameters, such as "zero-scale" or "full-scale" output voltage, should be determined by an amplifier's V_{OL} (for zero-scale) and V_{OH} (for full-scale).

Since the majority of single-supply data acquisition systems require at least 12- to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications.

SINGLE-SUPPLY/RAIL-TO-RAIL OP AMP INPUT STAGES

With the increasing emphasis on low-voltage, low-power, and single-supply operation, there is some demand for op amps whose input common-mode range includes *both* supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished

from the many applications where common-mode range *close* to the supplies or one that includes *one* of the supplies is necessary, but input rail-rail operation is not.

In many single-supply applications, it is required that the input go to only *one* of the supply rails (usually ground). Amplifiers which will handle zero-volt inputs are relatively easily designed using either PNP transistors (see OP90 and the OPX93 in Figure 1.3) or N-channel JFETs (see AD820 family in Figure 1.4). P-channel JFETs can be used where inputs must include the positive supply rail (but not the negative rail) as shown in Figure 1.4 for the OP282/OP482.

OP90 AND OPX93 INPUT STAGE ALLOWS INPUT TO GO TO THE NEGATIVE RAIL

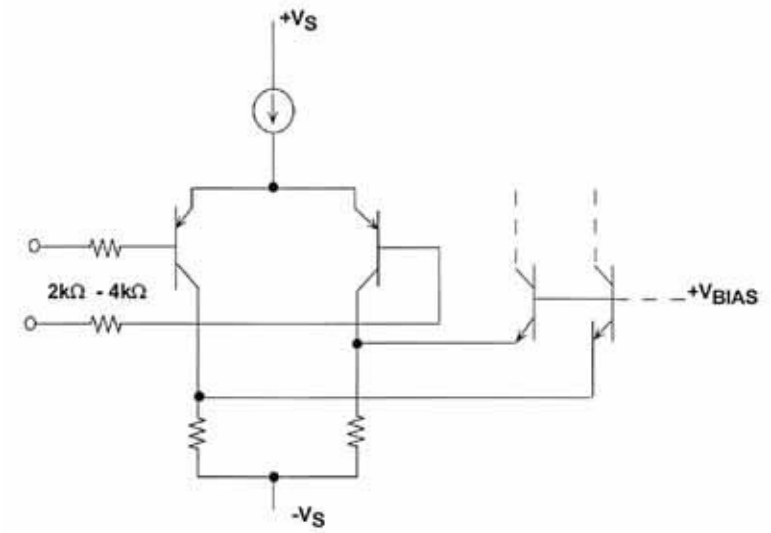


Figure 1.3

In the FET-input stages of Figure 1.4, the possibility exists for phase reversal as input signals approach and exceed the amplifier's linear input common-mode voltage ranges. As described in Section 7, internal amplifier stages saturate, forcing subsequent stages into cutoff. Depending on the structure of the input stage, phase reversal forces the output voltage to one of the supply rails. For n-channel JFET-input stages, the output voltage goes to the negative output rail during phase reversal. For p-channel JFET-input stages, the output is forced to the positive output rail. New FET-input amplifiers, like the AD820 family of amplifiers, incorporate design improvements that prevent output voltage phase reversal for signals within the rated supply voltage range. Their input stage and second gain stage even offer protection against output voltage phase reversal for input signals 200mV *more* positive than the positive supply voltage.

**AD820/AD822/AD824 INPUT INCLUDES NEGATIVE RAIL,
OP-282/OP-482 INCLUDES POSITIVE RAIL**

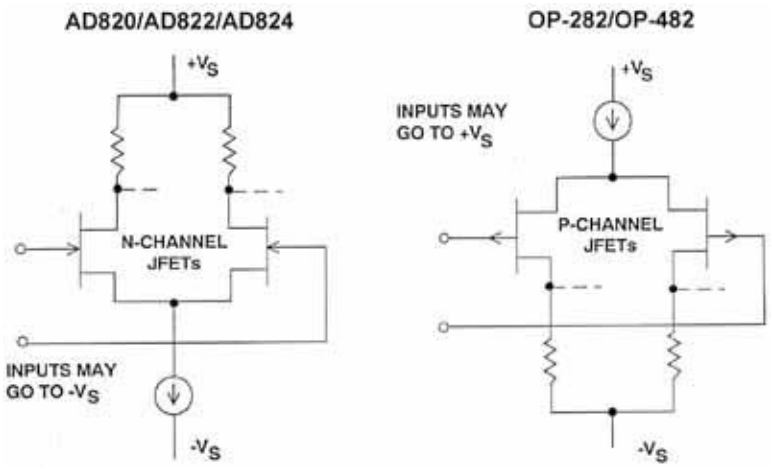


Figure 1.4

As shown in Figure 1.5, true rail-to-rail input stages require two long-tailed pairs, one of NPN bipolar transistors (or N-channel FETs), the other of PNP transistors (or p-channel FETs). These two pairs exhibit *different* offsets and bias currents, so when the applied input common-mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources (I1 and I2) remain active throughout the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the NPN pair and the PNP pair. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the common-mode input voltage range, compared to familiar dual supply precision devices like the OP07 or OP97. These specifications should be considered carefully when choosing a rail-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices.

RAIL-TO-RAIL INPUT STAGE TOPOLOGY

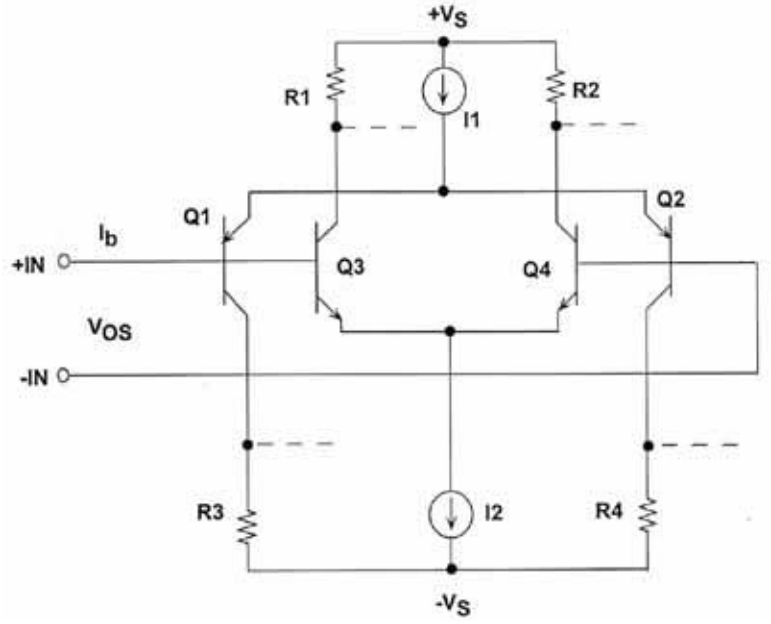


Figure 1.5

Many rail-to-rail amplifier input stage designs switch operation from one differential pair to the other differential pair somewhere along the input common-mode voltage range. Devices like the OPX91 family and the OP279 have a common-mode crossover threshold at approximately 1V below the positive supply. In these devices, the PNP differential input stage remains active; as a result, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are all determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly. Also, amplifier bias currents, dominated by the PNP differential pair over most of the input common-mode range, change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active. As a result, source impedance levels should be balanced when using such devices, as mentioned before, to minimize input bias current offsets and distortion.

An advantage to this type of rail-to-rail input stage design is that input stage transconductance can be made constant throughout the entire input common-mode voltage range, and the amplifier slews symmetrically for all applied signals.

Operational amplifiers, like the OP284/OP484, utilize a rail-to-rail input stage design where both PNP and NPN transistor pairs are active throughout the entire input common-mode voltage range, and there is no common-mode crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages. Amplifier input offset voltage exhibits a smooth transition throughout the entire input common-mode voltage range because of careful laser-trimming of resistors in the input stage. In the same manner, through careful input stage current balancing and input transistor design, amplifier input bias currents also exhibit a smooth transition throughout the entire common-mode input voltage range. The exception occurs at the extremes of the input common-mode range,

where amplifier offset voltages and bias currents increase sharply due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1V of either supply rail.

When *both* differential pairs are active throughout the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of the square root of 2 for FET input stages. Input stage transconductance determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching V_{POS}) or the NPN stage (signals approaching GND) are forced into cutoff. The thresholds at which the transconductance changes occur approximately within 1V of either supply rail, and the behavior is similar to that of the input bias currents.

Applications which initially appear to require true rail-rail inputs should be carefully evaluated, and the amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable. A true rail-to-rail input amplifier should not generally be used if an input range which includes only one rail is satisfactory.

SINGLE-SUPPLY/RAIL-TO-RAIL OP AMP OUTPUT STAGES

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 1.6. Naturally, the slew rates were greater for positive-going than for negative-going signals. While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. This asymmetry, which generally results from the use of IC processes with better NPN than PNP transistors, may also result in the ability of the output to approach one supply more closely than the other.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity.

OP AMP OUTPUT STAGES USING COMPLEMENTARY DEVICES ALLOW PUSH-PULL DRIVE

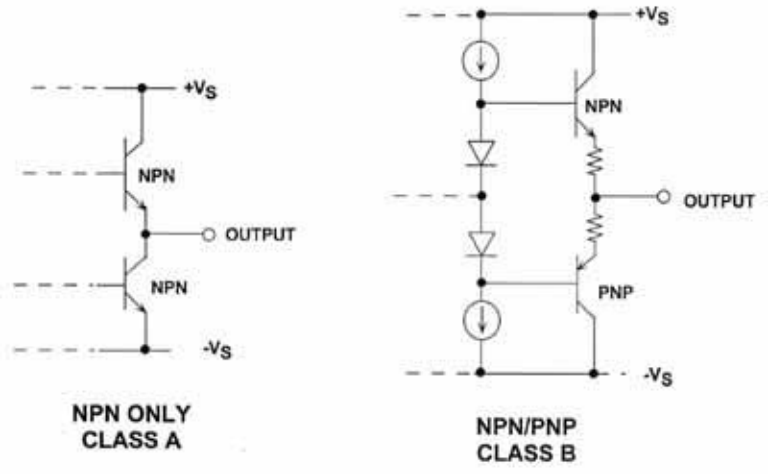


Figure 1.6

An IC process with relatively well-matched (AC and DC) PNP and NPN transistors allows both the output voltage swing and slew rate to be reasonably well matched. However, an output stage using BJTs cannot swing completely to the rails, but only to within the transistor saturation voltage (V_{CESAT}) of the rails (see Figure 1.7). For small amounts of load current (less than 100µA), the saturation voltage may be as low as 5 to 10mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500mV at 50mA).

On the other hand, an output stage constructed of CMOS FETs can provide true rail-to-rail performance, but only under no-load conditions. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs internal "on" resistance (typically, 100ohms).

RAIL-TO-RAIL OUTPUT STAGE SWING
IS LIMITED BY Vcesat, Ron, AND LOAD CURRENT

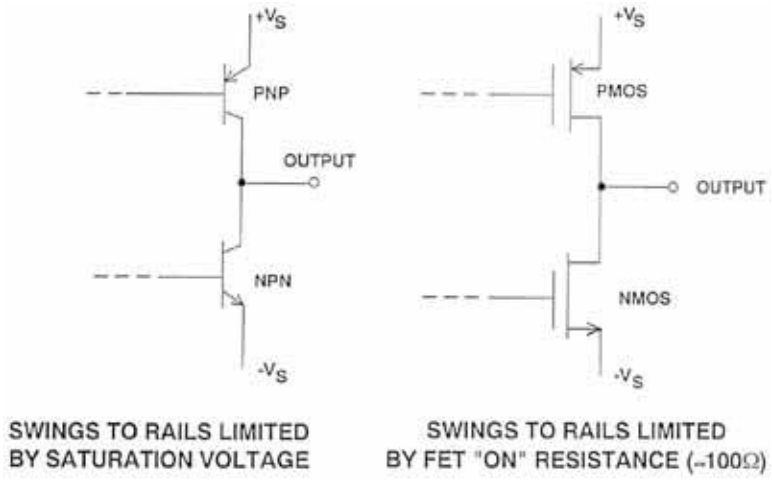


Figure 1.7

In summary, the following points should be considered when selecting amplifiers for single-supply/rail-to-rail applications:

First, input offset voltage and input bias currents can be a function of the applied input common-mode voltage (for true rail-to-rail input op amps). Circuits using this class of amplifiers should be designed to minimize resulting errors. An inverting amplifier configuration with a false ground reference at the non-inverting input prevents these errors by holding the input common-mode voltage constant. If the inverting amplifier configuration cannot be used, then amplifiers like the OP284/OP484 which do not exhibit any common-mode crossover thresholds should be used.

Second, since input bias currents are not always small and can exhibit different polarities, source impedance levels should be carefully matched to minimize additional input bias current-induced offset voltages and increased distortion. Again, consider using amplifiers that exhibit a smooth input bias current transition throughout the applied input common-mode voltage.

Third, rail-to-rail amplifier output stages exhibit load-dependent gain which affects amplifier open-loop gain, and hence closed-loop gain accuracy. Amplifiers with open-loop gains greater than 30,000 for resistive loads less than 10kohm are good choices in precision applications. For applications not requiring full rail-rail swings, device families like the OPX13 and OPX93 offer DC gains of 0.2V/µV or more.

Lastly, no matter what claims are made, rail-to-rail output voltage swings are functions of the amplifier's output stage devices and load current. The saturation voltage (V_{CESAT}), saturation resistance (R_{SAT}), and load current all affect the amplifier output voltage swing.

These considerations, as well as those regarding rail-to-rail precision, have implications in many circuits, namely instrumentation amplifiers, which will be covered in the next sections.

THE TWO OP AMP INSTRUMENTATION AMPLIFIER TOPOLOGY

There are several circuit topologies for instrumentation amplifier circuits suitable for single-supply applications. The *two op amp* configuration is often used in cost- and space-sensitive applications, where tight matching of input offset voltage, input bias currents, and open-loop gain is important. Also, when compared to other topologies, the two op amp instrumentation amplifier circuit offers the lowest power consumption and low total drift for moderate-gain (G=10) applications. Obviously, it also has the merit of using a single dual op amp IC.

Figure 1.8 shows the topology of a two op amp instrumentation circuit which uses a 5th gain-setting resistor, R_G. This additional gain-setting resistor is optional, and should be used in those applications where a fine gain trim is required. Its effect will be included in this analysis.

Circuit resistor values for this topology can be determined from Equations 1.1 through 1.3, where R1 = R4. To maintain low power consumption in single-supply applications, values for R should be no less than 10kohms:

$$R1 = R4 = R \qquad \text{Eq. 1.1}$$

$$R2 = R3 = \frac{R}{0.9G - 1} \qquad \text{Eq. 1.2}$$

$$R_G = \frac{2R}{0.06G} \qquad \text{Eq. 1.3}$$

where G equals the desired circuit gain. Note that in those applications where fine gain trimming is not required, Eq. 1.2 reduces to:

$$R2 = R3 = \frac{R}{G - 1} \qquad \text{Eq. 1.4}$$

A nodal analysis of the topology will illustrate the behavior of the circuit's nodal voltages and the amplifier output currents as functions of the applied common-mode input voltage (V_{CM}), the applied differential (signal) voltage (V_{IN}), and the output reference voltage (V_{REF}). These expressions are summarized in Equations 1.5 through 1.8, Eq. 1.12, and in Eq. 1.13 for positive, input differential voltages. Due to the structure of the topology, expressions for voltages and currents are similar in form and magnitude for negative, input differential voltages.

From the figure, expressions for the four nodal voltages A, B, C, and V_{OUT} as well as the output stage currents of A1 (I_{OA1}) and A2 (I_{OA2}) have been developed. Note that the direction of the amplifier output currents, I_{OA1} and I_{OA2}, is defined to be *into* the amplifier's output stage. For example, if the nodal analysis shows that I_{OA1} and I_{OA2} are positive entities, their direction is *into* the device; thus, their output stages are *sinking* current. If the analysis shows that they are negative quantities, their direction is opposite to that shown; therefore, their output stages are *sourcing* current.

Resistors R_{P1} and R_{P2} at the inputs to the circuit are optional input current limiting resistors used to protect the amplifier input stages against input overvoltage. Although any reasonable value can be used, these resistors should be less than 1kohm to prevent the unwanted effects of additional resistor noise and bias current-generated offset voltages. For protection against a specific level of overvoltage, the interested reader should consult the section on overvoltage effects on integrated circuits, found in Section 7 of this book.

THE TWO OP AMP INSTRUMENTATION AMPLIFIER TOPOLOGY IN SINGLE-SUPPLY APPLICATIONS

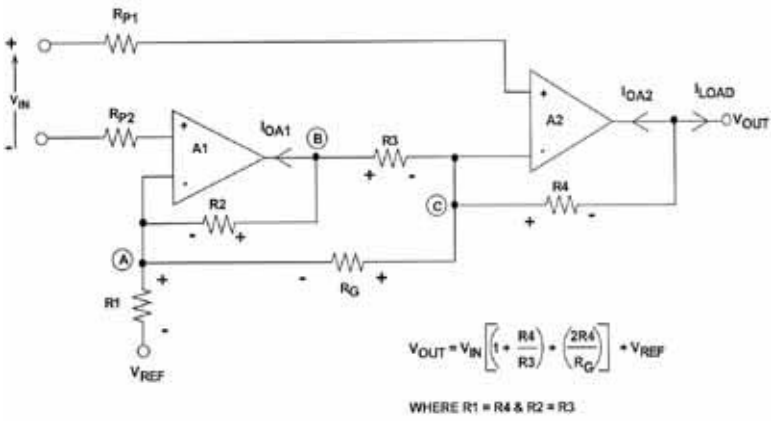


Figure 1.8

Using half-circuit concepts and the principle of superposition, the input signal voltage, V_{IN-} ,on the non-inverting input of A1 is set to zero. Since the input signal, V_{IN+} , is applied to the non-inverting terminal of A2, an expression for the nodal voltage at the inverting terminal of A1 is given by Eq. 1.5:

$$V_A = V_{CM} \qquad \text{Eq. 1.5}$$

An expression for the output voltage of A1 (node B) shows that it is dependent on all three externally applied voltages (V_{IN}, V_{CM}, and V_{REF}), and is illustrated in Eq. 1.6:

$$V_B = (-V_{IN+})\left(\frac{R2}{R_G}\right) + V_{CM}\left(1 + \frac{R2}{R1}\right) - V_{REF}\left(\frac{R2}{R1}\right) \qquad \text{Eq. 1.6}$$

Since the input signal, V_{IN+} ,as well as the applied input common-mode voltage, V_{CM}, is applied to the non-inverting terminal of A2, then the expression for the voltage at A2's inverting input (node C) is given by:

$$V_C = V_{CM} + V_{IN+} \qquad \text{Eq. 1.7}$$

For the case where R1 = R4 and R2 = R3, combining the results in Eq. 1.5, 1.6, and 1.7 yields the familiar expression for the circuit's output voltage:

$$V_{OUT} = (V_{IN+})\left(1 + \frac{R4}{R3} + \frac{2R4}{R_G}\right) + V_{REF} \qquad \text{Eq. 1.8}$$

At this point, it is worth noting the behavior of the circuit's nodal voltages based on the applied external voltages. From Eq. 1.5 and Eq. 1.7, the common-mode component of the current through R_G is equal to zero, whereas the full differential input voltage appears across it. Furthermore, Eq. 1.6 has shows that A1 *amplifies* the applied common-mode input voltage by a factor of (1 + R2/R1). In low-gain applications, the ratio of R2 to R_G can be as small as 1:1 (for circuit gains greater than or equal to 2). Therefore, Equation 1.6 sets the upper bound on the input common-mode voltage in low-gain applications. If the output of A1 is allowed to saturate at high input common-mode voltages, then it will not have enough "headroom" to amplify the input signal, as shown in Eq. 1.6. Therefore, in order for A1 to amplify accurately input signal voltages for any circuit gain > 1 (circuit gains equal to 1 are not permitted in this topology) requires that an upper bound on the total applied input voltage (common-mode plus differential-mode voltages) be determined to prevent amplifier output voltage saturation. This upper bound can be determined by the desired circuit gain, G, and the amplifier's minimum output high voltage:

$$V_{IN(TOTAL)} < V_{OH(MIN)}\left(\frac{0.9G - 1}{0.9G}\right) - V_{IN+} \qquad \text{Eq. 1.9}$$

In a similar fashion, a lower bound on the total applied input voltage is also determined by circuit gain and the amplifier's maximum output low voltage:

$$V_{IN(TOTAL)} > V_{OL(MAX)}\left(\frac{0.9G - 1}{0.9G}\right) + V_{IN+} \qquad \text{Eq. 1.10}$$

For example, if a rail-to-rail operational amplifier exhibited a $V_{OL(MAX)}$ equal to 10mV and a $V_{OH(MIN)}$ equal to 4.95V, and if the application required a circuit gain of 10 to produce a 1V full-scale output, then the total input voltage range would be bounded by:

$$0.109\ V < V_{IN(TOTAL)} < 4.3\ V$$

Therefore, the range over which the circuit will handle input voltages without amplifier output voltage saturation is given by:

$$V_{OL(MAX)}\left(\frac{0.9G-1}{0.9G}\right)+V_{IN+} < V_{IN(TOTAL)} < V_{OH(MIN)}\left(\frac{0.9G-1}{0.9G}\right)-V_{IN+} \qquad \text{Eq. 1.11}$$

In low-gain instrumentation circuits, the usable input voltage range is limited and asymmetric about the supply mid-point voltage. To complete the nodal analysis of the two op amp instrumentation circuit, expressions for operational amplifier output stage currents are shown in Equations 1.12 and 1.13:

$$I_{OA1} = (V_{IN+})\left(\frac{2}{R_G}+\frac{1}{R3}\right)+(V_{REF}-V_{CM})\left(\frac{2}{R1}\right) \qquad \text{Eq. 1.12}$$

$$I_{OA2} = (-V_{IN+})\left(\frac{2}{R_G}+\frac{1}{R3}\right)+(V_{CM}-V_{REF})\left(\frac{1}{R4}\right) \qquad \text{Eq. 1.13}$$

Equation 1.12 illustrates that A1's output stage must be able to sink current as a function of the applied differential input voltage and the output reference voltage. On the other hand, A1's output stage is required to source current over the entire input voltage range. *In the single-supply case where the circuit is required to sense small differential signals near ground, Eq. 1.6 and Eq. 1.12 both illustrate that A1's output stage is required to sink current while trying to maintain a more negative output voltage than its own negative supply. A1 is thus forced into saturation.*

As shown in Eq. 1.13, A2's output stage sources current for positive differential input voltages with no differential or common-mode voltage constraints placed upon its output by Eq. 1.8. *Note, however, that as a function of the applied common-mode voltage, A2 is required to sink current. Unfortunately, in the absence of an input signal, Eq. 1.13 shows that A2's output stage may be forced into saturation, trying to sink current while maintaining its output voltage at V_{OL}.*

To circumvent the circuit topological and amplifier output voltage limitations, a reference voltage should be used to bias the output of the circuit (A2's output) *in the middle of its output voltage swing*, and not at exactly one-half the supply voltage:

$$V_{REF} = \frac{V_{OH(MIN)} + V_{OL(MAX)}}{2} \qquad \text{Eq. 1.14}$$

The output reference voltage allows the output stages of A1 and A2 to sink or source current without any output voltage constraints. So long as Eq. 1.11 is used to define to total input voltage range, then amplifier behavior for differential- and common-mode operation is linear. To maximize output signal dynamic range and output SNR, the gain of the instrumentation amplifier circuit should be set according to Eq. 1.15:

$$\text{Circuit Gain} = \frac{V_{OH(MIN)} - V_{OL(MAX)}}{2\ V_{IN(MAX)}} \qquad \text{Eq. 1.15}$$

Under these operating conditions, the differential output voltage of the instrumentation amplifier circuit is now measured relative to V_{REF} and not to GND. Thus, negative full-scale input signals produce output voltages near A2's V_{OL}, and positive full-scale signals produce output voltages near A2's V_{OH}. Therefore, the circuit's input common-mode range and output dynamic range are optimized in terms of the desired circuit gain and amplifier output voltage characteristics.

For minimal impact of amplifier output load currents on V_{OH} and V_{OL}, circuit resistor values should be greater than 10kohm in most single-supply applications. Thus, Equations 1.11, 1.14, and 1.15 can all be used to design accurate and repeatable two op amp instrumentation amplifier circuits with single-supply/rail-to-rail operational amplifiers.

One fundamental limitation of the two operational amplifier instrumentation circuit is that since the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths), there will be generally poor AC common-mode rejection without the use of an AC CMR trim capacitor. For optimal AC CMR performance, a trimming capacitor should be connected between the inverting terminal of A1 to ground.

A TWO OP AMP, FET-INPUT INSTRUMENTATION AMPLIFIER

Figure 1.9 illustrates a two op amp instrumentation amplifier using the AD822, a dual JFET-input, rail-to-rail output operational amplifier. The output offset voltage is set by V_{REF}.

A SINGLE-SUPPLY, PROGRAMMABLE, FET-INPUT INSTRUMENTATION AMPLIFIER

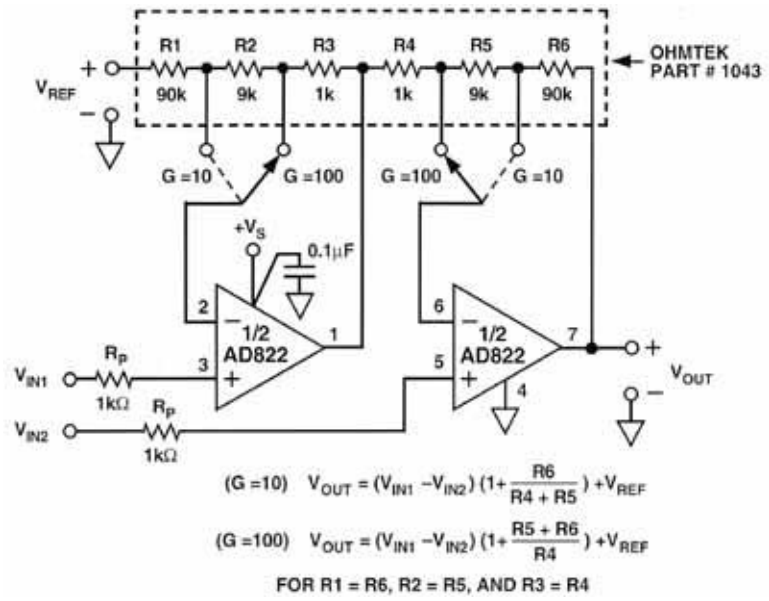


Figure 1.9

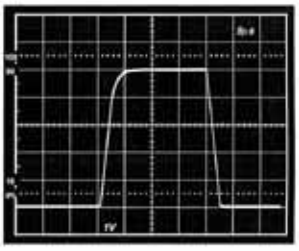
Dual operational amplifiers, like the AD822, make these types of instrumentation amplifiers both cost- and power-efficient. In fact, when operating on a single, +3 V supply, total circuit power consumption is less than 3.5mW. The AD822's 2pA bias currents minimize offset errors caused by unbalanced source impedances.

Circuit performance is enhanced dramatically by the use of a matched resistor network. A thin-film resistor array sets the circuit gain to either 10 or 100 through a DPDT (double-pole, double-throw) switch. The array's resistors are laser-trimmed for a ratio match of 0.01%, and exhibit a maximum differential temperature coefficient of 5ppm/°C. Note that in this application circuit, the fifth gain-setting resistor is not used. The use of this gain trim resistor would introduce serious gain and linearity errors due to the resistance of the double-pole, double-throw switches.

A performance summary and transient response of this instrumentation amplifier is shown in Figure 1.10. Note that the small-signal bandwidth of the circuit is independent of supply voltage, and that the rail-to-rail output pulse response is well-behaved. For greater bandwidth at the expense of higher supply current, the functionally similar AD823 can also be used.

PERFORMANCE SUMMARY OF AD822 IN-AMP

Parameters	V_S = 3V, 0V	V_S = ± 5V
CMRR	74dB	80dB
Common-Mode Voltage Range, G = 10	+0.51 to +1.75V	-4.49 to +3.75V
G = 100	+0.06 to +1.98V	-4.90 to +3.98V
3dB BW, G=10	180kHz	180kHz
3dB BW, G=100	18kHz	18kHz
$t_{settling}$ 2V Step (V_S = 0V, 3V)	2 µs	
5V Step (V_S = ±5V)		5 µs
Noise @ 1kHz, G=10	270 nV/√Hz	270 nV/√Hz
(RTO) G=100	2.2 µV/√Hz	2.2 µV/√Hz
Supply Current	1.10mA	1.15mA



Input = 500mV, G=10, Vs = +5V, 0V
Vertical Scale: 1V/div
Horizontal Scale: 5 µs/div

Figure 1.10

THE THREE OP AMP INSTRUMENTATION AMPLIFIER TOPOLOGY

For the highest precision and performance, the *three op amp* instrumentation amplifier topology is optimum for bridge and other offset transducer applications where high accuracy and low nonlinearity are required. This is at the expense of additional power consumption over the two op amp instrumentation circuit (3 amplifiers versus 2 amplifiers). Furthermore, like the two op amp configuration, the input amplifiers can use one dual op amp for tight matching of input offset voltage matching, input bias current, and open-loop gain. Or, a single quad operational amplifier can be used for the whole circuit, including a reference voltage buffer, if required.

Single-supply/rail-to-rail amplifiers can be used in this topology, like that shown for two op amp designs, if the output characteristics of the single-supply/rail-to-rail amplifiers are understood. As shown in Figure 1.11, a generalized, comprehensive analysis of the structure will illustrate the behavior of the nodal voltages and amplifier output currents as functions of the applied common-mode input voltage (V_{CM}), the applied differential (signal) voltage (V_{IN}), and the output reference voltage (V_{REF}). As shown in Eq. 1.16 through 1.27, the nodal analysis was carried out for positive-input differential voltages; because of the symmetry in the circuit, the expressions for the nodal voltages and amplifier output currents carried out for negative-input differential voltages are identical.

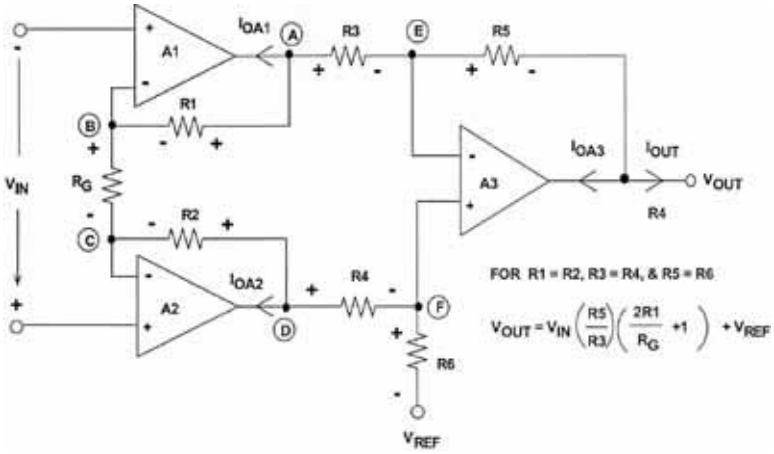


Figure 1.11

Using half-circuit concepts and the principle of superposition, the signal voltage applied to the non-inverting terminal of A1 is set to zero. Since the input signal is applied to the non-inverting terminal of A2, then an expression for the output voltage of amplifier A1 (node A) for positive, differential input signals is given by Eq. 1.16:

$$V_A = (-V_{IN+})\left(\frac{R1}{RG}\right) + V_{CM} \qquad \text{Eq. 1.16}$$

Since the voltage at the inverting input of A1 must equal the voltage at its non-inverting terminal, then an expression for the voltage at amplifier A1's inverting terminal (node B) is given by Eq. 1.17:

$$V_B = V_{CM} \qquad \text{Eq. 1.17}$$

In a similar manner, the voltage at A2's inverting terminal must equal the voltage on A2's non-inverting terminal:

$$V_C = V_{IN+} + V_{CM} \qquad \text{Eq. 1.18}$$

The expression for the output voltage of A2 (node D) shows that it is dependent upon both the input signal and the applied input common-mode voltage:

$$V_D = (V_{IN+})\left(1 + \frac{R2}{RG}\right) + V_{CM} \qquad \text{Eq. 1.19}$$

At this point, it is worth noting the behavior of the nodal voltages of the input amplifiers as functions of the applied differential input voltage and the input common-mode voltage. From Eqs. 1.17 and 1.18, the common-mode component of

the current through the gain setting resistor, R_G,is zero – the input stages simply buffer the applied input common-mode voltage. In other words, *the input stage common-mode gain is unity*.

On the other hand, the full differential input voltage appears across R_G. In fact, Eq. 1.16 shows that A1 multiplies and inverts the input differential voltage by a factor of (– R1/R_G), while Eq. 1.19 shows that A2 multiplies the input voltage by a factor of (1+ R1/R_G). For the case where the output subtractor stage is configured for a gain of 1, all the differential gain is set in the input stage. Therefore, the ratio of R1 to R_G (or R2 to R_G) could be as small as 1:1 or as large as 5000:1. Therefore, to avoid input amplifier output voltage saturation requires an upper and a lower bound be placed on the total input voltage (defined to be common-mode plus differential-mode voltages). These bounds are set by the gain of the instrumentation amplifier and the output high and low voltage limits of the amplifier. The lower bound on the total applied input voltage is given by Eq. 1.20:

$$V_{IN(TOTAL)} > V_{OL(MAX)} + \left(\frac{G-1}{2}\right)(V_{IN+}) \qquad \text{Eq. 1.20}$$

An upper bound on the total input voltage can be determined in a similar fashion and is also dependent on the circuit gain and the amplifier's minimum output high voltage:

$$V_{IN(TOTAL)} < V_{OH(MIN)} - \left(\frac{G+1}{2}\right)(V_{IN+}) \qquad \text{Eq. 1.21}$$

For example, if a rail-to-rail operational amplifier exhibited a $V_{OL(MAX)}$ equal to 10mV and a $V_{OH(MIN)}$ equal to 4.95V, and if the application required a circuit gain of 10 for a 1V full-scale output, then the total input voltage range would be bounded by:

$$0.46\ V < V_{IN(TOTAL)} < 4.4\ V$$

Therefore, for the three op amp instrumentation circuit, the total applied input voltage range expressed in terms of circuit gain and amplifier output voltage limits is given by:

$$V_{OL(MAX)} + \left(\frac{G-1}{2}\right)(V_{IN+}) < V_{IN(TOTAL)} < V_{OH(MIN)} - \left(\frac{G+1}{2}\right)(V_{IN+}) \qquad \text{Eq. 1.22}$$

Since the non-inverting input of the subtractor amplifier A3 determines the voltage on its inverting terminal, an expression for the voltages at Nodes E and F is given by Eq. 1.23:

$$V_E = V_F = (V_{IN+}) \left(\frac{R6}{R4 + R6}\right)\left(1 + \frac{R2}{R_G}\right) + V_{CM}\left(\frac{R6}{R4 + R6}\right) + V_{REF}\left(\frac{R4}{R4 + R6}\right)$$

Eq. 1.23

For the case where R3, R4, R5, and R6 are all equal to R (typically the case for instrumentation amplifier gains greater than or equal to 1), then these nodal voltages will set up at one-half the applied output voltage reference (V_{REF}) and at one-half the applied input common-mode voltage (V_{CM}). Furthermore, the component due to the amplified differential input signal is also attenuated by a factor of two. Finally, Eq. 1.24 shows an expression for the circuit's output voltage in its familiar form for R4 = R3 and R6 = R5:

$$V_{OUT} = (V_{IN+})\left(\frac{R5}{R3}\right)\left(1 + \frac{2R1}{R_G}\right) + V_{REF} \qquad \text{Eq. 1.24}$$

From Eq. 1.24, the circuit output voltage is only a function of the amplified input differential voltage and the output reference voltage. Provided that R4 = R3 and R6 = R5, the component of the output voltage due to the applied input common-mode voltage is completely suppressed. The only remaining error voltage is that due to the finite CMR of A3 and the ratio match of R3 to R5 and R4 to R6. Also, in the absence of either an input signal or an output reference voltage, A3's output voltage is equal to zero; in a single-supply application where rail-to-rail output amplifiers are used, it is equal to V_{OL}.

To complete the analysis of this instrumentation circuit, expressions for operational amplifier output stage currents have been developed and are shown in Eqs. 1.25 through 1.27:

$$I_{OA1} = \frac{V_{IN+}}{R3}\left[\left(\frac{R1}{R_G}\right)\left(1 + \frac{R3}{R1}\right) + 1 + \frac{R2}{R_G}\left(\frac{R4}{R4 + R6}\right)\right] + \frac{V_{REF} - V_{CM}}{R3}\left(\frac{R4}{R4 + R6}\right)$$

Eq. 1.25

$$I_{OA2} = (-V_{IN+})\left[\left(1 + \frac{R2}{R_G}\right)\left(\frac{1}{R2}\right) + \frac{1}{R4} - \frac{1}{R4}\left(\frac{R6}{R4 + R6}\right)\right] - \left(\frac{1}{R2}\right) + \frac{V_{REF} - V_{CM}}{R4 + R6}$$

Eq. 1.26

$$I_{OA3} = \frac{-(V_{IN+})}{R3 + R5}\left(\frac{R1}{R_G}\right) + \frac{R5}{R3} + \frac{2\ R1\ R5}{R3\ R_G} + \frac{V_{CM} - V_{REF}}{R3 + R5} \qquad \text{Eq. 1.27}$$

Recall in the analysis of the two-amplifier instrumentation circuit that amplifier output stage currents were defined to be positive, if current flow is *into* the device, the amplifier is *sinking* current. Conversely, if the nodal analysis shows that output currents are negative quantities, then current flow is *out of* the amplifier, and the amplifier is *sourcing* current.

Equation 1.25 illustrates that A1's output stage must be able to sink current as a function of the applied differential input voltage and the output reference voltage. On the other hand, A1's output stage is required to source current throughout the applied common-mode voltage. In the single-supply case where the circuit is required to sense small differential signals near ground, Eq. 1.16 and Eq. 1.25 both illustrate that A1's output stage is required to sink current while trying to maintain a more negative output voltage than its own negative supply. A1 cannot sustain this operating point, and thus is forced into output saturation.

As shown in Eq. 1.26, A2's output stage sources current for positive input signal voltages with no differential nor common-mode voltage constraints placed upon its output by Eq. 1.19. A3's output stage is also required to source current around its feedback resistor as a function of the positive input differential voltage. Note, however, that as a function of the applied common-mode voltage, it is required to sink current. *Unfortunately Eq. 1.24 showed that in the absence of an input signal, A3's output stage can be forced into saturation, trying to sink current while maintaining its output voltage at A3's* V_{OL}.

To circumvent circuit topological and amplifier output voltage limitations, the results shown in Eq. 1.14 and Eq. 1.15 for the two op amp instrumentation circuit apply equally well here. The output reference voltage is chosen in the middle of A1 and A2's output voltage swing:

$$V_{REF} = \frac{V_{OH(MIN)} + V_{OL(MAX)}}{2} \qquad \text{Eq. 1.14}$$

Similarly, output signal dynamic range and output SNR are maximized if the gain of the instrumentation circuit is set according to Eq. 1.15:

$$\text{Circuit Gain} = \frac{V_{OH(MIN)} - V_{OL(MAX)}}{2\ V_{IN(MAX)}} \qquad \text{Eq. 1.15}$$

Under these operating conditions, the differential output voltage of the instrumentation amplifier circuit is now measured relative to V_{REF} and not to GND. Thus, negative full-scale input signals yield output voltages near A3's V_{OL}, and positive full-scale signals produce output voltages near A3's V_{OH}. Thus, circuit input common-mode range and output dynamic range are optimized in terms of the desired circuit gain and amplifier output voltage characteristics.

For minimal impact on V_{OH} and V_{OL} due to amplifier output load currents, circuit resistor values should be greater than 10kohm in single-supply applications. Thus, Equations 1.22, 1.14, and 1.15 can all be used to design accurate and repeatable three op amp instrumentation amplifier circuits with single-supply/rail-to-rail operational amplifiers.

A COMPOSITE, SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER [3]

As it has been shown throughout this chapter, operation of high performance linear circuits from a single, low-voltage supply (5V or less) is a common requirement. While there are many precision single supply operational amplifiers (some rail-rail), such as the OP213, the OP291, and the OP284, and some good single-supply instrumentation amplifiers, such as the AMP04 and the AD626 (both covered later), the highest performance instrumentation amplifiers are still specified for dual-supply operation.

One way to achieve both high precision and single-supply operation takes advantage of the fact that several popular transducers (e.g. strain gauges) provide an output signal centered around the (approximate) mid-point of the supply voltage (or the reference voltage), where the inputs of the signal conditioning amplifier need not operate near "ground" or the positive supply voltage.

Under these conditions, a dual-supply instrumentation amplifier referenced to the supply mid-point followed by a "rail-to-rail" operational amplifier gain stage provides very high DC precision. Figure 1.12 illustrates one such high-performance instrumentation amplifier operating on a single, +5V supply. This circuit uses an AD620 low-cost precision instrumentation amplifier for the input stage, and an AD822 JFET-input dual rail-to-rail output operational amplifier for the output stage.

A PRECISION SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL OUTPUT

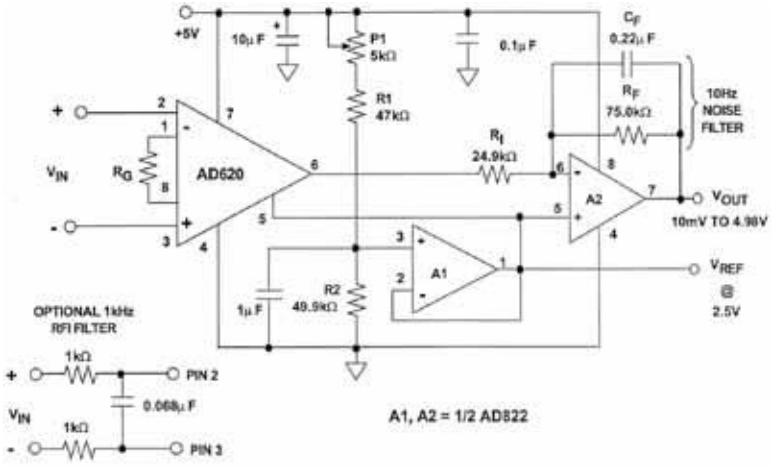


Figure 1.12

In this circuit, R1 and R2 form a voltage divider which splits the supply voltage in half to +2.5V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of an AD822 which buffers it and provides a low-impedance source needed to drive the AD620's output reference port. The AD620's REFERENCE input has a 10kohm input resistance and an input signal current of up to 200µA. The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output ±2.5V, "rail-to-rail," with only ±0.83V required of the AD620. This output voltage level of the AD620 is well within the AD620's capability, thus ensuring high linearity for the "dual-supply" front end. *Note that the final output voltage must be measured with respect to the +2.5V reference, and not to GND.*

The general gain expression for this composite instrumentation amplifier is the product of the AD620 and the inverting amplifier gains:

$$GAIN = \left(\frac{49.4k\Omega}{R_G} + 1\right)\left(\frac{R_F}{R_I}\right) \quad \text{Eq. 1.28}$$

For this example, an overall gain of 10 is realized with R_G = 21.5kohm (closest standard value). The table (Figure 1.13) summarizes various R_G/gain values.

In this application, the total input voltage applied to the inputs of the AD620 can be up to +3.5V with no loss in precision. For example, at an overall circuit gain of 10, the common-mode input voltage range spans 2.25V to 3.25V, allowing room for the ±0.25V full-scale differential input voltage required to drive the output ±2.5V about V_{REF}.

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the buffer's feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100kHz for gain configurations up to 300. Figure 1.13 summarizes the performance of this composite instrumentation amplifier. To reduce the effects of unwanted noise pickup, a capacitor is recommended across A2's feedback resistance to limit the circuit bandwidth to the frequencies of interest. Also, to prevent the effects of input-stage rectification, an optional 1kHz filter is recommended at the inputs of the AD620.

PERFORMANCE SUMMARY OF THE +5V SINGLE-SUPPLY AD620/AD822 COMPOSITE INSTRUMENTATION AMP WITH RAIL-TO-RAIL OUTPUTS

CIRCUIT GAIN	R_G (Ω)	Vos, RTI (μV)	TCVos, RTI (μV/°C)	Nonlinearity*	Bandwidth** (kHz)
10	21.5k	1000	4.5	<0.005%	600
30	5.49k	430	1.5	<0.005%	600
100	1.53k	215	1.4	<0.005%	300
300	499	150	1.1	<0.005%	120
1000	149	150	1.0	<0.005%	30

*Nonlinearity measured over the output voltage range: 0.1V < V_{OUT} < 4.90V
**Bandwidth measured with no input filter and no 10Hz noise filter

- Input bias current (2nA, max) must have DC return path to power supply
- Total V_{IN} (CM + DM) = $V_{IN,CM} \pm \frac{V_{IN,DM}}{2}$

Figure 1.13

LOW-SIDE AND HIGH-SIDE SIGNAL CONDITIONING

As previous discussions have shown, single-supply and rail-to-rail operational amplifiers in two and three op amp instrumentation amplifier circuits impose certain limits on the usable input common-mode and output voltage ranges of the circuit. There are, however, many single-supply applications where low- and high-side signal conditioning is required. For these applications, novel circuit design techniques allow sensing of very small differential signals at GND or at V_{POS}. Two such devices, the AMP04 and AD626, have been designed specifically for these applications.

As illustrated in Figure 1.14, the AMP04, a single-supply instrumentation amplifier, uses a inverting-mode output gain architecture, where an external resistor, R_G (connected between the AMP04's Pins 1 and 8), is used as the input resistor to A4, and an internal 100kohm thin-film resistor, R1, serves as the output amplifier's feedback resistance. Unity-gain input buffers A1 and A2 both serve two functions: they present a high impedance to the source, and provide a DC level shift to the applied common-mode input voltage of one V_{BE} for amplifiers A3 and A4. As a result, their output stages can operate very close the negative supply without saturating.

The input buffers are designed with PNP transistors that allow the applied common-mode voltage range to extend to 0V. In fact, the usable input common-mode voltage range of the AMP04 actually extends 0.25V *below* the negative supply (although not guaranteed, applied input voltages to any integrated circuit should always remain within its total supply voltage range). On the other hand, since the input buffers are PNP stages, the input common-mode voltage range does not include the AMP04's positive supply voltage. When the inputs are driven within 1V of the positive rail,

the PNP input transistors are forced into cutoff; and, as a result, input offset voltages and bias currents increase, and CMR degrades.

SINGLE SUPPLY INSTRUMENTATION AMP HANDLES ZERO-VOLTS INPUT AND ZERO-VOLTS OUTPUT (AMP04)

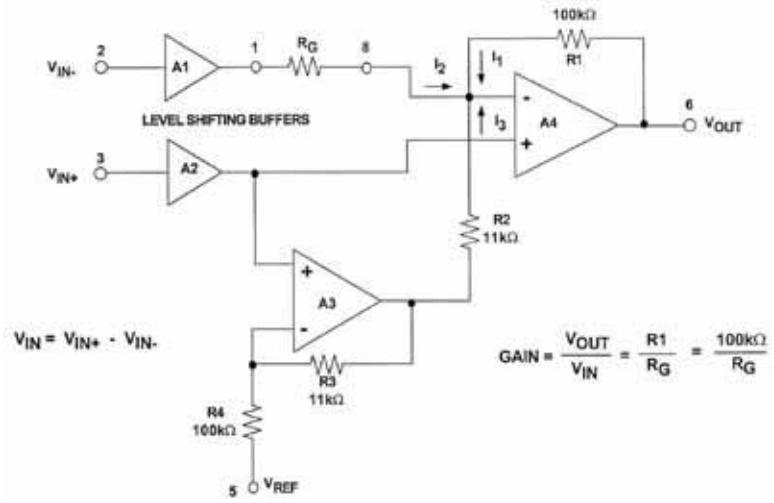


Figure 1.14

A pulsed-bridge transducer-driver/amplifier illustrates the utility of this low-power, single-supply instrumentation amplifier circuit as shown in Figure 1.15. Commonly available 350ohm strain-gauge bridges are difficult to apply in low-voltage, low-power systems for a number of reasons, including the requirements for high bridge drive currents and high sensitivity. For low-speed measurements, power limitations can be overcome by operating the bridge in a pulsed-power mode, reading the amplified output on a low-speed, low-duty-cycle basis.

A LOW POWER, PULSED LOAD CELL BRIDGE AMPLIFIER

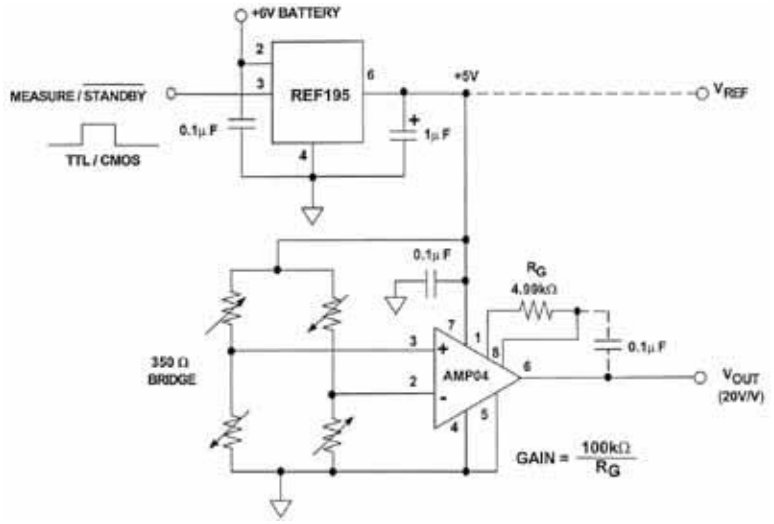


Figure 1.15

In this circuit, an externally generated 800µs TTL/CMOS pulse is applied to the SHUTDOWN input to the REF195, a +5V precision voltage reference. The REF195's shutdown feature is used to switch between a normal +5V DC output if left open (or at logic HIGH), and a low-power-down standby state (5µA maximum current drain) with the shutdown pin held low. The switched 5V output from the REF195 drives the bridge and supplies power to the AMP04. The AMP04 is programmed for a gain of 20 by the 4.99kohm resistor, which should be a stable film type (TCR = 50ppm/°C or better) in close physical proximity to the amplifier. Dynamic performance of the circuit is excellent, because the AMP04's output settles to within 0.5mV of its final value in about 230µs (not shown).

This approach allows fast measurement speed with a minimum standby power. Generally speaking, with all active circuitry essentially being switched by the measurement pulse, the average current drain of this circuit is determined by its duty cycle. On-state current drain is about 15mA from the 6V battery during the measurement interval (90mW peak power). Therefore, an 800µs measurement strobe once per second will dissipate an average of 72µW, to which is added the 30µW standby power of the REF195. In any event, overall operation is enhanced by the REF195's low-dropout regulation characteristics. The REF195 can operate with supply voltages as low as +5.4 V and still maintain +5V output operation.

If low-frequency filtering is desired, an optional capacitor can be connected between pins 6 and 8 of the AMP04. However, a much longer strobe pulse must be used so that the filter can settle to the circuit's required accuracy. For example, if a 0.1µF capacitor is used for noise filtering, then the R-C time constant formed with the AMP04's internal 100kohm resistor is 10ms. Therefore, for a 10-bit settling criterion, 6.9 time constants, or 70ms, should be allowed. Obviously, this will place greater demands upon system power, so trade-offs may be necessary in the amount of filtering used.

Of course, the amplified bridge output appears only during the measurement interval, and is valid after 220µs unless filtering is used. During this time, a sampled-input ADC (analog-to-digital converter) reads V_{OUT}, eliminating the need for a dedicated sample-and-hold circuit to retain the output voltage. If 10-bit measurements are sufficient, the 5V bridge drive can also be assumed to be constant (for 10-bit accuracy), because the REF195 exhibits a ±1mV (±0.02 %) output voltage tolerance. For more accurate measurements, a ratiometric reading of the bridge status can be obtained by reading the bridge drive (V_{REF}) as well as V_{OUT}.

On the other hand, single-supply instrumentation amplifiers, like the AD626, shown in Figure 1.16, exhibit an input stage architecture that allows the sensing of small differential input signals, not only at its positive supply, but beyond it as well. The AD626 is a differential amplifier consisting of a precision balanced attenuator, a very low-drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages, without the use of any other external active or passive components.

AD626 SCHEMATIC ILLUSTRATES INPUT PROTECTION AND SCALING RESISTORS AND ALLOWS INPUT COMMON MODE VOLTAGE UP TO 6 x (Vs - 1V)

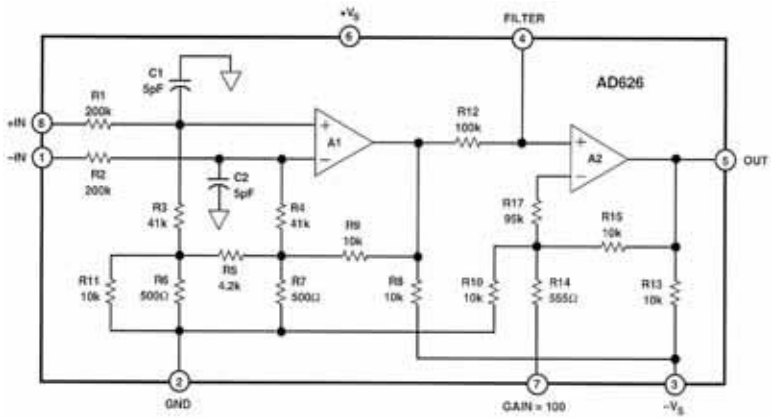


Figure 1.16

The simplified equivalent circuit in Figure 1.16 illustrates the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to the dual resistive attenuators R1 through R4, whose purpose is to reduce the peak common-mode voltage at the inputs of A1. This allows the applied differential voltage to be accurately amplified in the presence of large common-mode voltages six times greater than that which can be tolerated by the actual input to A1. As a result, input common-mode rejection extends to $6\times(V_S - 1V)$. The overall common-mode error is minimized by precise laser trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio (CMRR) of at least 10,000:1 (80dB).

To minimize the effect of spurious RF signals at the inputs due to rectification at the inputs to A1, small filter capacitors C1 and C2, internal to the AD626, limit the input bandwidth to 1MHz.

The output of A1 is connected to the input of A2 via a 100kohm resistor (R12) to allow the low-pass filtering to the signals of interest. To use this feature, a capacitor is connected between Pin 4 and the circuit's common. Equation 1.29 can be used to determine the value of the capacitor, based on the corner frequency of this low-pass filter:

$$C_{LP} = \frac{1}{2\pi\ (100\ k\Omega)\ f_{LP}} \quad \text{Eq. 1.29}$$

where f_{LP} = the desired corner frequency of the low-pass filter, in Hz.

The 200kohm input impedance of the AD626 requires that the source resistance driving this amplifier should be less than 1kohm to minimize gain error. Also, any mismatch between the total source resistance of either input will affect gain accuracy and common-mode rejection. For example, when operating at a gain of 10, an 80ohm mismatch in the source resistance between the inputs will degrade circuit CMR to 68dB.

Output amplifier, A2, operates at a gain of 2 or 20, thus setting the overall, precalibrated gain of the AD626 (with no external components) at 10 or 100. The gain is set by the feedback network around amplifier A2.

The output of A2 uses an internal 10kohm resistor to $-V_S$ to "pull down" its output. In single-supply applications where $-V_S$ equals GND, A2's output can drive a 10kohm ground-referenced load to at least +4.7V. The minimum nominal "zero" output voltage of the AD626 is 30mV.

If pin 7 is left unconnected, the gain of the AD626 is 10. By connecting pin 7 to GND, the AD626's gain can be set to 100. To adjust the gain of the AD626 for gains between 10 and 100, a variable resistance network can be used between pin 7 and GND. This variable resistance network includes a fixed resistor with a rheostat-connected potentiometer in series. The interested reader should consult the AD626 data sheet for complete details for adjusting the gain of the AD626. For these applications, a ±20% adjustment range in the gain is required. This is due to the on-chip resistors absolute tolerance of 20% (these resistors, however, are ratio-matched to within 0.1%).

An example of the AD626 high-side sensing capabilities, Figure 1.17 illustrates a typical current sensor interface amplifier. The signal current is sensed across the current shunt, R_S. For reasons mentioned earlier, the value of the current shunt should be less than 1ohm and should be selected so that the average differential voltage across this resistor is typically 100mV. To generate a full-scale output voltage of +4V, the AD626 is configured in a gain of 40. To accommodate the tolerance in the current shunt, the variable gain-setting resistor network shown in

the circuit has an adjustment range of ±20%. Note that sufficient headroom exists in the gain trim to allow at least a 10% overrange (+4.4V).

AD626 HIGH-SIDE CURRENT MONITOR INTERFACE

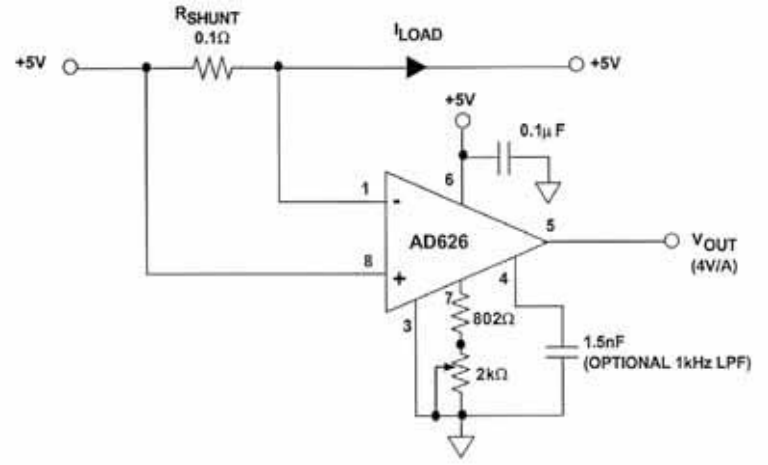


Figure 1.17

INSTRUMENTATION AMPLIFIER INPUT-STAGE RECTIFICATION

A well-known phenomenon in analog integrated circuits is RF rectification, particularly in instrumentation amplifiers and operational amplifiers. While amplifying very small signals, these devices can rectify unwanted high-frequency, out-of-band signals. The results are DC errors at the output in addition to the wanted sensor signal. Unwanted out-of-band signals enter sensitive circuits through the circuit's conductors which provide a direct path for interference to couple into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling. Regardless of the type of interference, the unwanted signal is a voltage which appears in series with the inputs.

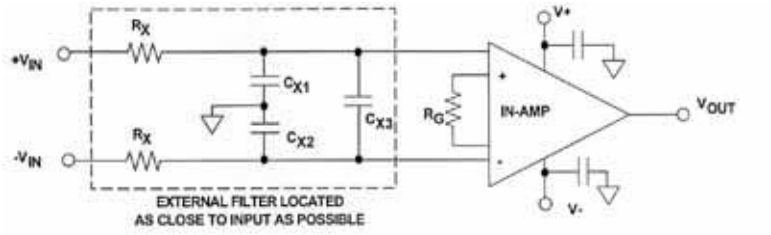
All instrumentation and operational amplifier input stages are either emitter-coupled (BJT) or source-coupled (FET) differential pairs with resistive or current-source loading. Depending on the quiescent current level in the devices and the frequency of the interference, these differential pairs can behave as high-frequency detectors. As it has been shown in [1], this detection process produces spectral components at the harmonics of the interference as well at DC. It is the DC component that shifts internal bias levels of the input stages causing errors, which can lead to system inaccuracies. For a complete treatment of this issue, including analytical and empirical results, the interested reader should consult Reference [1].

Since it is required to prevent unwanted signals and noise from entering the input stages, input filtering techniques are used for these types of devices. As illustrated in Reference [1], this technique uses an equivalent approach suggested for operational amplifiers. As shown in Figure 1.18, low-pass filters are used in series

with the differential inputs to prevent unwanted noise from reaching the inputs. Here, capacitors, C_{X1}, C_{X2}, and C_{X3}, connected across the inputs of the instrumentation amplifier, form common-mode (C_{X1} and C_{X2}) and differential-mode (C_{X3}) low-pass filters with the two resistors, R_X. Time constants R_X-C_{X1} and R_X-C_{X2} should be well-matched (1% or better), because imbalances in these impedances can generate a differential error voltage which will be amplified.

On the other hand, an additional benefit of using a differentially-connected capacitor is that it can reduce common-mode capacitive imbalance. This differential connection helps to preserve high-frequency AC common-mode rejection. Since series resistors are required to form the low-pass filter, errors due to poor layout (CMR imbalance), component tolerance of R_X (input bias current-induced offset voltage) and resistor thermal noise must be considered in the design process. In applications where the sensor is an RTD or a resistive strain gauge, R_X can be omitted, provided the sensor is close to the amplifier.

EXTERNAL COMMON-MODE AND DIFFERENTIAL-MODE INPUT FILTERS PREVENT RFI RECTIFICATION IN INSTRUMENTATION AMPLIFIER CIRCUITS



- C_{X1}, C_{X2} forms common-mode RC filter with R_X; $\tau_{CM}(LPF) = R_X C_{X1}$
- C_{X3} forms differential RC with R_X; $\tau_{diff}(LPF) = 2R_X C_{X3}$
- C_{X3} reduces common-mode capacitance imbalance → AC CMRR
- Choose $\tau_{diff}(LPF) >> \tau_{cm}(LPF)$
- Evaluate R_X errors -- CMR, Bias Current, Noise
- R_X may be omitted if transducer is resistive and close to amplifier

Figure 1.18

REFERENCES

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