High Frequency Current Mode Class-D Amplifiers With High Output Power and Efficiency

By

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High Frequency Current Mode Class-D Amplifiers With High Output Power and Efficiency

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By

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ABSTRACT

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A 13 watt Current Mode Class-D (CMCD) with 60% efficiency is presented. This amplifier is the highest power switch mode microwave power amplifier reported to date. The CMCD architecture is an improvement over the Voltage Mode Class-D in that the parasitic reactance in the active device can be absorbed into the tank circuit resulting in a zero voltage switching condition. Additionally, two similar amplifiers are presented for use with advanced linearization techniques.

Dedication

Joseph Francis Martinet
N6ELW
November 24 1960 – February 12, 2003

I dedicate this thesis to my Uncle Joe who inspired me at a young age to become an engineer, and always gave me advice and support for my fascination with all things wireless and microwave.

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I. Introduction

a. Motivation - Why Investigate Switching Mode Power Amplifiers?

The 1990's saw the rapid development of the wireless telecommunications industry around the world. Wireless handheld devices (phones, pagers, two-way messaging devices, etc.) have become massively popular, spurring a need for new electronic components and circuits in both mobile and base station systems as competition drives the introduction of expanded capabilities.

Consuming and wasting the most power in these new wireless communications systems are the RF power amplifiers. To extend battery life in mobile units, and reduce operating costs of base stations, new amplifiers must be developed to replace the traditionally inefficient, old designs currently in use.

Broadband wireless data services and multiple-carrier next generation systems specify amplifiers with a high degree of linearity over a broad frequency range. Base station amplifiers of today employ many complex techniques to meet this requirement, with accompanying low efficiencies of perhaps 10%. Handset power amplifiers also suffer from efficiency problems, often more critical than those for base stations.

For many decades, linear power amplifiers of the Class-A and Class-AB type have been employed as RF power amplifiers for cellular base station systems. These amplifiers are based on the operation of a transistor in its linear mode. As such, they

are limited in their ability to efficiently amplify RF signals. In 1975 N.O. and A. D. Sokal published the first paper [1] on a new class of RF amplifiers wherein the transistor is operated as a switch, or in its saturated mode. The losses associated with the saturated mode of operation are potentially very close to zero, resulting in amplifiers with perfect theoretical efficiency and very high (up to 97%) measured efficiency.

Switching mode amplifiers have seen many years of use in various electronic systems including audio power amplifiers and switching power supply circuits. They have however been traditionally limited to a low frequency and power product, with relatively modest power of as much as one and a half a watts (figure I-1) at higher frequencies.

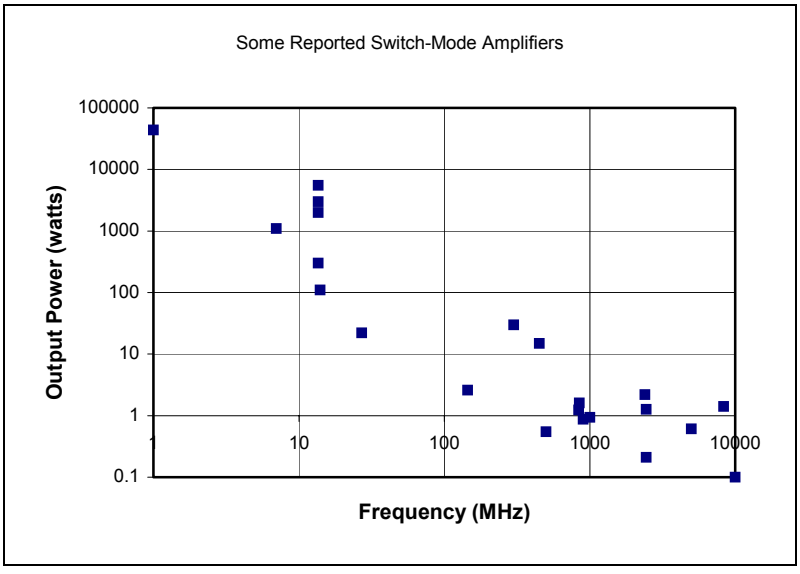


Figure I-1: Some reported switch-mode power amplifiers.

Fundamental limits (such as large parasitic capacitance) exist which prevent many transistors from working well at high power and frequency in the class-E configuration, the most popular switching mode scheme. Until recently, the most significant improvements in high frequency output power have come from the use of improved device technologies.

Switch-mode amplifiers are by nature non-linear amplifiers and are not suitable for all applications without additional equipment. Frequency and phase modulated communications systems are well suited to take advantage of switch-mode amplifiers, as the need to maintain an amplitude envelope is not necessary. Other systems however, require advanced techniques to maintain amplitude linearity when using non-linear amplifiers. One of these techniques is called LiNC (Linearization of Non-linear Components). The LiNC technique allows the use of two non-linear amplifiers to create a fully linear signal. Approaches such as LiNC allow the use of nonlinear amplifiers for virtually any communications mode. There is however a lack of RF amplifiers which at the same time produce high power at high frequencies, efficiently.

b. Outline of Thesis Approach

The topic of this thesis is the design, development and testing of a Current Mode Class D (CMCD) amplifier. At the time of writing, it is the highest power microwave (1 GHz and above) switching amplifier reported. This version produces

13 watts at 60% efficiency at 1 GHz. The next section contains a discussion of why the CMCD topology may be the topology of choice for many high power, high frequency amplifiers. It exhibits no fundamental limit on the frequency of operation, nor on output power, though practical limitations of course exist, and will be discussed. The CMCD PA also offers the highest degree of transistor utilization. That is, for a given transistor, the CMCD topology will take advantage of its capabilities more than any other topology.

This thesis is structured in a similar way to the development and testing of the amplifier. The next section discusses the topology and general characteristics of the CMCD amplifier, justifying its development and illustrating its differences among other switch-mode amplifiers. The development begins with a description of the circuit and active devices, then simulation results. Next, the details of how the final circuit design was developed are described. This includes construction details, tuning methods, and results. Next, the measurements section covers the analysis and operation of the three amplifiers that were built. After discussing the development and testing, the final sections are devoted to analysis of the measurements and a discussion of the results of simulations and measurements.

II. CMCD Topology

c. Why Current Mode Class-D

In section I, the use of switching amplifier architectures was introduced and justified. This section will seek to justify the investigation and development of the Current Mode Class-D amplifier. Important differences exist between the popular switch-mode architectures and CMCD, and this section will illustrate these differences and explain why the CMCD architecture is better suited for some applications.

Switching amplifiers come in many varieties with class designations from D through S. All of these classes of amplifiers differ from their linear counterparts in that the active device is used as a switch rather than as a linear amplification element. Many variations of these basic modes have been developed and published, with subsequently increasing performance. Classes F and E form the basis of most switch-mode RF power amplifier designs, while Class D has not seen much application.

d. Differences and Similarities Between CMCD, and F, D, inverse F, EF_{odd}

A Class-F amplifier is one which is defined as "having a halfwave rectified sine wave for its RF current and a maximally flat third harmonically enhanced sine

wave for its RF voltage, has been termed a class F amplifier...” [2]. The waveforms for a Class F amplifier are shown in Figure II-1.

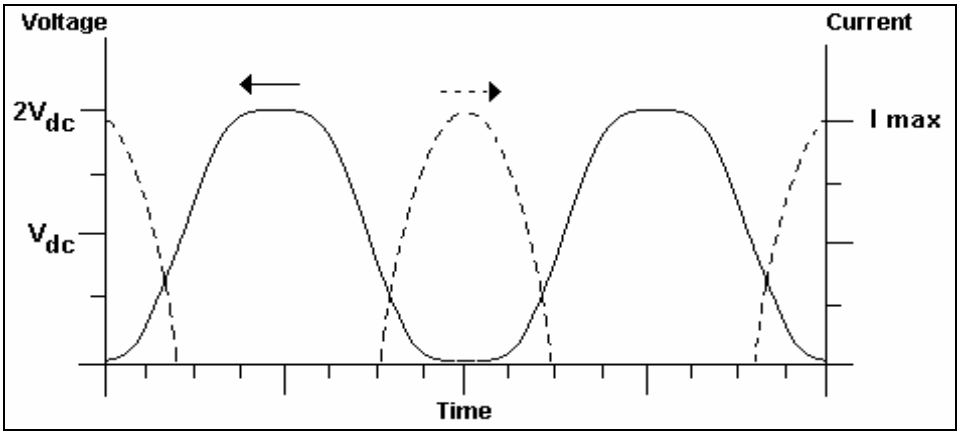


Figure II-1: Class-F waveforms

Often, Class F amplifier designs achieve this result by intentionally squaring the voltage waveform through controlling the harmonic content of the output waveform. This is commonly accomplished by implementing an output matching network which provides a high impedance ‘open circuit’ to the odd harmonics and low impedance ‘shorts’ to even harmonics. This results in a squared off (though for class-F, truly squared) voltage waveform. Traditionally, the third harmonic only is peaked. Figure II-2 shows an example of a class-F amplifier.

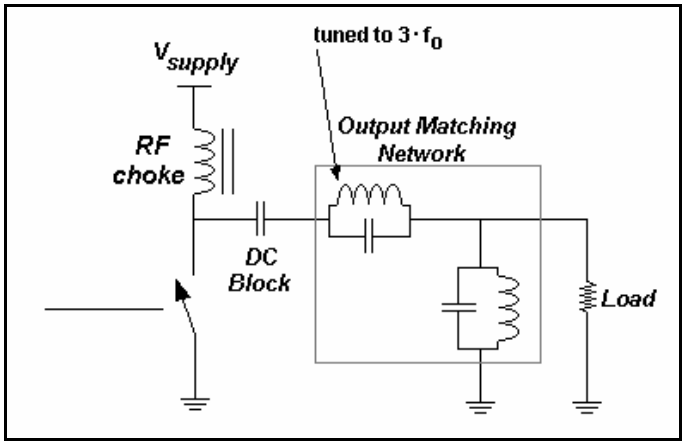


Figure II-2: Class-F amplifier

Class-F amplifiers are capable of high efficiency (88.4% for traditionally defined class-F, or 100% if infinite harmonic tuning is used). Class-F amplifier design is difficult mainly due to the complex design of the output matching network. At microwave frequencies, it becomes difficult to fabricate Class-F amplifiers, as capacitors and inductors function poorly, and planar structures become hard to realize, especially when tuning multiple harmonics. The ideal Class-F architecture, when tuned with many harmonics, and when the losses in the switch are neglected, can achieve a "maximally-flat" condition [3] wherein no overlap of voltage and current waveforms take place. Under this condition, no power is dissipated in the switching element.

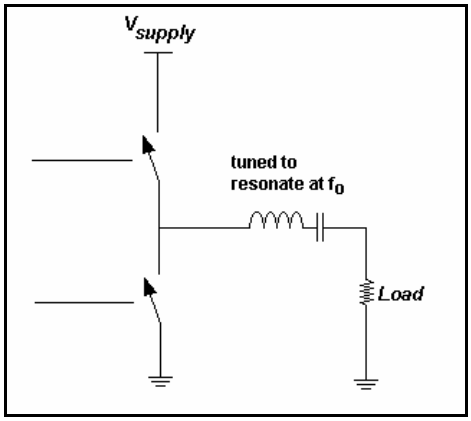


Figure II-3: Class-D amplifier

The Class-D amplifier architecture (Figure II-3) has been around for some time and has seen extensive use in low frequency and audio frequency applications. The traditional, or voltage mode Class D amplifier is defined as a switching circuit that results in the generation of a half-sinusoidal current waveform and a square voltage waveform as seen in figure II-4.

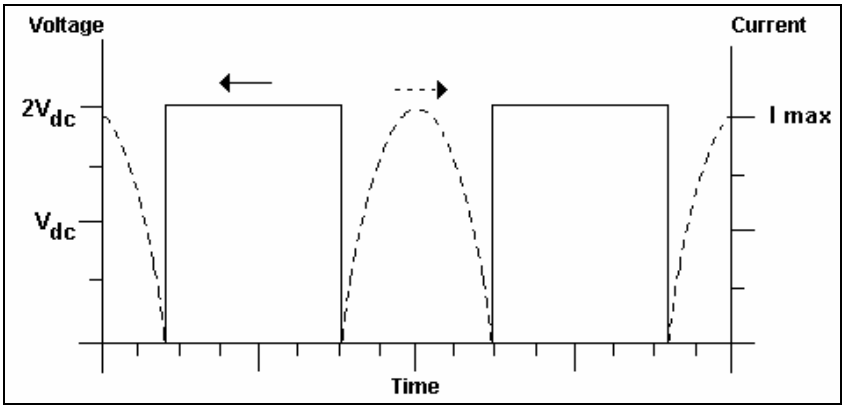


Figure II-4: Class-D voltage and current waveforms

Traditional Class-D amplifiers suffer from a number of problems that make them difficult to realize, especially at high frequencies. First, the availability of suitable devices for the upper switch is limited. Secondly, device parasitics such as drain-source capacitance and lead inductance result in $\frac{1}{2}C \cdot v^2$ or $\frac{1}{2}L \cdot i^2$ losses in each cycle. If realized, (they are common at low RF and audio frequencies) Class-D amplifiers theoretically can reach 100% efficiency, as there is no period during a cycle where the voltage and current waveforms overlap.

A continuum exists between the Class F and Class D amplifiers insofar as the waveforms progress from a nearly square drain voltage, to a fully square drain voltage shape. Real amplifiers operating under these circumstances are then best categorized by the circuit topology used, and the methods used to achieve the desired result. No real amplifier can be a true Class-D, as non-zero switch resistances and capacitive as well as inductive parasitics restrict the shape of the drain voltage waveform.

An alternative exists to the Class-F and Class-D amplifier schemes, which also results in highly efficient switch-mode amplification. The Class-E architecture, first proposed by Sokal and Sokal in 1975 [1] achieves high efficiency by careful shaping of the "voltage and current waveforms to prevent simultaneous high voltage and high current in the transistor; that minimizes the power dissipation, especially during the switching transitions." [4]. Explicitly, a load network is designed such that the voltage at switching time is zero, or very small, and the slope of the voltage waveform is also zero. This results in no capacitive discharge loss and zero overlap in

the current and voltage waveforms. Figure II-5 shows the typical waveforms of a Class E amplifier.

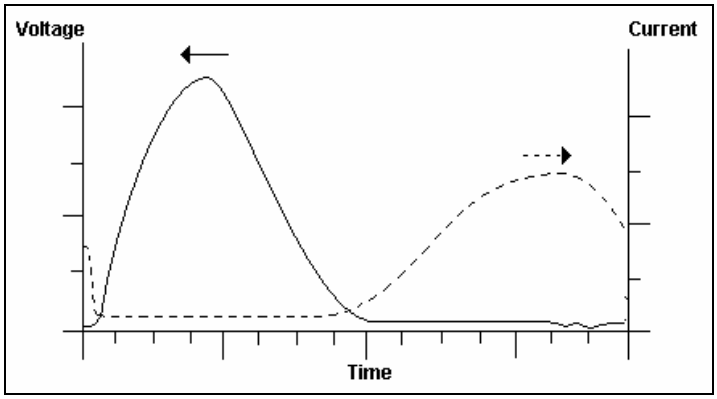


Figure II-5: Typical Class-E voltage and current waveforms

The most obvious difference in the voltage and current waveforms between the Class-E and Class-F/Class-D is that the current waveform of the Class-E amplifier is not square, or even close to being square. By the rules of Class-E amplifier design, it is not strictly speaking a half-sinusoid. Nevertheless Class-E amplifiers have been shown to produce high efficiency at high frequencies [4].

Class E amplifiers have shortcomings with respect to RF amplifiers that must simultaneously operate with high efficiency, high output power, and high frequency. At high power levels, the cost of transistors is very high, and the full utilization of a transistor is critical to making cost efficient amplifiers. A Class-E amplifier will exhibit an upper limit on its frequency of operation based on the output capacitance required for the output matching circuit that produces the waveforms described and

shown above. Specifically, a Class-E amplifier (see figure II-6) for optimum efficiency requires an upper limit on capacitance Cs [5]. It is related to frequency of operation by the following expression:

$$C_P = \frac{P_{out}}{\pi f V_{dd}^2}$$

Equation II-1

Where Pout is the amplifier's output power, V_{DD} the supply voltage, and f the frequency of operation. This places a restriction on the value of C_P. If a given transistor has an intrinsic capacitance greater than $C_{P,max}$, it is not useable at the desired frequency. This Cs requirement implies that for high power at high frequencies, higher current densities are required, as the cross-sectional area of the switch corresponds directly to the device's intrinsic capacitance.

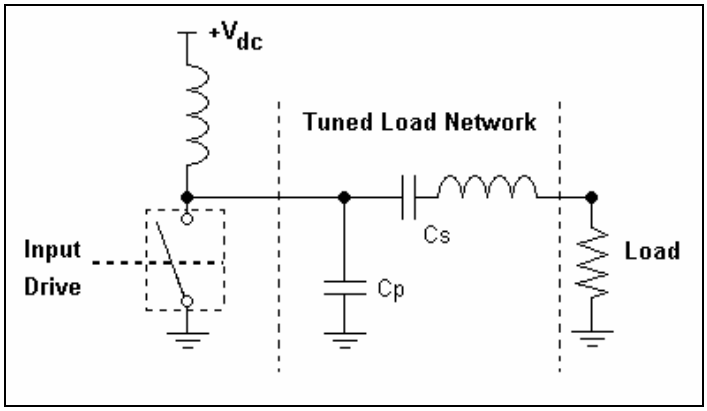


Figure II-6: Class-E amplifier

Class E amplifiers are relatively poor at exploiting a switching devices' ability to produce power, as the waveforms are far from square. Raab [10] defines a metric for an amplifier's utilization of a device's ability to produce power can be written as follows:

$$P_{\max} = \frac{P_O}{v_{\max} \cdot i_{\max}}$$

Equation II-2

Where P_{max} is the power utilization, P_O the output power of a given amplifier, and v_{max}, i_{max} the peak values of the voltage and current waveforms. For a Class E amplifier, the peaks are high and the shape of the voltage and current waveforms is peaky. Thus for a Class-E amplifier, P_{max} is small, as the V_{max}=3.56, and Imax=2.86. Therefore, Class-E has power utilization 0.0981. For Class D, the output power and CMCD as well, this utilization is 0.318. Power Utilization of 0.318 is the highest of any of the common amplifier topologies. So by comparison, the Class-E amplifier makes poorer use of a given transistor than the CMCD, both in terms of power and maximum frequency.

In 2001, the "Current Mode" Class-D amplifier was proposed, built and tested [6]. The CMCD is fundamentally the inverse of the Class F/D amplifier. The waveforms are switched in as much as the current is a square and the voltage a half-sinusoid. Being a dual of the Class F/D, the CMCD achieves the same 100% theoretical efficiency, but is much easier to realize.

The CMCD amplifier shown in Figure II-7 uses two switches and a single tank circuit. The key advantage of the CMCD versus a Voltage Mode Class-D (VMCD) is that the device capacitance is absorbed into the tank circuit. The discharge effects resulting in lower efficiency are thus nulled, leaving the far less (but still existent) significant lead inductance as the sole source of loss. For large devices with multiple fingers, this inductance can be quite small. At high frequencies, the resistive loss of the transistor is present, though it is swamped by the losses attributed to capacitive or inductive loss.

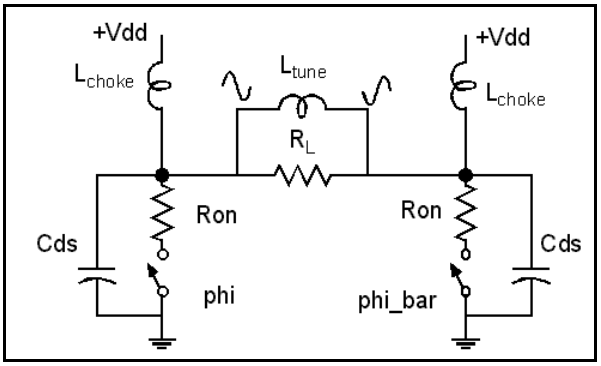


Figure II-7: Current Mode Class D (CMCD) amplifier

The CMCD architecture exhibits a number of benefits over the Class-E, Voltage Mode Class-D, and F architectures. In each case, the CMCD has performance benefits in terms of either maximum frequency of operation, maximum power output, or transistor utilization. For a given transistor, CMCD produces more power than any other design (equal for the case voltage mode class D). Additionally, there is no fundamental limit on the value of the shunt capacitance in CMCD, as it is included in the tank circuit. A tradeoff may be considered however for very large

devices between the Q of the tank and the output power. Because there is no restriction on Cs, the maximum usable frequency of the CMCD is much higher than for Class E, given the same transistor. Limits on usable frequency do exist however, in the form of the f_t of the device, etc.

Two more amplifier topologies exist which are similar to CMCD. Inverse Class-F produces the same voltage and current waveforms as CMCD, though usually under different design goals. Inverse F assumes that the active device is not actually switching, but is instead mildly saturated. This results in higher order harmonics having miniscule power, leaving only a few harmonics to be dealt with by the rest of the circuit. CMCD is designed with the intent to switch the active device well into saturation, reducing the transition time such that the current waveform may become more square. In the case of the new E/F amplifiers [8], the design is a mix between the tuning of Class-E and the waveform shaping of Inverse-F. Inverse-F, CMCD, and E/F_{odd} are remarkably similar and may be thought of as variations of each other. Topologically, CMCD and inverse-F are similar with CMCD being the push-pull version of inverse-F, and vise versa.

As the frequency of operation, bandwidth, and power requirements continue to expand, it is clear that new methods of power amplification are necessary. The CMCD architecture is a large step in the direction of increasing the product of power output and frequency for highly efficient RF PAs. Based on these motivations and the successes with the work of H. Kobayashi; J. Hinrichs; P. M. Asbeck [6], it was decided to take advantage of these benefits and build a high power high frequency,

highly efficient amplifier. The following sections outline the development and testing of a three CMCD amplifiers, with one producing a record 13 watts at 1 GHz with 60% efficiency. At the time of writing this is the highest power high frequency switch mode PA published.

III. Current Mode Class D Amplifier Design

a. The Circuit

i. Expected Mode of Operation/Heuristic Explanation

The well known Voltage Mode Class-D (VMCD) circuit can be characterized by its square switch voltage and half-sinusoidal switch current waveforms. Current Mode Class D (CMCD) Figure III-1(a) is the dual of VMCD, having a square switch current and half-sinusoidal switch voltage. These waveforms are illustrated in figure III-2 and can be approximated by the following series:

CMCD:

$$V_{switch} = V_{DC} + \tfrac{4}{3} V_{DC} \sin\theta - \tfrac{1}{3} V_{DC} \cos 2\theta + \ldots$$

Equation III-1

$$I_{switch} = I_{DC} - \tfrac{9}{8} I_{DC} \sin\theta - \tfrac{1}{8} I_{DC} \sin 3\theta + \ldots$$

Equation III-2

VMCD:

$$I_{switch} = I_{DC} + \tfrac{4}{3} I_{DC} \sin\theta - \tfrac{1}{3} I_{DC} \cos 2\theta + \ldots$$

Equation III-3

$$V_{switch} = V_{DC} - \tfrac{9}{8} V_{DC} \sin\theta - \tfrac{1}{8} V_{DC} \sin 3\theta + \ldots$$

Equation III-4

V_{switch} is the voltage across either switch and I_{switch} is the current through either switch.

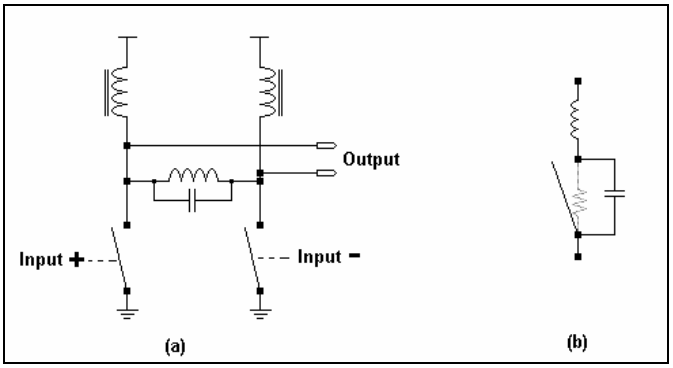


Figure III-1: CMCD amplifier (a) and non-ideal switch model (b)

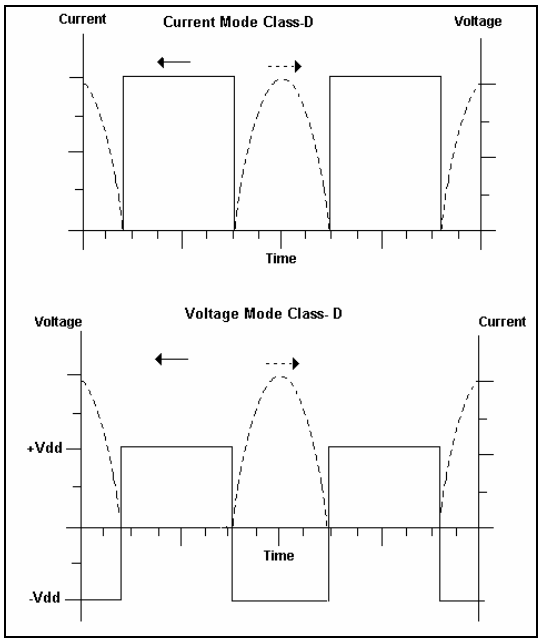


Figure III-2: CMCD versus VMCD waveforms

The CMCD amplifier is operated with the switches driven out of phase, such that one is open and the other closed at any given time. This effectively 'steers' the current from one branch to the other, generating a corresponding sinusoidal voltage response across the tank circuit.

With non-ideal switches as in the case of virtually all semiconductor devices, parasitics exist which affect the amplifier's performance. In transistors, these parasitics take the form of lead inductance, channel resistance, and parallel capacitance. These are the dominant parasitics for amplifier use. When either of the switches of the CMCD amplifier (figure III-3) closes, the parasitic capacitance adds in parallel to the capacitor in the tank circuit. This parallel summing is true for the case when the inductance and resistance (figure III-1(b)) are very small. For many modern devices and especially for integrated devices, this is a reasonable approximation. It is however a reason why CMCD cannot be 100% efficient in practice. In a VMCD amplifier, the inductance rather than the capacitance is absorbed into the tank circuit. Because parasitic capacitance typically swamps inductance, VMCD is limited to low frequency operation.

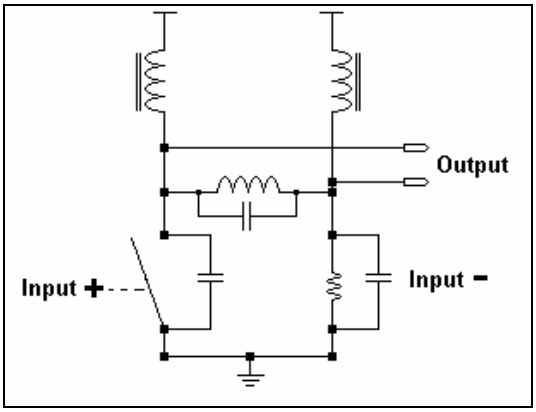


Figure III-3: CMCD in operation (one switch closed).

Because the tank circuit is a resonator, at the instant the switch opens or closes, the voltage across the switch is zero. With zero voltage switching (ZVS), the capacitor is shorted out. Even if the closed switch has some resistance (as seen in Figure III-3), power is not lost if the ZVS condition is met.

To form the voltage and current waveforms, harmonics of the tank resonant frequency must be treated appropriately. As seen in the voltage and current equations (III-1 through III-4), the drain voltage contains even harmonics, so these must 'see' a high impedance presented by the output circuitry and the DC feeds (RF chokes). Odd-mode harmonics are shorted through the tank circuit capacitance and cancel out. For the current waveform, odd harmonics must flow while evens are open

Nearly ideal waveforms are critical to maximizing efficiency as the overlap of the current and voltage waveforms correspond to power dissipated in the switch. Also, ZVS must be approximated to avoid excessive losses. As the number of harmonics is increased, the peak voltage and currents increase. Using the equation for switching voltage in CMCD (III-1), which is limited to two harmonics, the peak

voltage (for $\theta=\pi/2$) is $8/3(V_{DC})$. However, the ideal waveform is a sinusoid for half the period and integrating gives:

$$\int_0^{2\pi} V_{switch} = 2\pi \cdot V_{DC}$$

Equation III-5

$$\int_0^{\pi} V_{peak} \sin\theta \cdot d\theta = 2V_{peak}$$

Equation III-6

$$2V_{peak} = 2\pi \cdot V_{DC}$$

Equation III-7

$$V_{peak} = \pi \cdot V_{DC}$$

Equation III-8

An upper limit of πV_{DC} may be reached by the CMCD amplifier, so V_{DC} must be set such that

$$V_{DC} \leq \frac{V_{breakdown}}{\pi}$$

Equation III-9

Power utilization was mentioned in Section II and here the calculation of the power utilization is given for the CMCD amplifier. The result holds for both CMCD and VMCD, as they are duals.

The power output of a CMCD amplifier is given in equation III-10, where V_1 and I_1 are the fundamental components of the Fourier series of the respective waveforms.

$$P_{out} = \tfrac{1}{2} V_1 I_1$$

Equation III-10

Since the CMCD amplifier is balanced, we can measure a voltage across the output terminals as being the differential voltage across the tank circuit. For a sinusoidal waveform, $V_1 = \frac{V_{\max}}{2}$. With $V_{diff} = 2 \cdot V_1$, $V_{diff}=V_{max}$. For current, $I_1 = \frac{4 I_{DC}}{\pi}$ for a square waveform. From before, we have that $V_{\max} = \pi \cdot V_{DD}$. Substituting to evaluate P_{out}, we get $P_{out} = 2 \cdot V_{DD} I_{DC}$. For maximum voltage and current, $I_{\max} = 2 \cdot I_{DC}$. Substituting into equation II-2, $P_{out} = \frac{V_{\max} I_{\max}}{\pi}$ and $P_{\max} = \frac{1}{\pi}$ or approximately 0.32.

The amplifier must be suitably driven out of phase, the outputs summed, and DC fed to each device. The next section details the function of these specific circuit elements.

ii. Detailed explanation of operation of each component

Figure III-4 below shows the complete amplifier circuit with input and output hybrids, DC feeds, matching networks, and tank circuit.

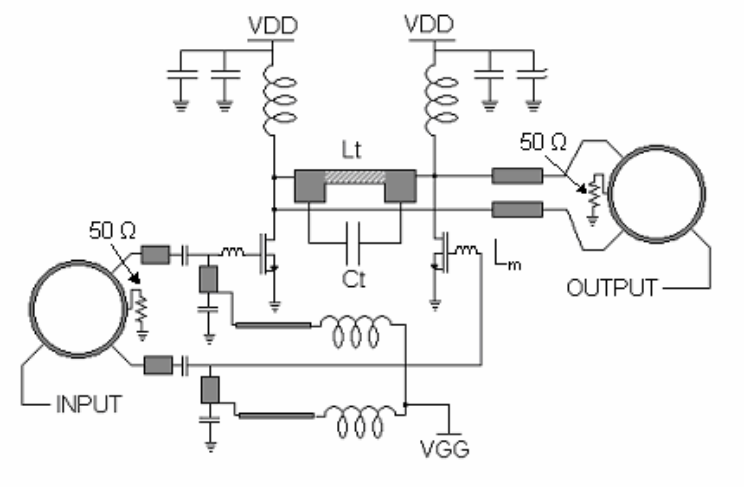


Figure III-4: CMCD amplifier circuit

The CMCD architecture requires that the switches be driven out of phase. For lab testing this amplifier will be driven by a single source though other applications and configurations do not necessarily require this. At the input of the amplifier a hybrid is required to delay the phase of one channel 180° from the other. Several options are available and three were ultimately used in the amplifier design and construction.

For preliminary simulations, a magic-tee was used. This circuit can be implemented in microstrip or waveguide, but requires large dimensions for the frequency of interest and materials available. Further, the magic-tee provides similar impedances to the operating frequency and its harmonics. Harmonic treatment is

important to the input, but even more important to the output summing hybrid, as it aides in shaping of the switch voltage and current waveforms.

The hybrid used in later simulations and the first constructed amplifier is a coherent splitter (a Wilkinson divider for simulation purposes) followed by a half-wave transmission line (coax or stripline) to one port, and no delay to the other. In practice, two coax lengths were used, with one being one half wavelength longer than the other. This balun configuration provides worse impedance control for the various harmonics.

A rat race hybrid is a transmission line circuit (as pictured on the amplifier schematic in figure III-4 characterized by its circular structure. Figure III-5 shows the wideband phase and magnitude input reflection coefficients for the two input ports (when configured as a summer for the output network). A close examination of the region around 2 GHz reveals that a sharp dip occurs around 2.07 GHz with a corresponding impedance of greater than 56 ohms. Tuning the combiner allows fine adjustment of harmonic impedances as documented in section IV(c).

The impedances of each structure are compared in table 1.

Simulated Harmonic Impedances for Hybrids			
Harmonic	Rat Race Hybrid	Balun	Magic Tee
fo	48.75 Ω	41.45 Ω	21.43 Ω
2fo	18.3 Ω*	25 Ω	36.5 Ω
3fo	40 Ω	35.7 Ω	52.7 Ω

Table III-1: Simulated Harmonic Impedances presented at the inputs to various hybrids with unused ports terminated into 50 ohms. *(56 ohms with tuning)

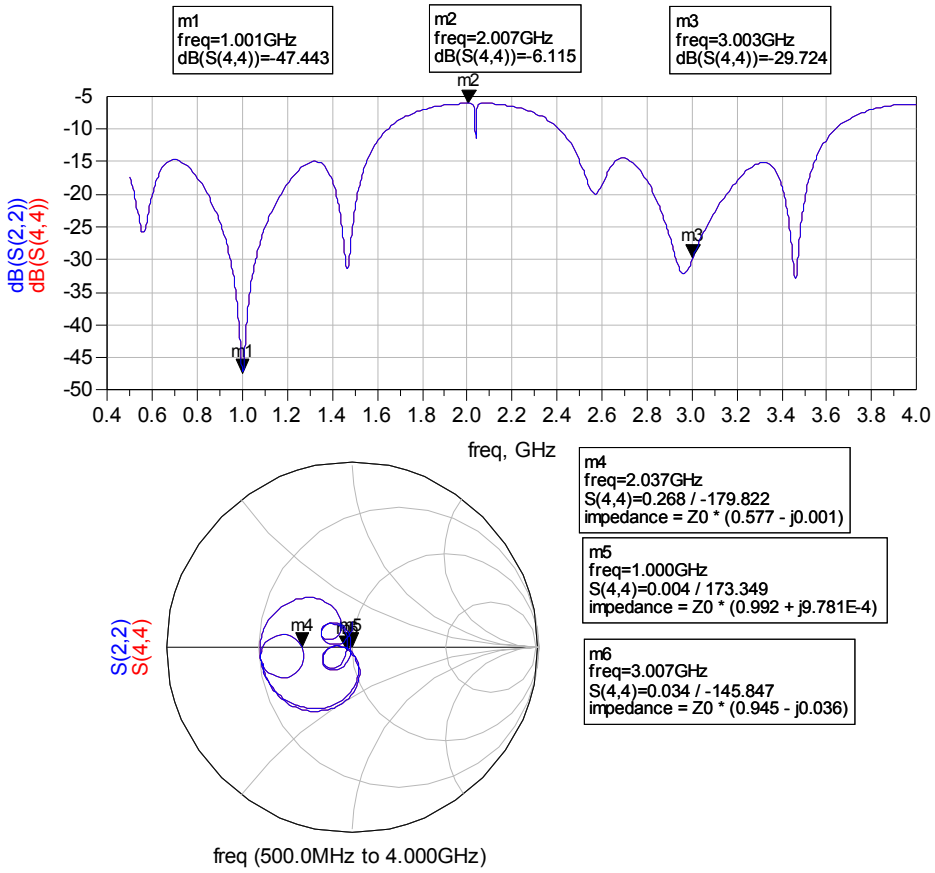


Figure III-5: Rat Race Combiner input reflection coefficients

The next element of the circuit is the input matching network. For simulation purposes, a series capacitor, shunt transmission line network was designed by maximizing the voltage swing at the input node of the transistor. The capacitor is 940 pF and the transmission line is 6.4° long and 50 ohms characteristic impedance. This input matching network is not the same network used in the constructed

amplifier. The input matching network for the constructed amplifiers is detailed in section IV(c).

The tank circuit is composed of an inductor and capacitor with accompanying parasitic resistance. The parasitic resistance R_p limits the performance of the amplifier, as it contributes to the loss in the tank circuit. The capacitor of the tank is a parallel combination of the tank capacitor and the intrinsic device capacitance. Package and lead parasitics, as well as printed traces present inductance between the drain of the transistor and the tank. This limitation will prevent perfect operation and tuning of the tank circuit.

Designing the tank circuit is fundamentally a tradeoff between harmonic control, amplifier bandwidth, efficiency, and power output, within the constraints of available components. Modern chip inductors can have series resistance below 0.1Ω and printed inductors considerably less. High quality ceramic chip capacitors may have series resistance of 0.06 ohms or less[11], representing the dominant series resistance for this circuit.

The following equations are used to generate values for C and L, the tank circuit component values. Choosing a Q sets the bandwidth. For this amplifier a Q of 5 was chosen. A high Q will limit the operating bandwidth of the amplifier but will help to control the harmonics. For large values of Q, component uncertainty will make construction difficult, and the amplifier will operate only in a narrow band of frequencies.

$$\omega = 2\pi f$$

Equation III-11

$$BW = \frac{\omega_0}{Q}$$

Equation III-12

$$Q = \omega_0 C R_P$$

Equation III-13

$$R_P = R_{Inductor} + R_{Capacitor}$$

Equation III-14

$$C_o = \frac{QR_P}{\omega}$$

Equation III-15

$$L = \frac{1}{\omega^2 C_o}$$

Equation III-16

$$C = \left(C_o - C_r\right)$$

Equation III-17

Lastly, the DC feed performs the important task of presenting a high impedance to any RF, while allowing the switches to pull large amounts of current quickly. In the case of a wideband amplifier, the DC feeds must respond over an

associated wide bandwidth. The DC feed (Figure III-6) used in the constructed amplifier consists of a high impedance (15 mil wide) line in series with a 82 nH chip inductor and a surface mount integrated pi-filter[1] to keep out unwanted low frequency noise from the power supply leads. A pair of 10 pF and 10000 pF chip capacitors are used as a current buffer. For simulation purposes, a simpler feed is used, as the simulator's power supply is ideal.

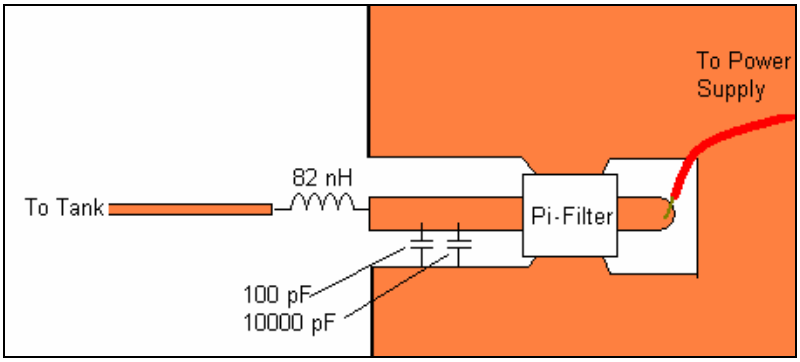


Figure III-6: DC Feed Detail

b. Devices Used

High power RF amplifier design (where power output is greater than 1 or 2 watts) has for many years involved a considerable amount of 'black magic' in the design process. Characterizing high power RF transistors is difficult, and without a clear understanding of the device, totally a priori design is impossible. Few companies provide design models of their transistors, and few have been published. Since a high power CMCD amplifier had never been built, it was important to have a well understood, characterized device. Luckily, another student, David Choi had as

[1] Pi-filter from Spectrum Controls, part number PSM1-402Z-05T

part of his PhD thesis [5], created a model of a high power transistor, the Ericsson PTF-10135 LDMOS FET (See appendix A for data sheet).

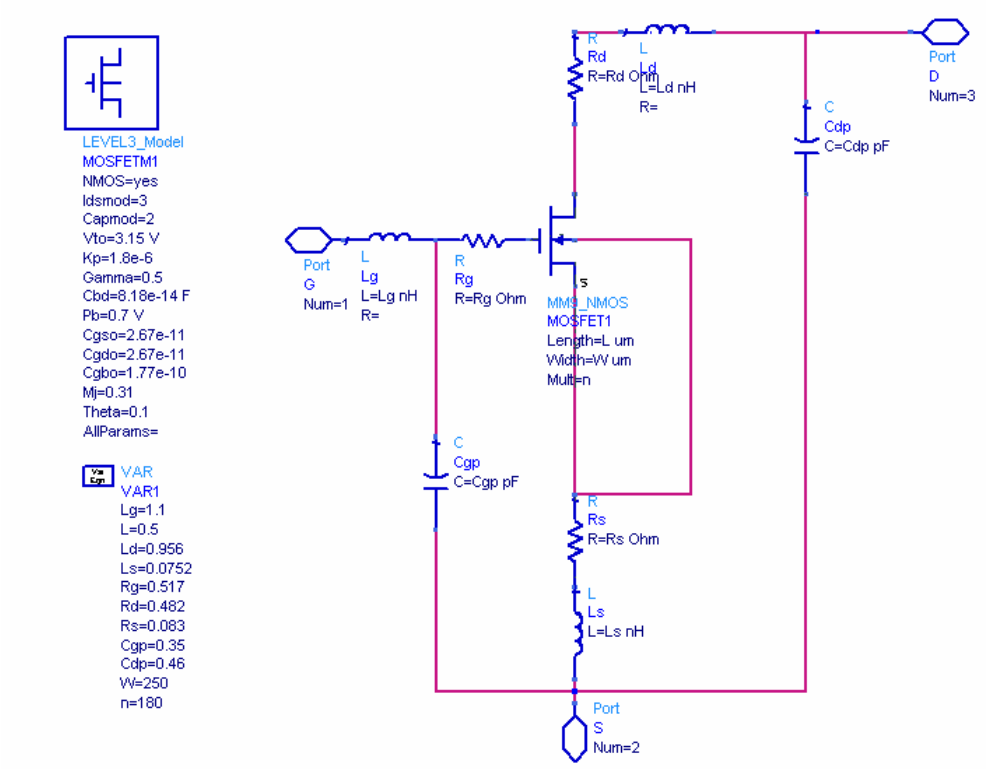


Figure III-7: Device Model

The transistor model (figure III-7) was used in Agilent's Advanced Design System software package for simulations. Some notable characteristics of this transistor are listed in table 2.

Parameter	Value
Cds (20V bias)	6 pF
Breakdown Voltage	65V
Gate On-Voltage	3V
Output Power (linear operation)	5 watts

Table III-2: Selected Device Parameters

c. Simulation Results and Predictions

i. Ideal CMCD (ADS Using Ideal Switch Model)

To test the concept of the CMCD, an ideal switch based amplifier was designed and simulated. The schematic diagram is shown in figure III-8. All components are idealized except for small switch resistance added to prevent oscillations in the output. A series LC resonator is employed to improve the harmonic control of the amplifier. This was omitted in the constructed amplifier as it was discovered that its benefit was lost due to component losses, and since the inductance was small, its effect on the second harmonic was small.

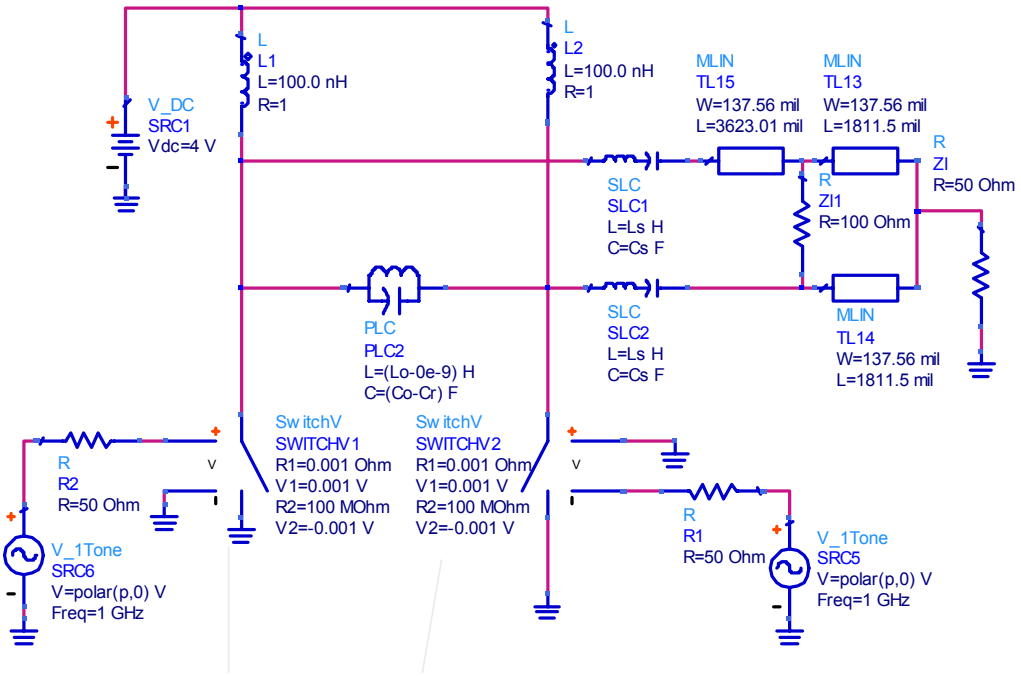


Figure III-8: Switch-based CMCD

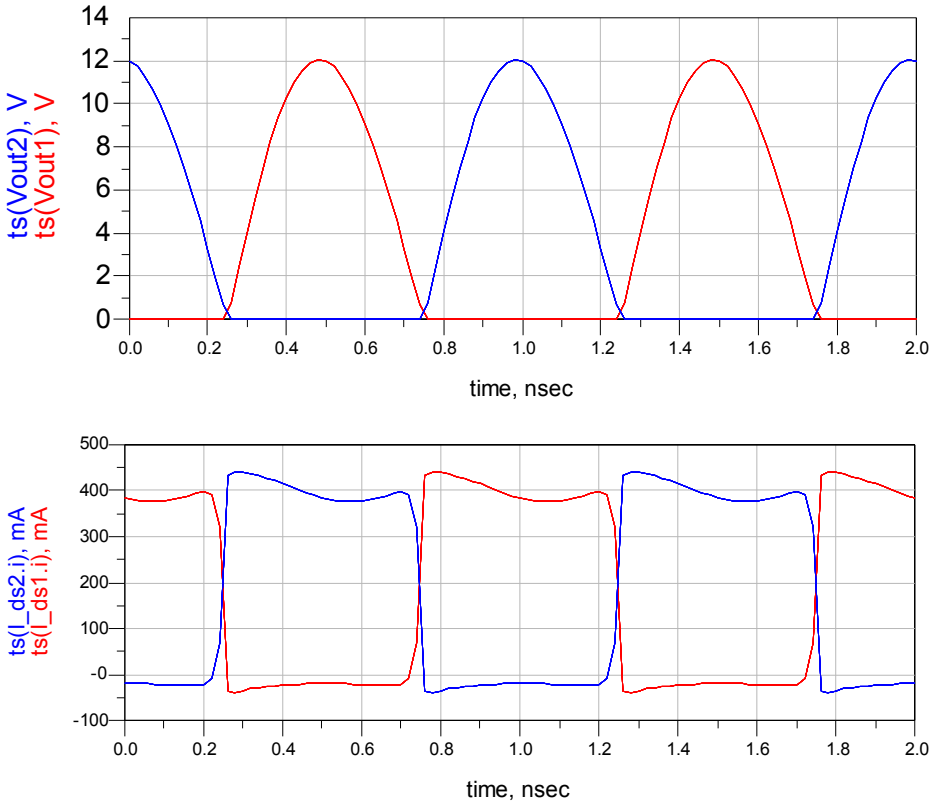


Figure III-9: Drain voltage and current waveforms for switch CMCD

The results of the switch-based amplifier show that very high efficiency can be achieved (93.1%) with some resistance in the switch model. The drain voltage waveform is almost ideal, with the peak voltage at 3 times the supply voltage, while the drain current exhibits some slight ringing. Moving from an ideal switch model to a transistor, complete with parasitics, it become clear that these waveforms will not be as clean.

ii. With Device Model

Using the device model from the previous section, a simple amplifier was designed. The specific design elements are detailed in section III(a) including the input and output hybrids (magic-Tees in this case) and input matching networks.

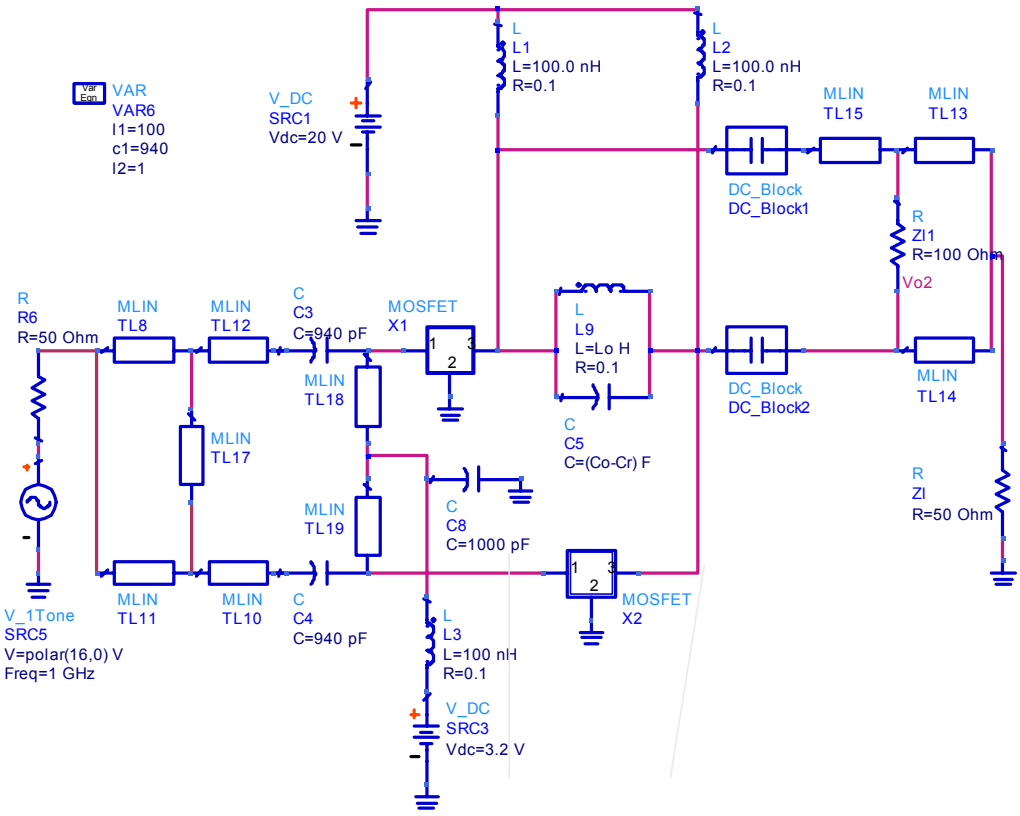
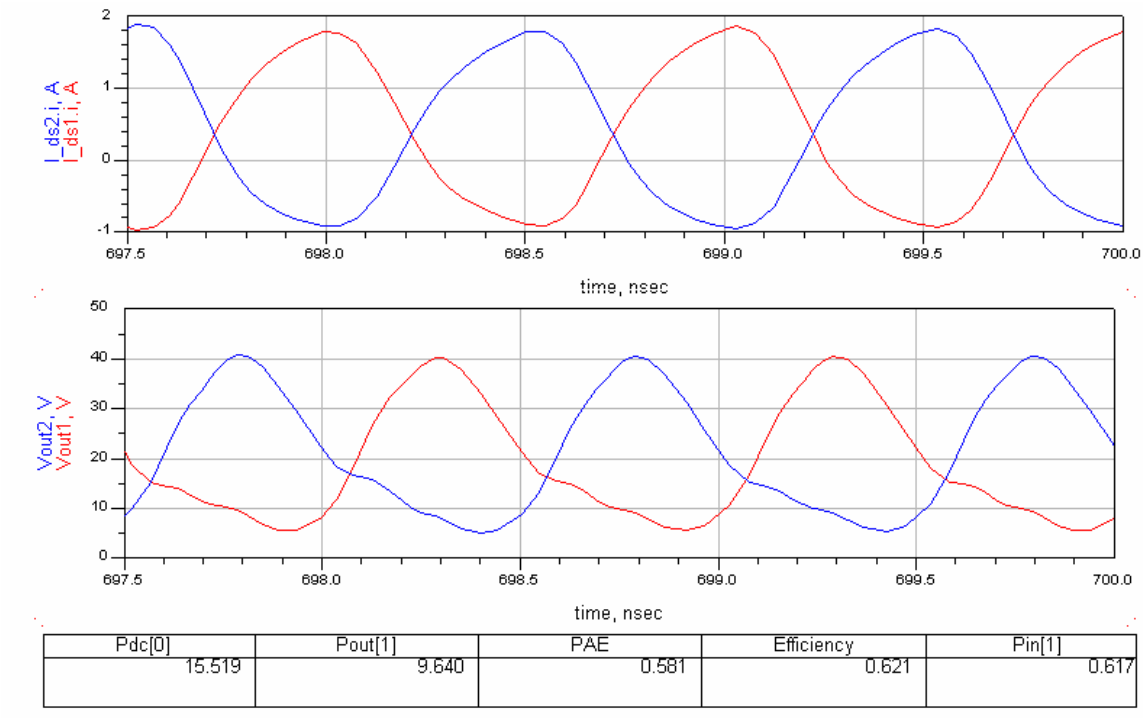


Figure III-10: Amplifier test circuit

iii. Early Simulations with simplified structures (Ideal Matching Networks, Etc.)

Initially, a transient simulation was performed to investigate the performance of the amplifier. Transient analysis simulations were used initially as convergence in Harmonic balance simulation was difficult to achieve. Eventually though, harmonic balance simulations were possible though not at the high input drive levels required to obtain corresponding high output power. Figure III-11 shows the results of the initial transient simulations. The drain voltage and current waveforms are shown along with parameters of the amplifiers performance.



Pdc[0]	Pout[1]	PAE	Efficiency	Pin[1]
15.519	9.640	0.581	0.621	0.617

Figure III-11: Simulation results

From figure III-11, it is apparent that the waveforms are not ideal. The drain currents are not square, and the drain voltage, while close to half-sinusoidal, have a significant amount of lag in their return to zero. Because the tank circuit is not ideal (due to the lead and package inductance of the transistor), inductive discharge occurs when the switch opens. This may be the cause for the lag in the drain voltage waveform. Adjusting the values of the tank components did little to improve the waveforms. Another factor affecting the waveform shape is the harmonic treatments. In this simulation, the half-wave transmission line balun was employed for the output combiner, which does not present the ideal termination for harmonics.

iv. Full Layout Based Simulations

The next step in the simulations was to model more closely the circuit that was to be built, especially the tank. By adding components incrementally, the effects of each component on the circuit performance could be more closely tracked. By concentrating on particular elements, it was possible to fine-tune for optimum performance.

Critical to the high efficiency operation of the CMCD amplifier is the correct configuration of the tank circuit. Since a relatively high Q was chosen (for harmonic control purposes) the value of the inductance in the tank was small, approximately 2 nH. This meant that the contribution to the total inductance by the printed circuit

could be significant, leading to a difference in the value of the inductor (made from a printed circuit trace) from that which was designed.

Modeling the 2-dimensional structure of the output network required an electromagnetic simulation, as its structure is complex. Unfortunately, this 6-port network could only be modeled in terms of its scattering parameters (s-parameters). This presents a problem to transient simulations, as long (greater than one period of the lowest frequency used) time delays are not incorporated into S parameters. A harmonic balance simulation was required to simulate the amplifier using this network model.

The harmonic balance simulator engine in ADS does not converge with negative drain voltages in MOSFET models and as a result, when simulating the amplifier, at input power levels in excess of roughly ½ watt, convergence was not possible. A drive level of close to 1 watt is necessary to achieve full output power. At this level of input power level the amplifier will not operate with great efficiency, as the slope of the input voltage waveform is small enough to drive the transistors into linear operation for too long. With power being dissipated during linear operation, the overall efficiency drops.

Harmonic balance simulations were performed at the reduced input power however, and the following results were produced. Figure III-11 shows the drain voltage and currents measured internally to the device.

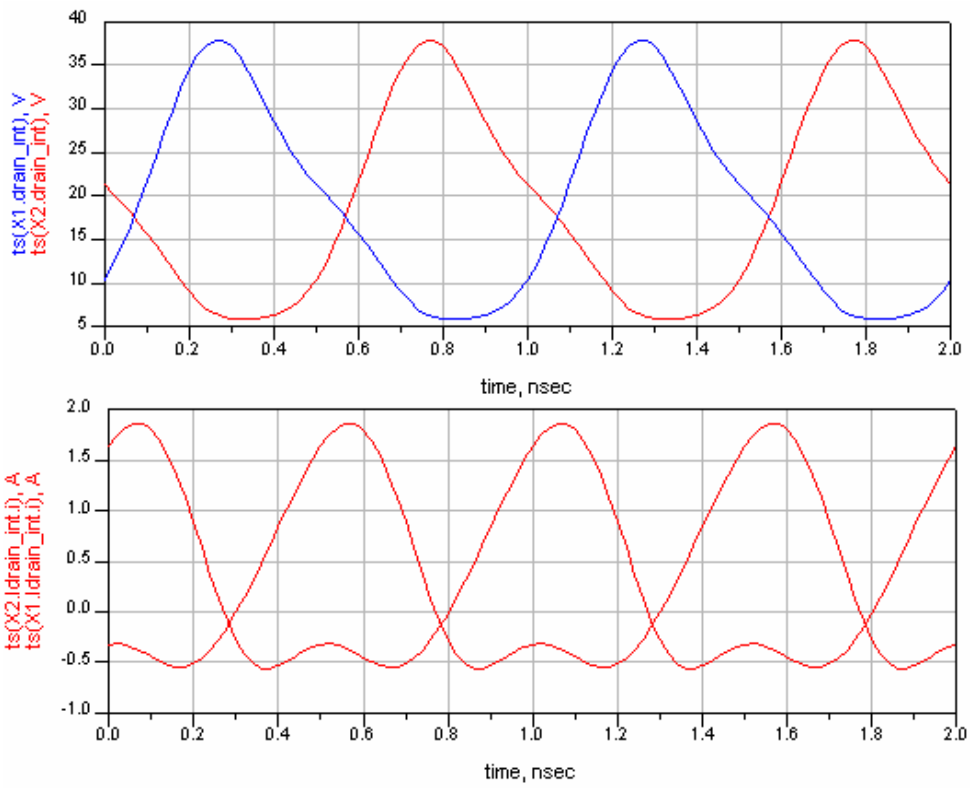


Figure III-12: Internal Drain Voltage and Currents (simulated)

At the drain of the transistor, the voltage waveform exhibits some of the lag seen in the previous simulation though it is less pronounced. The drain current, while not square, behaves better, as it stays very close to zero when the switch is off, thereby reducing the overlap of the voltage and current waveforms.

As more advanced and developed simulation tools become available, as well as better passive device models, simulations such as these will function better and provide more accurate results.

IV. From Schematic to Actual Circuit

a. Construction Considerations

Converting the simulated circuit to a realizable circuit required an examination of the sensitivities of the circuit to component parasitics and to implementation details such as printed circuit fabrication and its effects on circuit performance.

Discrete components for the amplifiers are used for several purposes. In the case of the input and output bypass capacitors, a short circuit at the fundamental is required. The capacitors chosen were measured on a network analyzer to have a series resonance at approximately 1 GHz. The value of 22 pF is less important than the requirement of self-resonance, which ensures a short circuit at the fundamental. Ceramic capacitors, such as the one used in this circuit have low transmission losses at high frequency, which is critical for high efficiency, and reliable high power operation.

Supplying DC current to transistors in RF amplifiers requires special attention to component parasitics, even those that are not apparent at the carrier frequency. The DC feed must act as a low impedance source from DC to the maximum modulation frequency, but as high impedance across the final bandwidth (centered around the carrier). For our purposes however, since the signals used are of very low bandwidth, a high impedance feed for all frequencies will suffice.

The current source for these amplifiers consists of a Coilcraft 82 nH inductor connected to the drain of each transistor followed by a pair of porcelain ATC B-size chip capacitors with values of 10000 and 100 pF respectively. Finally, a Spectrum Controls feed-through capacitor (4000 pF) acts as an RF short for the connection to the power supply. Figure IV-1 shows the results of a simulation of this bias network circuitry.

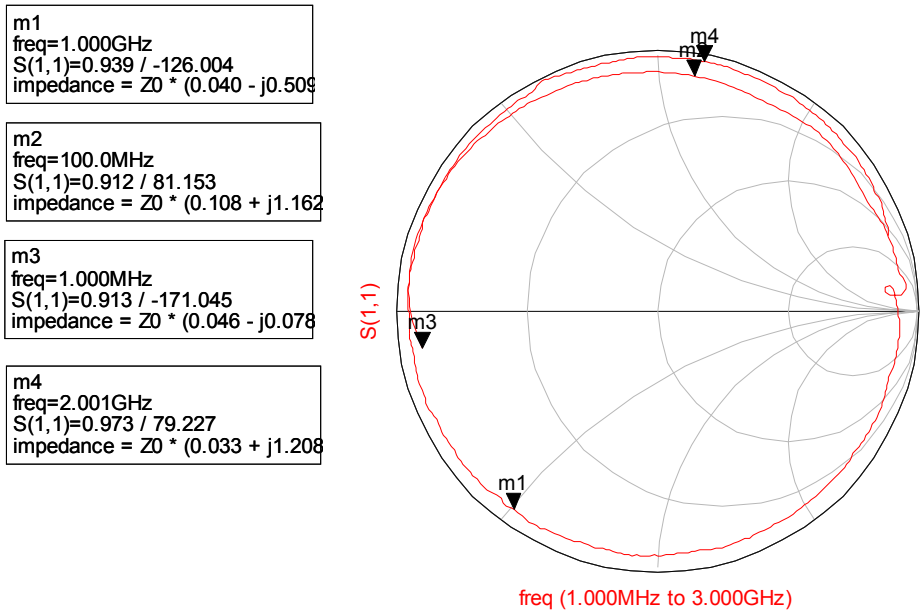


Figure IV-1: Simulated input impedance to DC feed network

Ideally the feed network should have no influence on the action of the tank circuit. Practically however, the DC feed circuit de-tunes the tank, as the Q of the feed network is not infinite. In this circuit the Q of the tank is around 5. The 82 nH

inductor has a Q of 54 (at 900 MHz) [12]. Factors involved in choosing the inductor include series resistance, resonant frequency , and the inductance value. For the DC feed, the resonant frequency must be far enough away from the frequency of operation so that it does not present a low impedance and drain power from the circuit. This inductor's series resonance is at 1.7 GHz, well away form the 1 GHz carrier frequency, though fairly close to the 2^{nd} harmonic. From Figure IV-1, all frequencies are presented a high impedance to the DC feed path.

On the supply side of the inductors is a bank (two in parallel in this case) of capacitors, which must supply transient currents to the amplifier as the transistor switches on. The effective series resistance of these capacitors must be small through the entire modulation bandwidth as well as around the carrier frequency. Porcelain capacitors offer some of the lowest series resistances available at moderate capacitance and voltage ratings.

b. Prototyping Details

i. Printed Circuit Board Manufacturing

When prototyping discrete circuits at microwave frequencies there is a great need for high performance circuit boards. High performance for microwave experimentation means principally, 1) tightly controlled substrate dielectric constant, 2) low loss tangent dielectrics, 3) closely controlled conductor geometries of fine

resolution, and 4) good grounding. Commercial manufacturers use a variety of complex and dangerous chemical processes to create circuit boards. Good results can however be realized using fairly simple bench-top processes. These processes are not without disadvantages however, namely variability in the success of the process.

Making suitable printed circuit boards for microwave frequency projects is traditionally a task left to companies that specialize in the lamination, photolithography, and etching of high performance dielectrics such as PTFE and Alumina. These companies are capable of producing multi-layered boards of varying dielectrics and thickness with vias and precise cutouts. It is impractical to create much more than a single layer (with ground plane) printed circuit board in a lab, as precision alignment, presses, and adhesives required for multi-layer boards are not practically obtainable.

Many simple circuits will function well with only a single layer board. Being able to rapidly prototype, test, and adjust boards is of great utility in microwave experimentation. These are the two main motivations for making boards in the lab.

Two commonly used methods exist (at the time of writing) to quickly prototype circuit boards. The first type involves a mechanical cutting of metal. Tabletop CNC milling machines are sold commercially for the purpose of rapid circuit prototype and work well for low frequencies and fiberglass substrates. For microwave circuits however, photolithographic techniques are often superior. Photolithography has a number of advantages specific to microwave circuits including the ability to create smaller feature sizes. Microwave dielectrics such as

PTFE are not well suited to machining with a rapidly spinning end-mill and develop a roughness on every edge of conductor. Ceramic/PTFE composites (as used in higher dielectric substrates) dull the bits extremely fast. Rapid prototyping machines often suffer from an inability to maintain accurate cutting depth, resulting in boards with varied dielectric thickness. Photolithographic techniques are generally not susceptible to these problems.

The photolithographic technique used to build the circuit boards described in this thesis requires the use of only a few chemicals. Table 2 lists the materials required for PCB manufacturing.

Perhaps the most difficult aspect of lab-made circuit boards is achieving a good photo resist coating on the boards to be used. For this project, the bare copper clad boards were first sourced from the manufacturer as samples (Rogers) and then sent to a company called Injectorall Corp. At Injectorall, the board is dipped in resist, with a very flat surface profile as a result. The starting point of this process is an evenly coated copper clad (on both sides) bare circuit board.

Generic Name	Manufacturers	Part number	Source
Positive Developer	MG Chemicals,	418	Newark
Exposure lamp	MG Chemicals	416-X	Newark
Ferric Chloride	MG Chemicals	415	Newark
Isopropyl alcohol	Many	---	---
Clean water	Many	---	---
Graduated	Many	---	Physics Store Room
Plastic trays	Many	---	Physics Store Room
Safety equipment	Many	---	Physics Store Room
Foam brush	Many, MG	---, 416S	Bookstore/Art Store,

Table IV-3: Supplies Needed For Printed Circuit Board Manufacture

The following is a step-by-step guide to making circuit boards in the lab.

1. Generate artwork from a CAD/layout program and print onto transparencies. Print twice (for greater contrast) and align the two transparencies such that the artwork overlaps exactly. Tape the transparencies together at the edges to hold the alignment. Set aside.
2. Place the pre-sensitized circuit board (as mentioned earlier) beneath the mask made in step 1. Cover the mask with the Plexiglas plate and compress the sandwich in the exposure frame. Ensure that the force holding down the stack is not so high that it deforms the Plexiglas, leaving a void in the center. Doing so will ruin the exposure by not forcing the artwork flat against the surface of the circuit board material
3. Place the frame under the exposure lamp and expose for 10 minutes.
4. Remove the exposed board and immerse into a solution of 7 parts water to 1 part developer. This is the most crucial stage of the process, as it is subject to significant variation in time required for development. Too little developing time and the board will not fully develop, resulting in extra copper where it is not wanted. Too much time and the exposed areas will also dissolve and a blank board will be left. It is best to make several test samples and repeat the process, each time using a fresh developer solution. With a sponge brush (available at any hardware store) gently agitate the developer on the surface. After approximately 1 or 2 minutes the image should be very clear. Under

dim light, look to see the reflection of the copper and the difference between that and the reflection from the resist. When the image is clear, remove from the developer. Determining when the development is complete requires constant calibration, as it is highly dependent on humidity and ambient temperature.

5. Rinse the solution in clean water for a moment to remove any remaining developer.
6. Submerge in ferric chloride. If possible, heat the ferric chloride to 120 degrees F, as this will speed the etching process considerably. At room temperature, etching a board can take 20 minutes or more. The time to complete the etching depends on the thickness of the copper and the complexity of the circuit. Additionally agitating the solution will result in faster etching.
7. After the circuit is fully etched (be sure not to over etch), remove the board and rinse in clean water. Use a solvent (isopropyl alcohol, methyl ethyl ketone, acetone, etc.) to remove the resist. Isopropyl alcohol works, is much less toxic than the rest, but takes longer.

The board is now finished and ready to be drilled and shaped. An optional step is to use tinning solution on the board. This helps prevent oxidation of copper and eases soldering by coating the metal surfaces with tin.

ii. Mechanical Test Fixtures

High power/efficiency RF amplifiers require careful construction to ensure minimal loss, effective thermal heat sinking, and mechanical stability. At microwave frequencies, good grounding and connector mating are essential. Mechanical structures made principally from metals such as aluminum, brass, and copper are used as mounting surfaces and heat sinks. Additionally, for very high gain amplifiers, these may be used to prevent oscillation, by isolating stages of amplification.

For the amplifiers presented, two different test fixtures were built. The first amplifier fixture (figures IV-2,3) was a three-part design, wherein the hybrid combiners are mounted on aluminum plates. Between these two plates is a copper plate, which holds the amplifier boards. This test fixture provides great flexibility and reasonable performance. The interface between the aluminum and copper board carriers presents a discontinuity of ground plane, as the junction will have mechanical contact over a region smaller than the plate edges due to limited machining tolerances. To overcome this limited contact region, silver epoxy is coated on the edges where the joint is made.

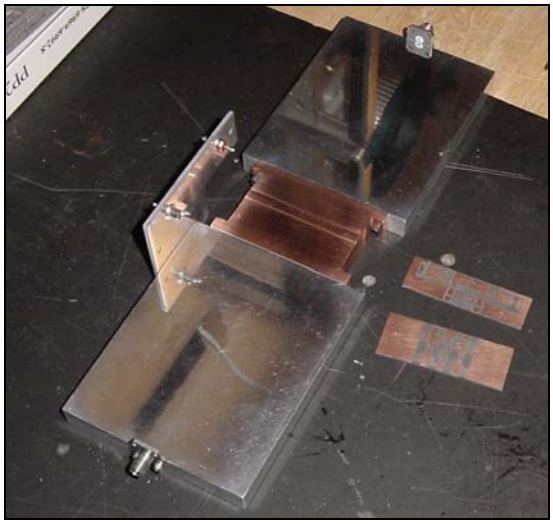


Figure IV-2: Test Fixture for Amplifier 1

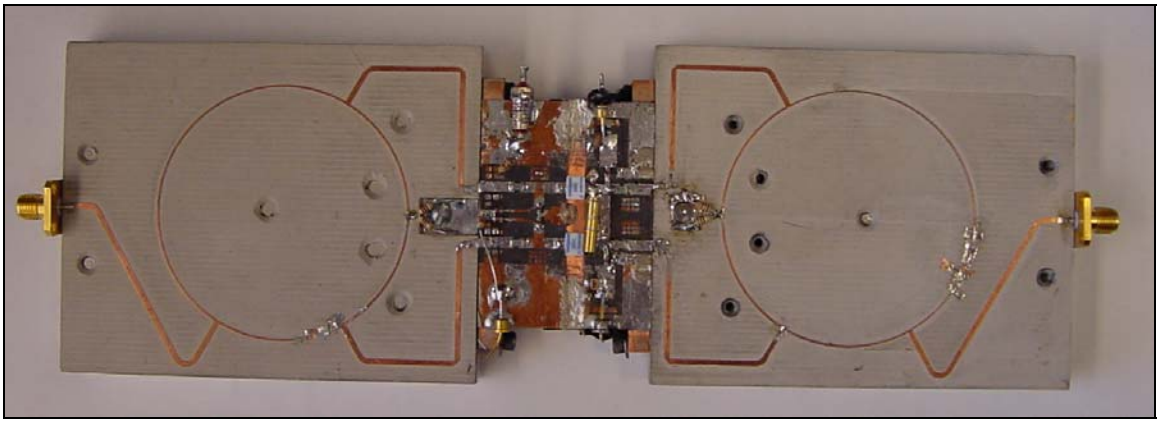


Figure IV-3: Completed Amplifier 1

The materials were selected according to on the heat sinking needs of each component, and difficulty of manufacture. Aluminum is the default material of choice due to its excellent machining characteristics, mechanical strength, and good thermal conductivity. Copper was chosen for the center portion for its superb thermal and electrical conductivity (surpassed only by silver and diamond). Each circuit board was mounted to its metal carrier with the use of silver loaded epoxy. Silver loaded epoxy (SPI Fast Setting Epoxy made by ChemWorks) provides high thermal

and electrical conductivity and the mechanical strength to hold the board to the carrier. Mechanical fasteners can be used, and are preferable for their ease in construction and modification. However, unless a large number of fasteners are used, small voids can be left between the ground plane of the circuit board and the carrier. These voids can become resonant cavities at high frequencies, but more likely they will introduce ground loops, resulting in an effective inductance.

In order to ensure good mating between the connectors and the circuit boards, the metal carriers were machined using a highly accurate milling machine to provide perpendicular and flat mounting surfaces. A pair of holes were drilled and threaded into the edge of the aluminum plates for the mounting of the 4-hole square flanged SMA connectors.

In the second generation of amplifier construction, a single plate of aluminum was chosen over the multi-plate construction method. Since the newer amplifiers were not expected to dissipate as much power as in the first amplifier, the copper was not necessary. Figure IV-4 below shows the mechanical drawing for the test fixture. Two identical fixtures were made to facilitate the construction of the dual amplifier setup.

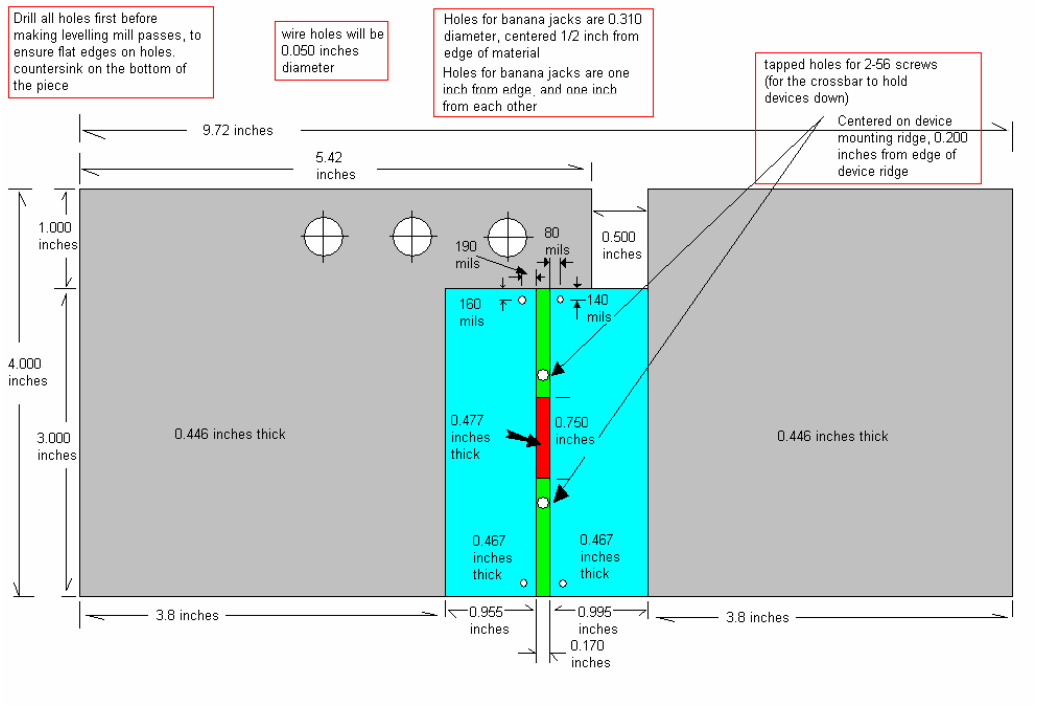


Figure IV-4: Test fixture mechanical drawing

iii. Test Equipment Setup

In order to test the amplifiers, several pieces of test equipment were used to measure various parameters such as output power, drain voltage waveform, supply voltage, and current. The high level of RF energy generated by the amplifiers exceeds the maximum limits of the inputs to the test equipment and requires sampling. Additionally, any coaxial interconnects (cables, adapters, etc.) on the output result in net losses that can be significant in the accurate measurement of output power capability. A directional coupler is used as close to the output

connector as possible. This is achieved by using a barrel adaptor on the output connector, directly connecting the coupler. Details of the functionality of the coupler are included in Section V on measurement methodologies. A great deal of care must be taken in the assembly of test equipment and interconnects to ensure repeatable, accurate measurements. The performance of coaxial connectors can be maintained by ensuring that care is taken to avoid mechanical stresses at interfaces. With the directional coupler used in this measurement, a block of metal was used to elevate the coupler such that the pull of the connected devices would not put a mechanical load on the output connector.

c. Tuning the Circuits

i. Tuning and Adjustments Required for Operation

Practical RF circuit performance is susceptible to differences in the designed and constructed circuits. Simulations are an approximation, and for this amplifier even more so, as the non-linear nature of the system makes for difficult accurate simulation using modern tools. Tuning of the circuits was required to achieve the performance indicated in the measurements section. Additionally, since the transmission lines connecting the output to the hybrid were not integer multiples of a half wavelength, the impedance presented to the output was not as expected.

As expected, when the amplifiers were first powered up, performance was not what was predicted by ADS. Initially the tuning of the amplifiers was incorrect. In the case of the first amplifier, the initial resonant frequency of the tank was roughly 750 MHz. An off-frequency tank circuit was not unexpected however, as the models used for the design of the tank were approximate, and due to the high Q of the tank, small differences can shift the resonant frequency significantly. An adjustable (0.5 to 6 pF) capacitor was soldered across the tank, which allowed for adequate tuning capability. After tuning the tank circuit, the combiners were tuned for peak performance. Key to the efficiency of this amplifier is the proper treatment of generated harmonics. The output combiner thus provides the most impact on the efficiency of the amplifier, as the input signal is sinusoidal, with little harmonic power content. Since the electrical length of the transmission line connecting the output tank to the combiner is not an integer multiple of half wavelengths, the harmonic terminations (shorts or opens) do not appear where they should. At initial powering of the amplifiers, this resulted in low efficiency. Solving this directly means lengthening or shortening the transmission line lengths, which is difficult. Another option is to aggressively tune the combiner using small flecks of tinned copper sheet. Soldering these to the combiners in the correct place results in a dramatic improvement in efficiency (more than 10% observed in each amplifier).

For simplicity and initial testing the first amplifier was constructed with a minimal input matching network design based on the transistor model. To improve the performance of the amplifier, a sliding tuner was inserted at the input to the input

hybrid. Adjustment of the sliding tuner was made to maximize power output and efficiency. Using the sliding tuner resulted in a doubling of the output power and a correspondingly dramatic increase in efficiency.

For the second amplifier, a matching network was designed empirically. A measurement of the input impedance of the switch transistor while the device is in its linear/ohmic region is needed to design the input matching network. This can be measured on the network analyzer by simply shorting the drain to the source, approximately the same condition as when the device is in conduction. Since the drain source capacitance is absorbed into the tank circuit, it is desirable to eliminate it during a measurement of the input match. The transistor was configured as a one-port network with the gate being the input and ground being the source-drain connection. To test this arrangement, the transistor was soldered onto a female bulkhead SMA connector as shown:

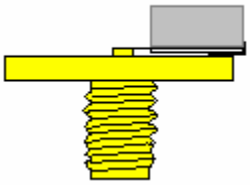


Figure IV-5: Input matching test fixture

Since the calibration of the network analyzer is not correct to the plane of the transistor, adjustments had to be made. By using an identical open female bulkhead flange connector, the reference plane was shifted. A short, an open and a 50 ohm load were used to check the accuracy of the adjusted calibration. All three of these

calibration loads showed good accuracy in phase delay and impedance. A bias-tee circuit allowed the transistor's gate to be biased at cutoff, around 3 volts. This then allowed an accurate measurement of the transistor's input impedance as shown in table IV-1 below.

1 GHz input capacitance reflection		
Gate Bias Voltage	Real	Imaginary
0	0.8097	-13.05
2.6	2.27	-11.67
2.8	2.835	-11.45
3	3.432	-11.33
3.2	4.157	-11.37
3.4	4.982	-11.79
3.6	5.264	-12.41

Table IV-1: Input impedance measurement

A matching network was conceived using a series inductor and a shunt capacitance. The series inductance in form of a narrowed section of the 50-ohm microstrip was used to feed each transistor because a series inductance of less than 1 nH is required. A small surface mount porcelain chip capacitor was soldered to the line and grounded through a via in the circuit board and filled with conductive silver epoxy as in figure IV-6.

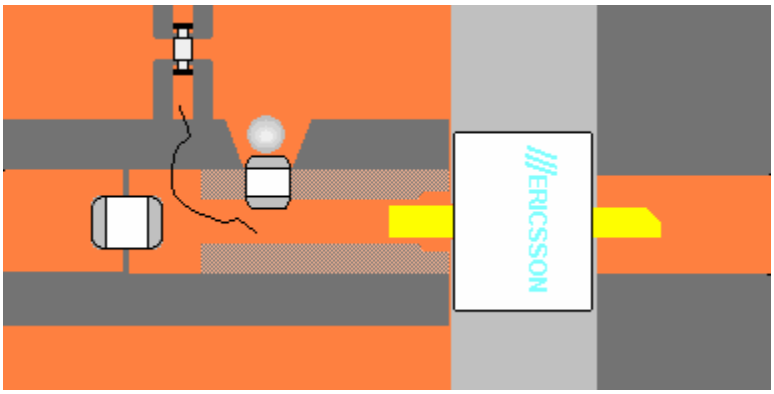


Figure IV-6: Input Matching network

ii. Results of Tuning

Initially the matching network provided a significant boost in the gain, which increased power added efficiency as well. Tuning was performed by an iterative process of sliding the capacitor, soldering it down and then trimming the line width.

With very little tuning, the match provided an increase of 3 to 4 dB of gain. After tuning, the circuit consists of a 200 mil long trace 60 mils wide and a 39 pF capacitor. Since the ground vias for the capacitors are not ideal, some inductance must be added in series with the capacitor.

Switch mode amplifiers such as the CMCD amplifiers presented here, are perhaps easier to tune than their linear counterparts due to a smaller dependency on the input and output matches for high efficiency. However this amplifier has unique tuning requirements for optimum performance, including accurate frequency response of the tank circuit, good phase (180 degrees offset) and amplitude balance between

the two transistors. Undoubtedly, much more could be learned about tuning CMCD amplifiers by experimenting with non-CW waveforms. The DC current feed would likely be a source of problems, requiring additional effort.

V. Measurements Section

Traditionally, microwave amplifiers are characterized using tools such as network analyzers. A network analyzer can easily measure the gain, linearity, bandwidth, input and output impedances, etc. For high power amplifiers (those which produce more than a watt or so, depending on the analyzer) a typical network analyzer is virtually guaranteed to sustain damage. Additionally, for an inherently non-linear amplifier, a network analyzer is insufficient to fully characterize the performance.

Measuring the performance of a CMCD power amplifier is unique with respect to traditional linear power amplifiers and even other switch-mode topologies. The critical data needed from the measurements are gain, efficiency, total output power, bandwidth, and a close look at the output voltage waveforms.

The following sections explain and justify what was measured, how they were measured, and the methods by which the test fixture is calibrated. Later, measurement results are given for the first high power CMCD amplifier built, and then for the matched pair built for the LiNC experiment.

a. Methodology

i. Justification for Measured Parameters

Characterizing an amplifier must describe at first, the degree to which an input signal is made stronger. In many applications an amplifier, especially a power amplifier, ought to exhibit some appreciable gain. Gain however is not the only important figure of merit, especially with RF power amplifiers, especially those intended for low power systems. Improving efficiency was the primary driver for the development of switch-mode amplifiers. Total output power is especially important to this project, as the goal was to push the power-frequency product significantly further than previous efforts. Gain, Efficiency, and Output power are thus the focus of the measurements taken.

An amplifier may exhibit high gain, efficiency, and output power, but at the same time be of limited use if its usable bandwidth is too small, production of harmonics to great, or instability too great. Characterizing these parameters is necessary to show that this amplifier is useful.

The shape of the voltage waveform across and current through an active device places the amplifier into its particular classification. In order to show that this amplifier is indeed a CMCD amplifier, these waveforms must be examined. Examining the current through a device is prohibitively difficult, so this was not attempted for these amplifiers. In order to obtain a good drain current measurement, probing inside the device would be necessary, as part of the tank capacitance lies within the package. Looking at the voltage waveform alone is not completely sufficient to categorize this amplifier, however if the waveform is a half-sine wave, then it can be deduced that the overlap of the current and voltage waveforms is likely

very small. Additionally, if the waveform peaks at pi*Vdd, and has a minimum of V_{dsat}, the amplifier can be safely said to be operating as CMCD.

ii. Test Setup

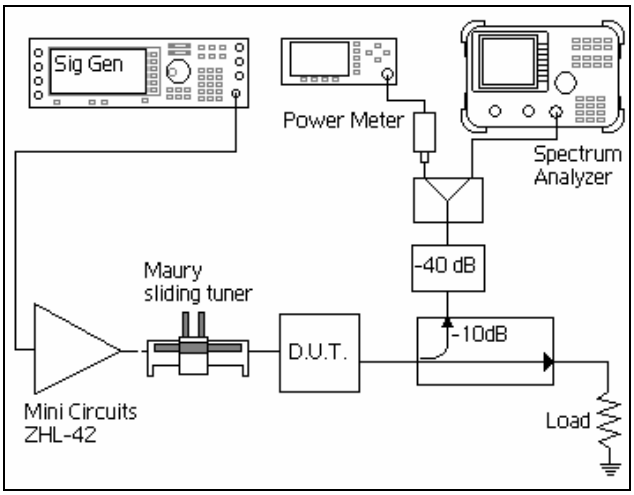


Figure V-1: Test Equipment Setup

Figure V-1 shows the test equipment setup for a single amplifier. The stimulus to the amplifier consists of a MiniCircuits ZHL-42 amplifier driven by an Agilent ESG series Signal generator. The output signal is fed through a directional coupler to a high power load termination. The directional couplers serve as a way of sampling the output to measure output power and look at the output spectrum. The directional coupler has a 10 dB coupling factor, so that at 10 watts output power, 1 watt appears at the coupled port. A large attenuator sits between the coupled port and a power divider. The power divider allows the power sensor and spectrum analyzer to monitor the output simultaneously.

iii. Calibrations

Calibrating the test setup is important, as a difference of a few tenths of a dB in gain or output power is significant. The following process is used to calibrate the test fixture.

a. Measure the loss through the coupled port of the directional coupler, attenuator and power divider.
b. Set the offset of the power meter to the value measured in a.
c. Connect power meter head to coupled port of the directional coupler through the attenuator and splitter. Terminate the unused port with 50 ohms.
d. Measure the output power of the signal source (signal generator) at the end of the cable feeding the driver amplifier.
e. Measure the output power from the driver amplifier at the end of the cable connecting to the CMCD amplifier.
f. Repeat steps d and e and record a table indicating the output power setting on the signal source and the power at the driver output. At close to +32 dBm of output power, the driver amp begins to saturate.

The above steps complete the calibration of the test fixture. Available input power and the loss of the coupler are known. If it is desired to test the amplifier over

a range of frequencies, these calibrations will have to be repeated for the frequencies of interest.

Special care should be taken during calibrations to ensure that connectors are properly mated. The use of a calibrated torque wrench ensures that the connections are repeatable and accurate. High quality cables and connector adapters should be used to minimize frequency dependent changes in loss and reflection.

b. First Amplifier Measurements

After completing the required tuning and adjustments of the first amplifier, detailed measurements were taken with the calibrated setup described above. This first amplifier exhibited the highest efficiency of the three, and the highest output power at high efficiency[2].

[2] The matched pair amplifiers delivered more power at high Vds, but at a significant drop in drain efficiency

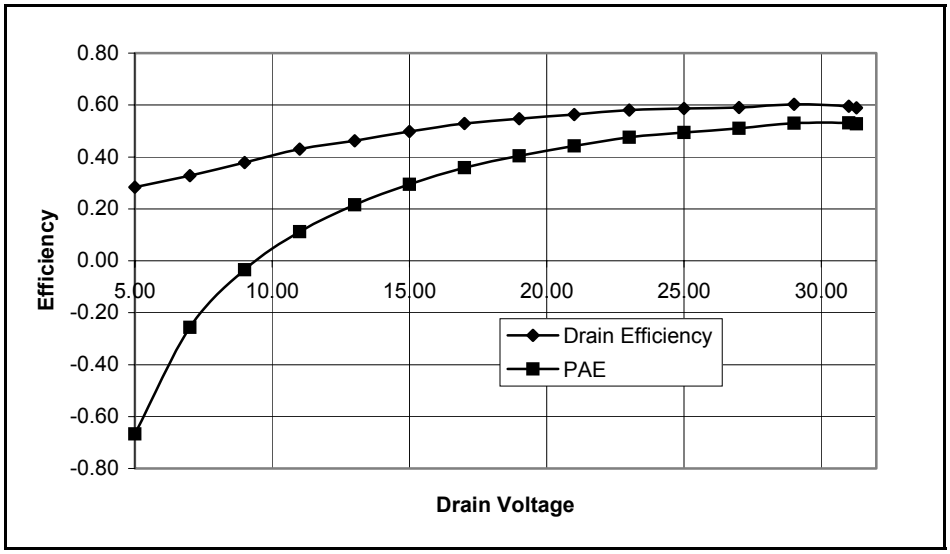


Figure V-2: Drain efficiency versus drain voltage (V_{gate}=3.63V)

Figure V-2 shows the relationship between Drain Efficiency and Drain Voltage. As the supply voltage increases, the total output power increases, thereby increasing power added efficiency substantially. Above 25 volts drain voltage, both efficiencies begin to saturate, and by extrapolation we see that beyond this point little is to be gained by increasing drain supply voltage. It is possible that the device is operating very close to, or in, breakdown in this region. Beyond this point damage to the active devices may occur, as the theoretical peak voltage would exceed the reverse breakdown voltage of the device.

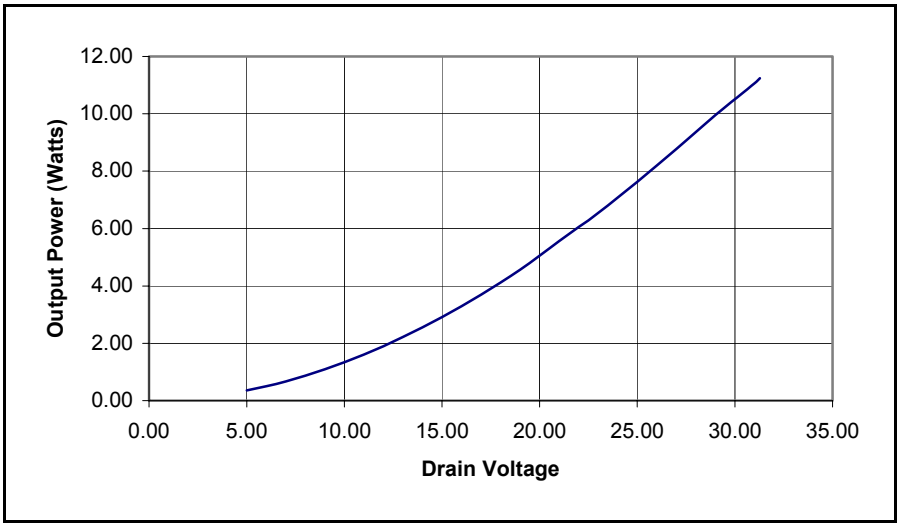


Figure V-3: Output power versus drain voltage (V_{gate}=3.63V)

Figure V-3 shows the increase in output power with an increase in drain supply voltage. This plot shows that for the region where the amplifier produces gain (above 1 watt output power) the increase in power is roughly linearly proportional to drain voltage.

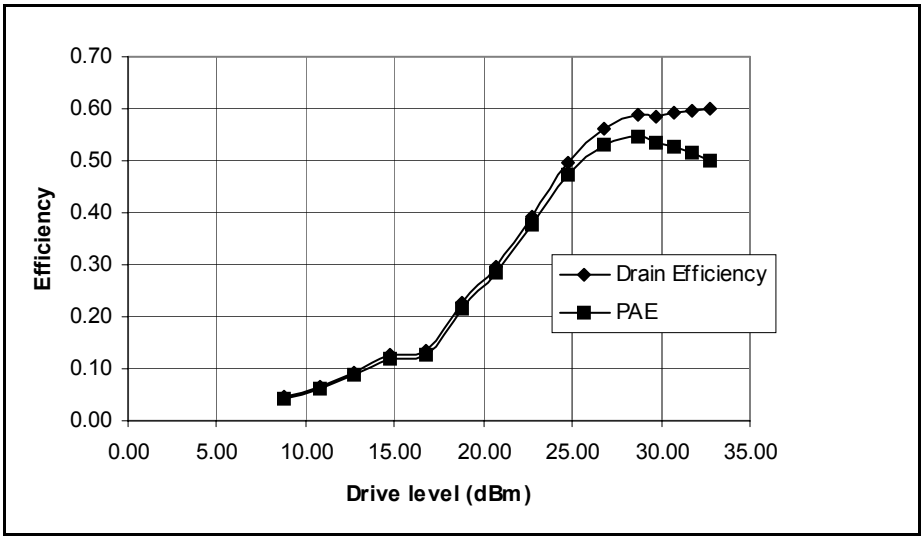


Figure V-4: Efficiency versus drive level (VDD=31.28V, VCC=3.63V)

Efficiency is plotted against drive level in Figure V-4. The purpose of this plot is to help discriminate the regions of operation of this amplifier based on drive level. For values of input power less than arpproximately 25 dBm, we can say that the amplifier exhibits a linear growth in efficiency with increased drive. Above 25 dBm input power however, we see that increases in input power result in rapidly diminishing increases in efficiency. If the efficiency is not affected by increases in the input power, the amplifier is operating in saturation. Since the power added efficiency begins to drop, we see that less and less power is being added to the total output power by the amplifier itself. The results of this measurement are in general agreement with those found by Kobayashi, et. al. [6].

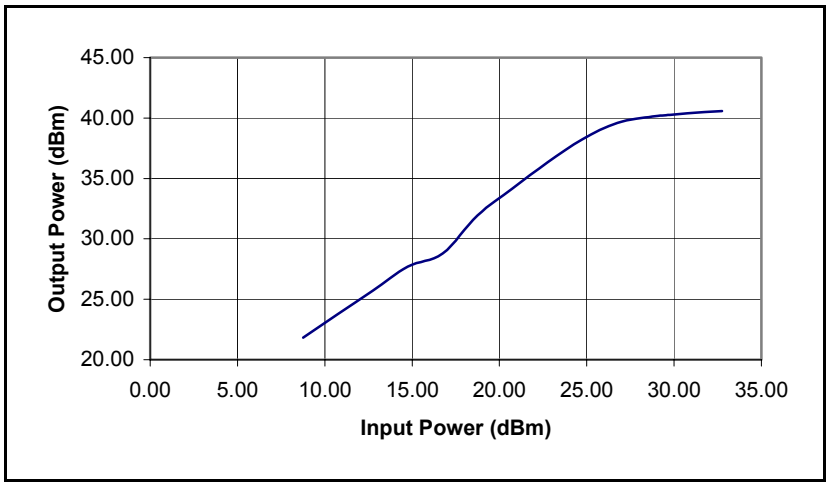


Figure V-5: Power Output Transfer Function (VDD=31.28V, VGG=3.63V)

A follow-on to figure V-4 is a plot of output power versus input power for the amplifier (figure V-5). Above 25 dBm input power, we see the same gain

compression as before. This is further evidence that the circuit is operating in the saturation region above roughly 25 dBm input drive.

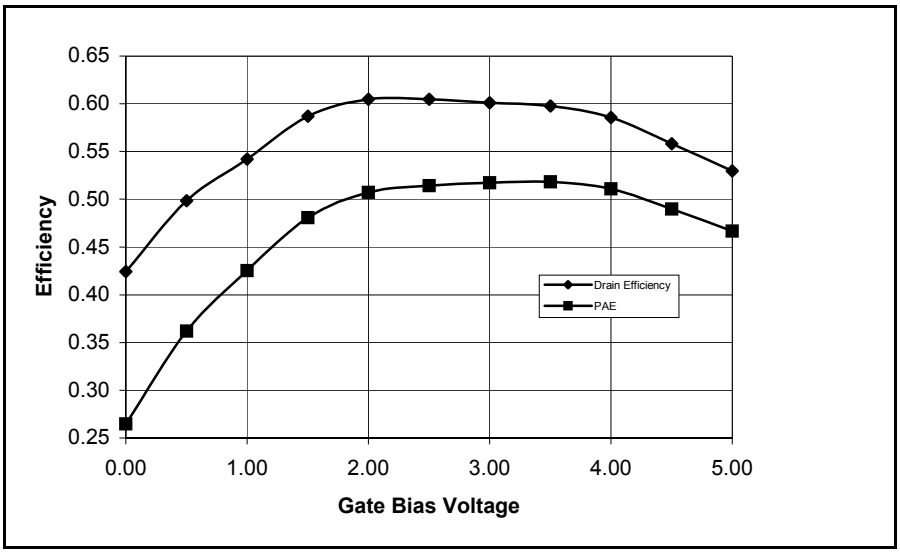


Figure V-6: Efficiency Vs. Gate Bias Voltage (VDD=31.28V, Pin=31.75 dBm)

Sweeping the gate bias changes the bias point at which the transistor operates, changing the level at which the transistor transitions from a linear to saturated mode of operation (Figure V-6). For low bias levels, the transistor turns on too late and does not conduct for 180 degrees of the period. Too high a switching threshold and the transistor wastes energy by conducting when no signal is present. An overlap in the voltage and current waveforms results, causing a dissipation of power in the transistor.

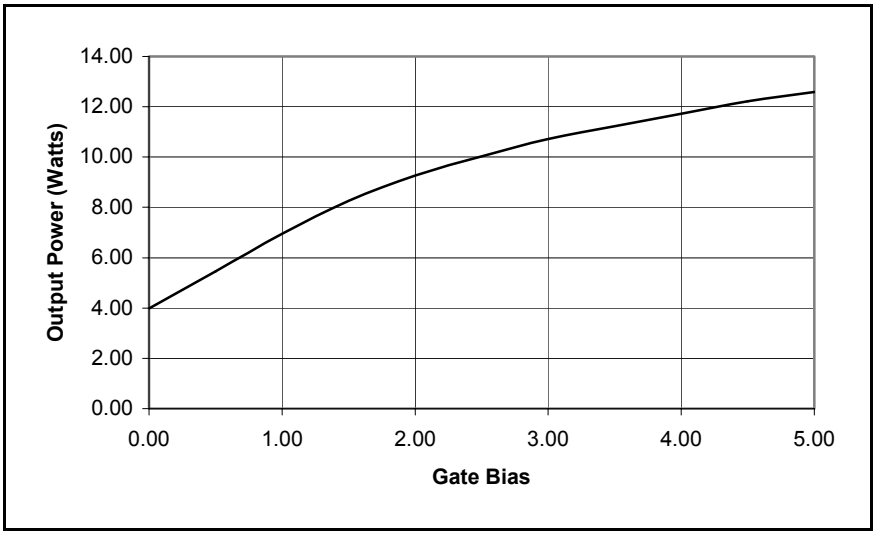


Figure V-7: Output Power Vs. Gate Bias (VDD=31.28V, Pin=31.75 dBm)

Output power saturates with high gate bias as seen in figure V-7. As the transistor conduction time per cycle maximizes, the total output power of the device reaches its maximum. However as in Figure V-6, the power added efficiency drops as the gain saturates. This is one reason why the amplifier is not operated at its maximum output power.

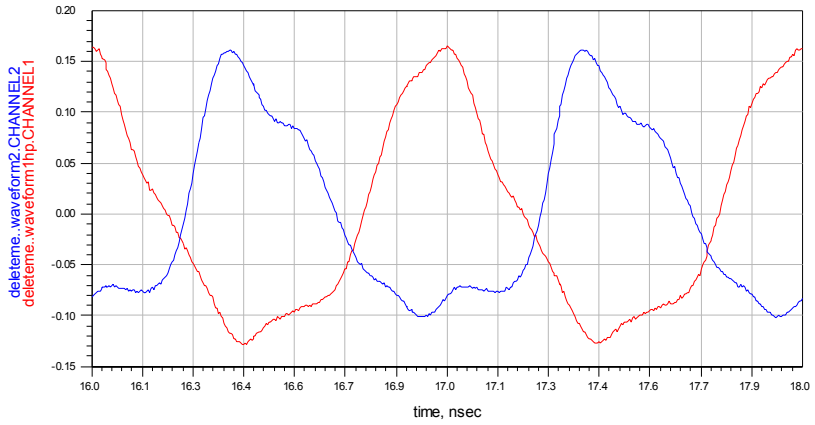


Figure V-8: Measured Drain Voltage Waveforms

Figure V-8 shows the drain voltage waveforms of the two transistor drains for the first amplifier. Some small amount of ringing is present, likely due to stray inductances.

c. Second and Third Amplifier Results

i. Results

The second and third amplifiers were tested with the same test fixture as described in the previous section. Presented below are the results of the two amplifiers intended for use in a LiNC system. These amplifiers were set up for more robust operation and tolerance to large load reactance. As such, the tuning and voltages were calibrated for maximum efficiency at 5 watts (+37 dBm) of output power. Keeping the output power at this level reduces the likelihood that a large

reflection from the load will damage the active devices. Comparing the following plots to those of the first amplifier will show that a similar efficiency and power added efficiency are attained, but at a lower output power, consistent with the application of these amplifiers.

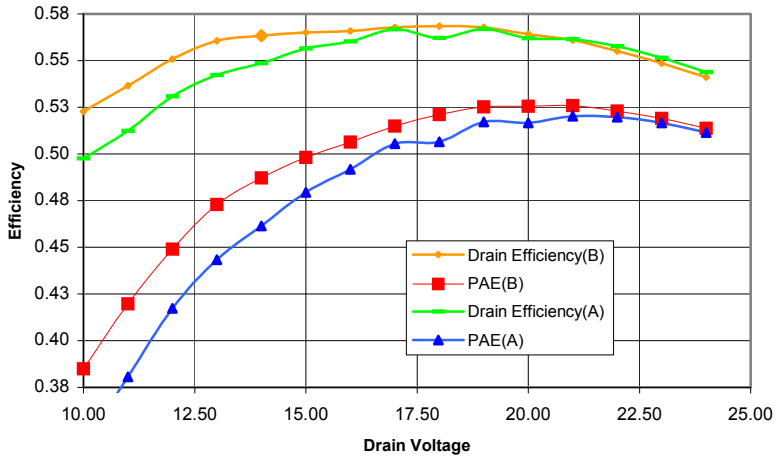


Figure V-9: Efficiency Versus Drain voltage (VDD=17V, Vgg=4.0V)

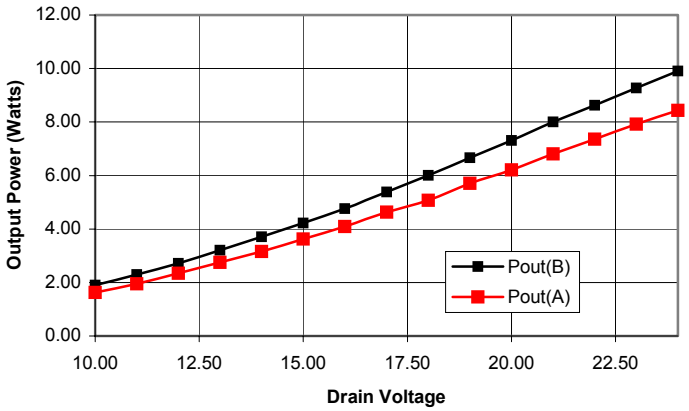


Figure V-10: Output Power Versus DC Drain Voltage (Vgg=4.0V, Pin=+27dBm)

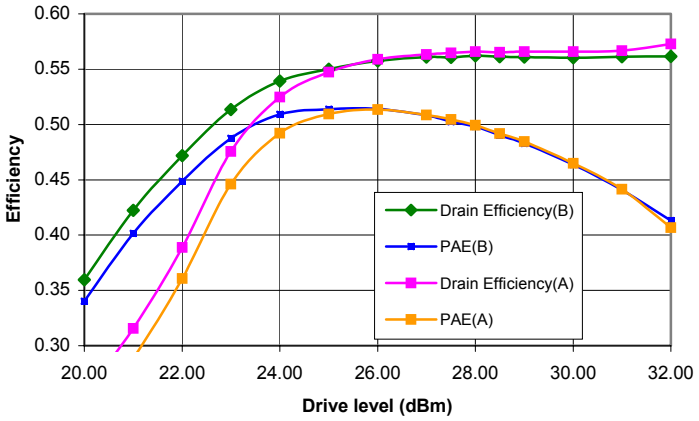


Figure V-11: Efficiency Versus Drive Level (Vgg=4.0V, Pin=+27dBm)

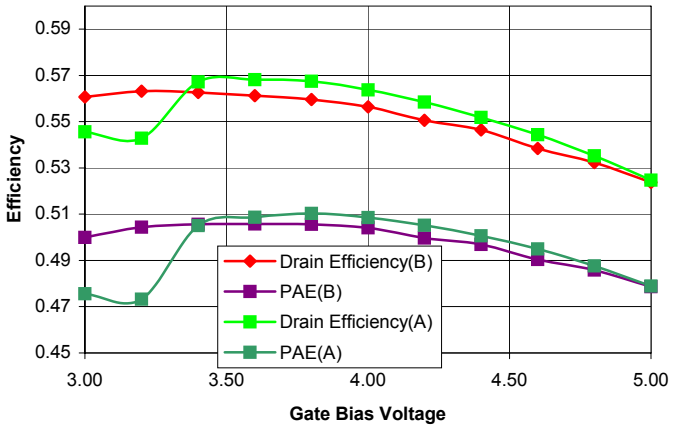


Figure V-12: Efficiency Versus Gate Bias Voltage (VDD=17.0V, Pin=+27dBm)

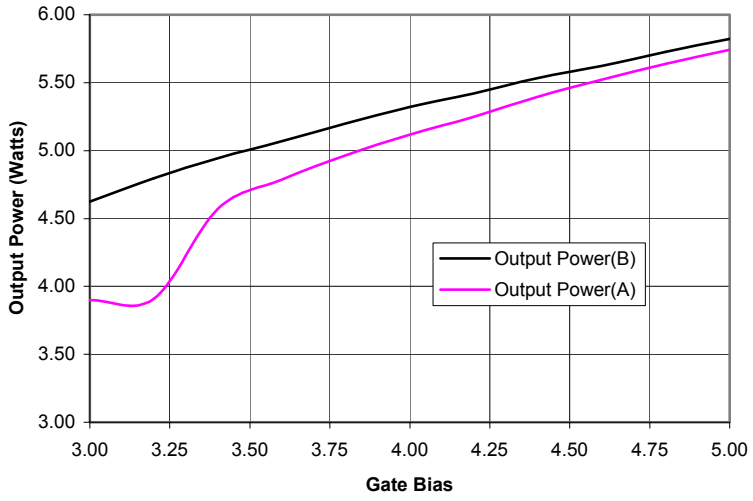


Figure V-13: Output Power Versus Gate Bias Voltage (VDD=17.0V, Pin=+27dBm)

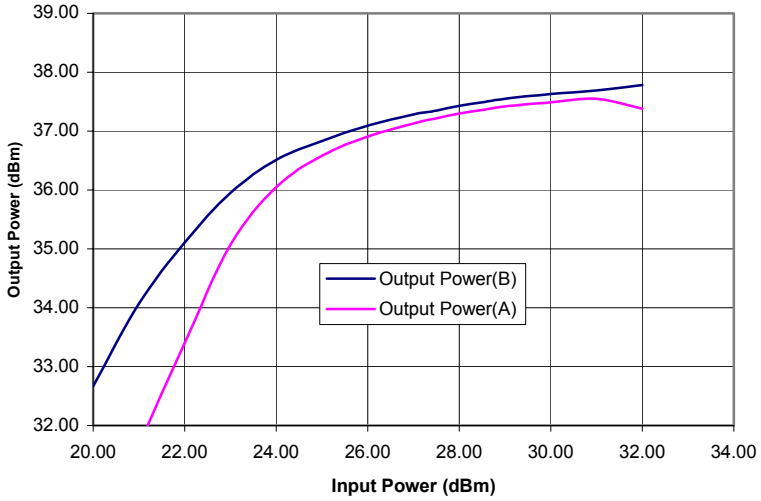


Figure V-14Output Power Versus Input Power (Gain) (VDD=17V, Vgg=4.0V)

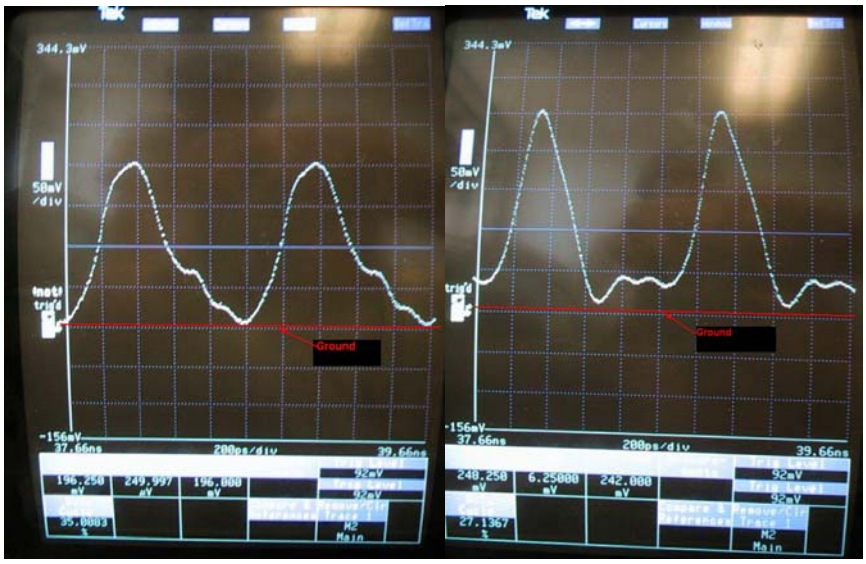


Figure V-15: Drain Voltage Waveforms From Amplifier A (VDD=17V, Vgg=4.0V)

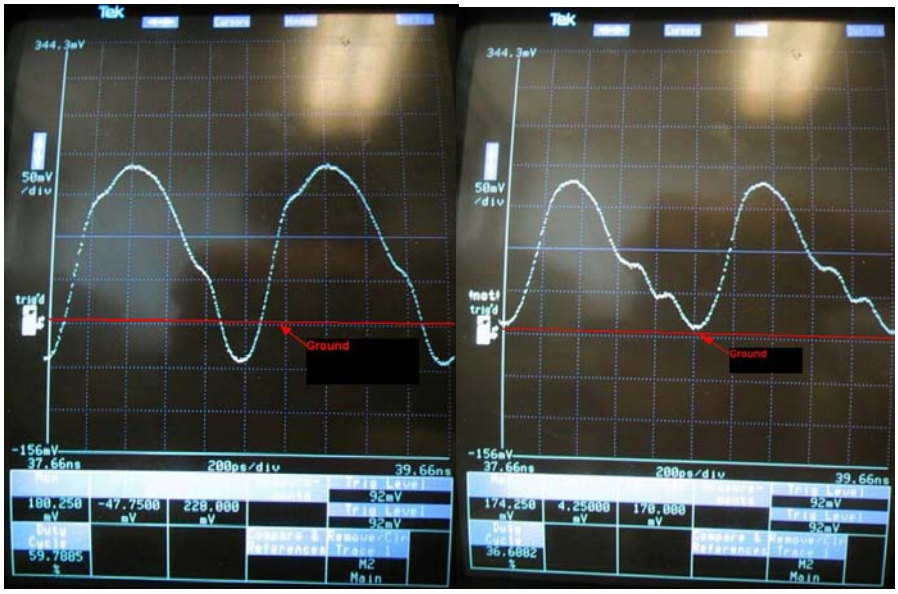


Figure V-16: : Drain Voltage Waveforms From Amplifier B (VDD=17V, Vgg=4.0V)

ii. Notes/Analysis

Amplifiers 2 and 3 operate with less output power and less efficiency at the cost of being as similar as possible. They still achieve a respectable result and will be useful for their intended purpose as testing elements for the LINC system. The trends of the second and third amplifier show that its operation is similar to that of the first. In V-15, and V-16, we have plots of the drain voltages of each transistor in each of the two amplifiers, A and B. The darker horizontal line below the curves indicates the ground potential or zero volts. Additionally, the drain voltage waveforms of the 2^{nd} and 3^{rd} amplifiers indicate that the zero switching voltage condition is being achieved. For one of the drain voltages on the B amplifier however, the drain voltage dips below zero for a brief time. This results in a loss of power and indicates the amplifier is not as well tuned as it could be.

The drain voltage waveforms of the 2^{nd} and 3^{rd} amplifiers range from fairly sharp peaks in figure V-15, to rounded peaks in figure V-16. The differences between these two amplifiers is small and is limited to small differences in tuning and slight variations in components and board manufacture. While the performance is very similar, the drain voltage waveforms are not identical, meaning that the current waveforms too must be different. It follows that the terminations of the harmonics is highly sensitive to tuning. It also shows that there are several possible termination combinations that result in similar performance.

Drain voltages for the above figures were measured through a resistor as shown in figure V-17 below.

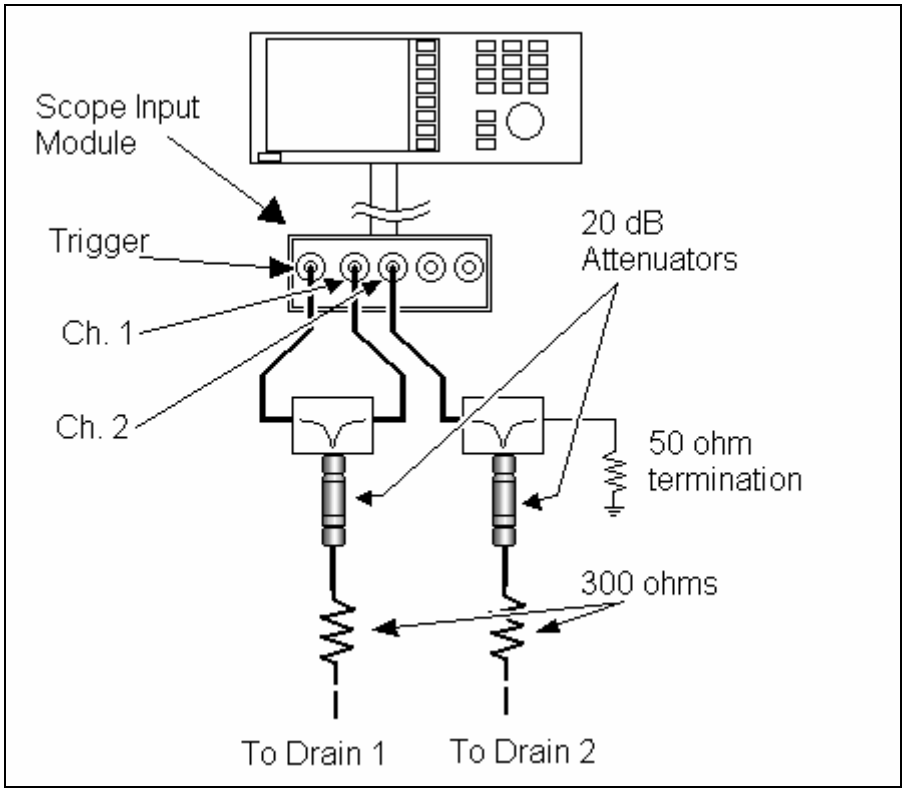


Figure V-17: Drain voltage measurement setup

VI. Analysis of Measurements

a. What Do We Actually Have? Class-D, Inverse F ?

Classification of power amplifier technology has been controversial for many decades. A plethora of classes of power amplifiers exist, and can be defined by the configuration of devices, harmonic content or treatments, conduction angle, etc. To claim that we have constructed and demonstrated a Current Mode Class-D amplifier, we need to first define what that is. A CMCD amplifier is one that meets the following criteria:

1) Creates an approximation of a square switch current waveform, and half-sinusoidal switch voltage profile.
2) Uses a pair of switches operating in parallel, out of phase across a resonant tank circuit.

The above requirements specify the resultant waveforms, so that a CMCD amplifier can be identified by its outputs, while the second specifies the method by which this waveform is created. An additional function of these requirements is to differentiate between a close relative of the CMCD, the "inverse-F" which creates the waveforms prescribed in the first requirement but with a different architecture. Since the CMCD is an isomer of the VMCD, it is appropriate to classify, in part, the amplifier based on its structure.

Do the amplifiers presented fit this definition of CMCD? The second requirement is clearly met even before the amplifier is powered on. Structurally speaking, these amplifiers consist of a pair of parallel switches being driven out of phase by a 180 degree hybrid, across a resonant tank circuit.

The first requirement however is more difficult to adhere to. It is difficult at best to measure the drain current waveforms of high frequency amplifiers. Since the drain currents weren't measured in this investigation, it is not easy to say whether the drain currents approximate a square pulse train. A real CMCD amplifier can never create a perfect square current pulse, so the definition is relaxed to include that which approximates it. The degree to which that approximation is valid requires some clarification. The question may well be framed in terms of the relevance to other amplifier classifications. For instance, a CMCD is not a Class-B, since the drain current waveforms are not nearly half-sinusoidal. At some point though, a waveform is more sinusoidal than square, or more square than sinusoidal. Practically speaking, if harmonic terminations are considered in the design and intentionally shape the waveform to become squarer, then it ought to fulfill the first requirement for CMCD.

The measurements in the previous section show a drain voltage waveform that is approximately half-sinusoidal. The results of second and third amplifiers show that the drain voltage reaches zero (or in one case dips slightly below). Reaching zero volts is critical to an important property of the CMCD the zero voltage switching condition.

Another way to classify an amplifier as CMCD is to distinguish not only what it is, but what it is not. There are at least two amplifiers that are similar enough to CMCD to warrant differentiation. Specifically, the Class-F, which is different fundamentally by design, and the recently reported $E/F_{2,odd}$. The $E/F_{2,odd}$ is remarkably similar in design and waveform to the CMCD [8]. The CMCD however does not intentionally tune the second harmonic as does the $E/F_{2,odd}$.

CMCD can be distinguished from Class-B by examining the linearity of the gain curve profile. CMCD has a non-linear gain profile when the transistors are operating in saturation. With a push-pull Class-B, the gain linearity would be extended beyond that of a comparable CMCD.

Yet another way to classify an amplifier is to compare it to other amplifiers in the same category as a check. The first published CMCD amplifier [6] is very similar in structure to our amplifiers. The main structural differences are in the input and output hybrids, the output filter, and the devices used. Comparing the measured results, we see that the drain voltage waveform (simulated as shown in figure VI-1) is similar to the measured drain voltage waveforms in Section V.

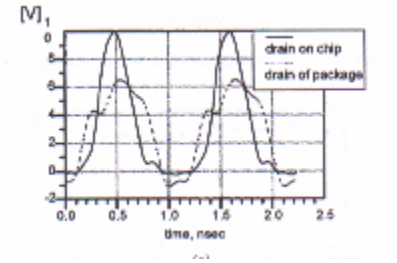


Figure VI-1: CMCD Simulated Drain Voltage Waveforms From Kobayashi, et. al. [6]

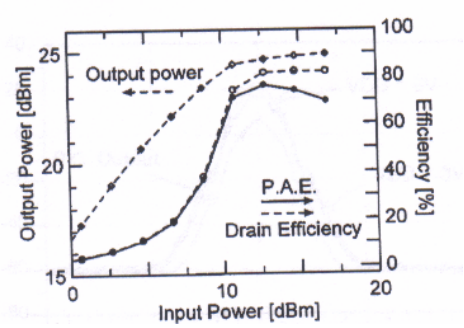


Figure VI-2: CMCD Measured Efficiency Versus Drain Voltage From Kobayashi, et. al. [6]

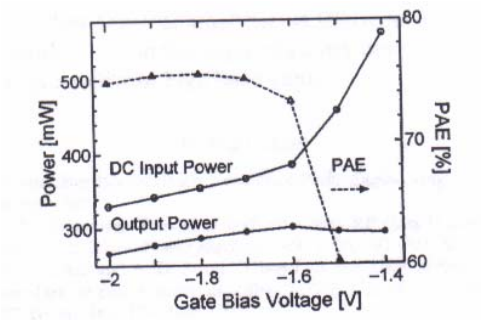


Figure VI-3: CMCD Efficiency Versus Gate Bias From Kobayashi, et. al. [6]

Additionally, the general trends of saturation of drain efficiency and efficiency versus gate bias are quite similar (figures VI-2 and VI-3). Thus the structure and behavior of the two amplifiers are similar enough to be classified together.

b. Differences between simulation and actual circuit

The simulations performed for the amplifiers presented are at best a rough approximation of the actual amplifiers. Due to extensive tuning and adjustments, the final amplifiers ended up being significantly different than their simulated counterparts. Additionally, because of the difficulty in simulating the amplifier, simplifications were made and some components were idealized. Useful results were obtained however. The results of the simulations in section III show properties similar to the measured results of the first (high power) amplifier built. For the same drain supply voltages however the power output is significantly reduced for the physical amplifier. This may be attributed to losses that were not considered in the simulation, such as micro-strip loss (there is a great deal of transmission line in the couplers), lower Q in the tank circuit due to capacitor losses, loss in the DC blocking capacitors and so forth.

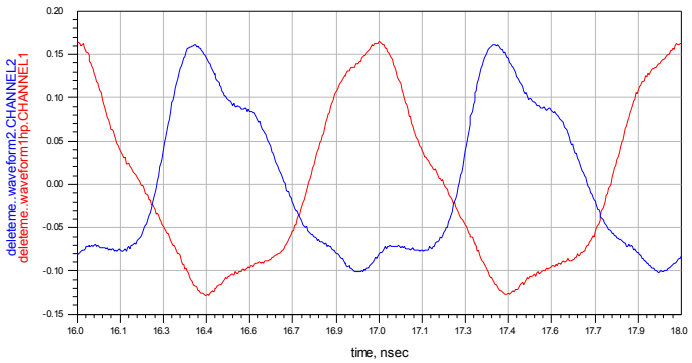


Figure VI-4: Measured Drain Voltage Waveforms

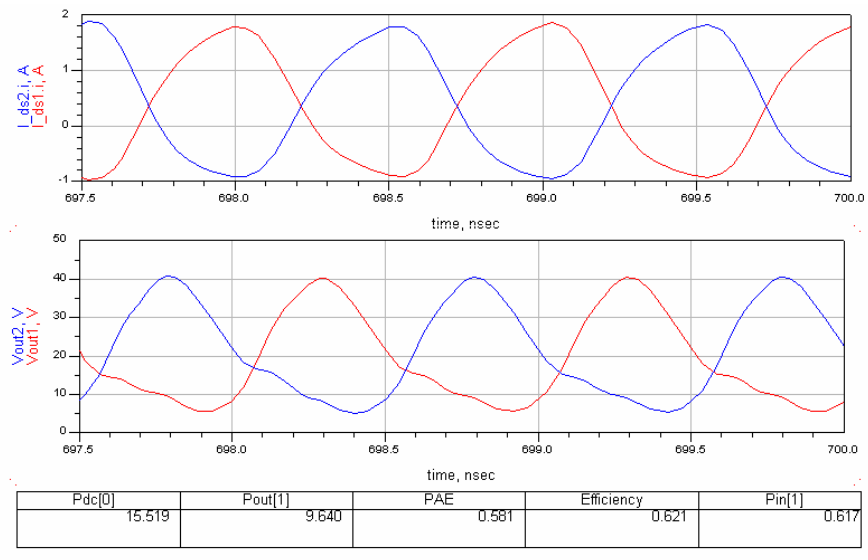


Figure VI-5: Simulated Drain Voltage and Current Waveforms

Figures VI-4 and VI-5 compare the measured and simulated drain voltage waveforms for the first amplifier built. The drain voltage waveforms in the simulation are free of the overshoot present in the measured waveforms. Due to the overshoot of the measured result, the maximum power output of the amplifier is reduced, as the peak voltage is higher. This results in a lower power utilization factor. With a lower power utilization factor, an amplifier will produce less power for a given bias supply voltage. The overshoot in the measured result is likely due to the differences in the components used in the circuit and their incomplete models used in simulation. Without including small parasitic reactances of tank and DC feed components, it is difficult to accurately predict the overshoot that will occur.

Since the drain currents were not measured, there is no sure way to predict those results. A best estimate would say that the drain current is peakier than that of the simulation, corresponding to a peaky drain voltage waveform. However, with the comparable efficiency of the two amplifiers, the drain current may be more square than the simulation, an artifact of the tuning done on the output hybrids.

With the differences in the drain waveforms, the similarities in efficiencies, the simulated amplifier and constructed amplifier appear slightly different in their particular functioning, yet similar in their results. A more detailed simulation of the circuit, including better models for passive components would certainly improve the correlation between the two. In this case it may be possible to design the amplifier to improve the overall performance and achieve higher output power and higher efficiency. Ultimately though, this amplifier is sensitive to small changes and could benefit from work on reducing these to the point where the amplifier is well behaved, and operates over a broad bandwidth. This may be achieved by investigating other types of input and output hybrids and taking closer consideration of harmonic impedance control.

VII. Conclusions

a. Summary

The results of this investigation into Current Mode Class-D amplifiers shows that it is indeed possible to obtain high efficiency amplification at high frequencies and high power using a switch-mode topology. A single amplifier achieved 13 watts of output power with 60% efficiency at 1 GHz. Two more identical amplifiers tuned for lower output power produced 5 watts with 57% efficiency, also at 1 GHz.

Producing higher power, the amplifiers presented build on the work of Kobayashi, et. al. and yielding even more evidence of the benefits of the CMCD topology. Additionally, the results presented take switch mode power amplifiers into a new realm of applications including wireless base station use. While much work is left to improve efficiency and increase power output, these results demonstrate a capability of switch-mode amplifiers not before demonstrated in published literature.

b. Future Work

With the completion of the two identical amplifiers, work will commence on researching linearization techniques, in particular, LiNC (Linearization of Non-linear Components). The goal of this investigation is to determine whether the high efficiency of switch-mode amplifiers can be exploited for applications requiring high

linearity. Ultimately this will determine the widespread success of switch-mode power amplifiers for high power high frequency applications.

There are many opportunities to expand on the results presented. For instance, a closer investigation into harmonic treatments is necessary, as well as a closer look at the effects of and sensitivities to various types of input and output hybrids. Additionally, alternative tank circuit structures merit investigation, as well as quantifying the most critical device parameters for this circuit's mode of operation.

VIII. Acknowledgements

I would like to acknowledge and thank the following for their assistance in this effort.

Dr. Stephen Long – Advisor with immeasurable patience and guidance, and assistance throughout.

David Choi – Developed the model necessary to simulate and design this amplifier

Jingshi Yao – Did early simulation work and design for the amplifier

Florian Bohn – A constant source of useful advice and insight.

Fujant Corp. – Provided funding for the project

Nokia Corp. – Provided funding for the project

UC MICRO program – Provided funding for the project

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12. Coil Craft Website http://coi1craft.com/smind.cfm

Appendix A: Data Sheets For Selected Components

Data Sheet for Ericsson PTF-10135

PTF-10135 Model From David Choi's pHd. Dissertation