Application Note AN-1088

PDP Power Devices

By
W. Tjokrodiponto

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1. Introduction

This Application Note discusses how to select optimal power devices for Alternating Current Plasma Display Panel (PDP) applications. A large number of power devices are used in a typical PDP. These devices are used for processing power from AC mains to generate various DC voltages and to sustain plasma discharge on the panel. Power circuits used for processing power from AC mains are widely known [1] and will not be covered in this paper. This Application Note will concentrate only on power circuits used to sustain plasma discharge on the panel.

2. Plasma Display Panel Basics

The structure of a plasma display glass panel is shown in Figure 1 [2].

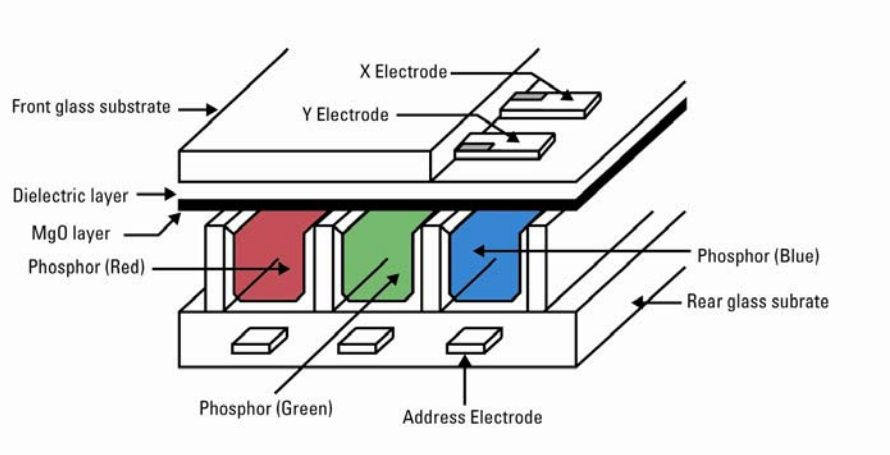

Figure 1. Cross section of an alternating current plasma display panel (PDP) of one picture element.

The X and Y electrodes located on the front glass substrate are covered with low melting glass dielectric material. This dielectric material is protected with a thin MgO layer. The address electrode is located on the rear glass substrate onto which barrier ribs are formed. These barrier ribs are alternately coated with red, green and blue phosphors. The barrier ribs are formed using various techniques such as screen-printing, sand blasting and embossing. The two glass substrates are then sandwiched together and sealed, the air is vacuumed out and a mixture of noble gases is injected between the glass substrates. Electrically, the entire assembly can now be considered as a three-electrode capacitor.

A cross point is formed where the X, Y and Address electrodes meet. Three adjacent red, blue and green cross points form a color picture element (pixel) of the panel. Each pixel can be independently controlled and can assume different color gradations. The number of pixels available determines the resolution of the glass panel vertically and horizontally. Comprehensive construction explanations of a plasma display glass panel are discussed in detail in [2].
In order to display various color combinations, each color element of the pixel is assigned a certain number of bits. For instance, if each color element has 8 bit gradations then

there will be 2^8 = 256 color gradations possible for that element. Since there are three color elements, each pixel can assume 256 x 256 x 256 = 1,677,216 color gradations. Most PDP technical specifications usually refer to such panel as having 16.7 Million RGB colors.

The most common method of displaying one picture field is using Address Data Separated method as shown in Figure 2 [3]. With this method, each field is divided into n subfields (SF). On every subfield, each cell is addressed, sustained and erased. For a typical 8 bit system, there will be 8 subfields. The subfields are weighted according to its binary values. A typical TV filed is 1/60 of a second.

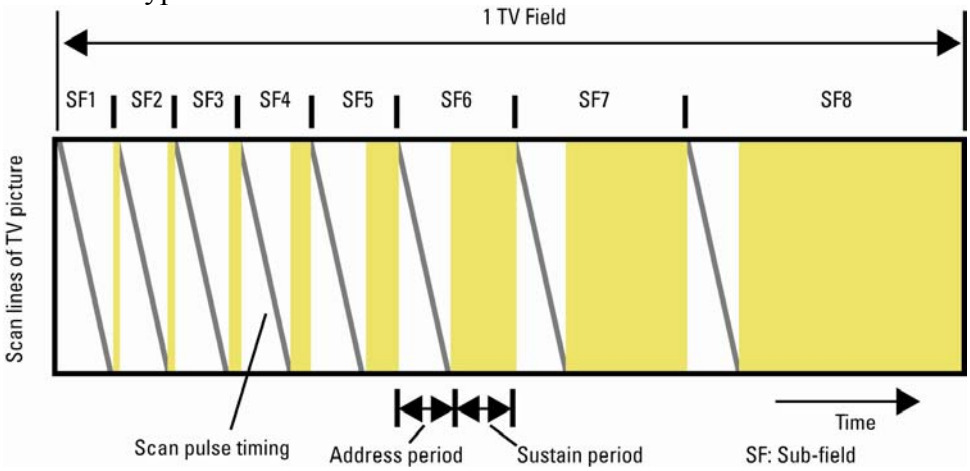

Figure 2. Address data separated of one TV field

Let's assume a color pixel that needs to have 1 red gradation, 100 blue gradations and 256 green gradations. The addressing process of that particular pixel during one TV field is presented in Figure 3.

			RED	BLUE	GREEN
1 Frame (16.67ms)	SF1	2 times discharge	✸	Off	✸
	SF2	4 times discharge	Off	Off	✸
	SF3	8 times discharge	Off	✸	✸
	SF4	16 times discharge	Off	Off	✸
	SF5	32 times discharge	Off	Off	✸
	SF6	64 times discharge	Off	✸	✸
	SF7	128 times discharge	Off	✸	✸
	SF8	256 times discharge	Off	Off	✸
		Number of Sustain Discharges	2	200	512
		Gradation level	1	100	256

Figure 3 ADS example for a color pixel requiring 1 red gradation, 100 blue gradations and 256 green gradations during one TV field.

3. PDP Sustain Circuit

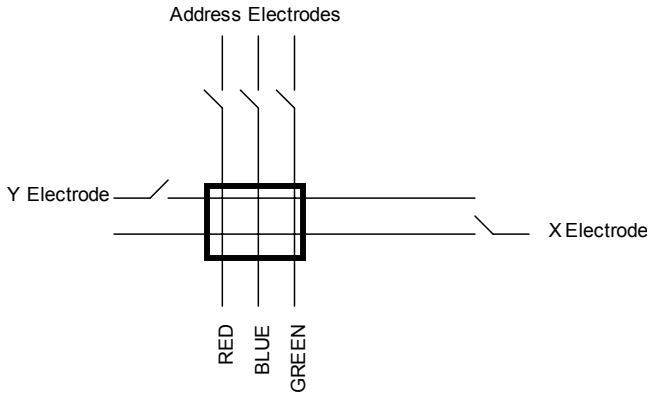

Figure 4. Schematic representation of a color picture element

Schematic representation of a PDP color picture element is shown in **Figure 4**. Each electrode is in series with a switch that connects the electrode to a voltage supply or to ground. In order to illuminate a cell, Y electrode is grounded and voltage is applied on address electrode leaving surface charge on the cell (memory effect). Typical address voltage is 85V. This process is repeated for each cell that needs to be illuminated. During addressing, none of the cells produce visible light yet.

During sustain period Y and X electrodes are alternately connected to sustain voltage and ground. This in effect produces alternating current across the panel. Sustain voltage is typically above 170V. The switches connected to the address electrodes are left opened. Cells that retain surface charge during address period will ionize the gas inside the cell. Ionized gas produces UV light that strikes the phosphor and produces visible light.

During reset period a slow ramping positive voltage up to 400V followed by slow ramping negative voltage down to -150V is applied across the X and Y electrodes to extinguish ionization and returns all cells to their off states.

The most common sustain circuit topology is shown in Figure 5 [4]. The pixels in the panel are connected in parallel and are represented as panel capacitor C3. By employing appropriate switching sequence, this circuit is capable of producing AC voltage required to illuminate, recover residual energy and reset the cells of the panel.

Power devices in Figure 5 can be grouped into the following circuit functions:

- ER circuit which consists of Q5, Q6, Q7, Q8, D1, D2, D5, D6
- Discharge circuit which consists of Q1, Q2, Q11 and Q12
- Pass circuit which consists of Q3 and Q4
- Set and Reset circuit which consists of Q9 and Q10

The operation of the sustain circuit can explained as follows. Let's assume that the cells on the panel have been addressed during the address period. The cells that need to be illuminated have accumulated enough surface charge (memory effect) to be ignited.

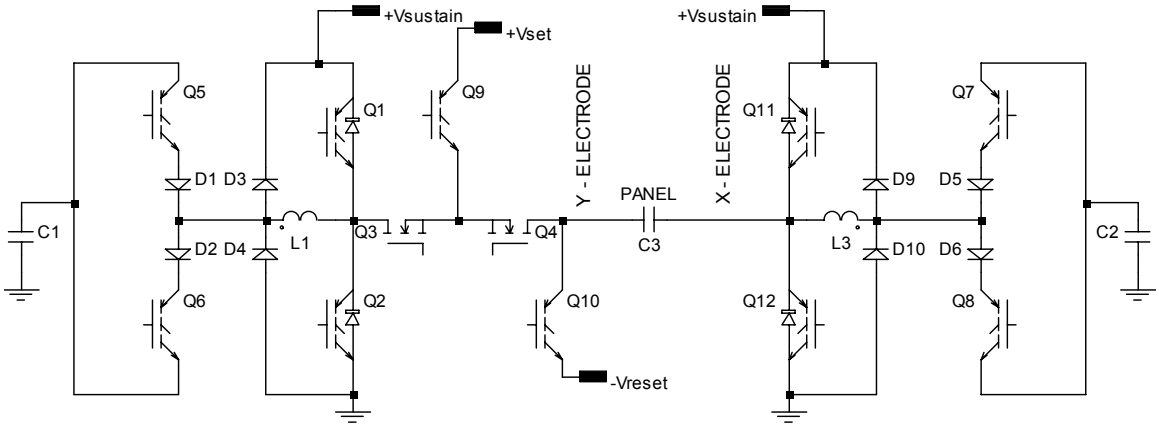

Figure 5 Typical PDP sustain circuit [4].

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Assume also that C1 has initial voltage from previous sustain cycles. To produce a positive voltage across Y – X Electrodes, Q3 and Q4 in addition to Q5 and Q12 are turned on. C1 charges and raises the voltage across the panel, C3. This step is called energy recovery since it recovers energy stored in capacitor C1 from previous sustain cycles back to the panel.

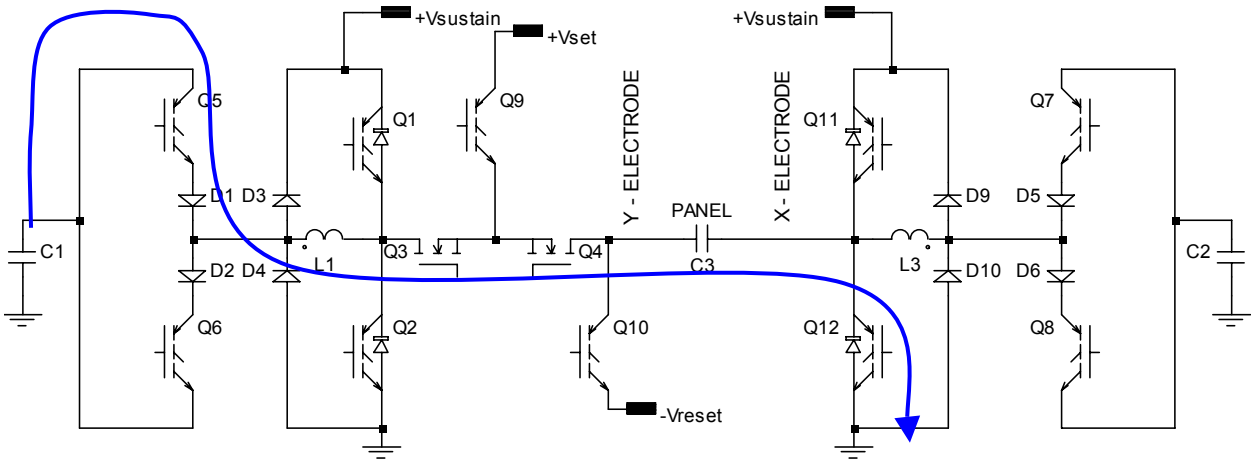


Figure 6 Positive energy recovery. Q3, Q4, Q5 and Q12 are turned on.

The equivalent circuit of the energy recovery circuit is shown in Figure 7. This is simply a series resonant inductor, capacitor, resistor (LCR) circuit. $R_{equivalent}$ is the equivalent resistance of the power devices, X-Y electrodes and copper traces of the circuit. V_C1 is the voltage across the energy recovery circuit capacitor C1. Since the value of C1 is much bigger than that of C3, C1 can be replaced with a constant voltage source V_C1. At steady state, the value of V_C1 is half of Vsustain.

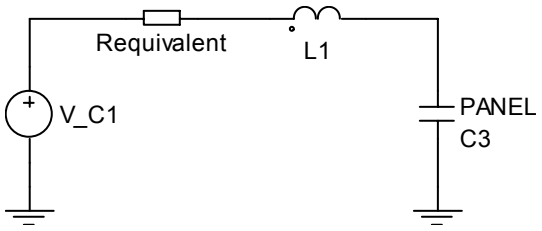


Figure 7. Energy recovery equivalent circuit.

The circuit on can be represented as a second order differential equation:

$$s^2 + \frac{R_{equivalent}}{L_1} s + \frac{1}{L_1 \cdot C_3} = V\_C_1 \quad \text{.....(1)}$$

The frequency of oscillation of the current in rad/sec can be approximated as:

$$wd \approx \frac{1}{\sqrt{L_1 C_3}} \quad \text{..... (2)}$$

And the peak current from V_C1 to panel capacitance C3 is:

$$I_{peak} = \frac{V\_C_1}{L_1 w_d} \quad \text{.....(3)}$$

The value of L3 in the energy recovery circuit is selected such that panel capacitance C3 is charged to V_C1 within half of the oscillation period (2/wd). The peak capacitor charging current is Ipeak. The typical profile of the current is half sinusoidal and is shown in Figure 8.

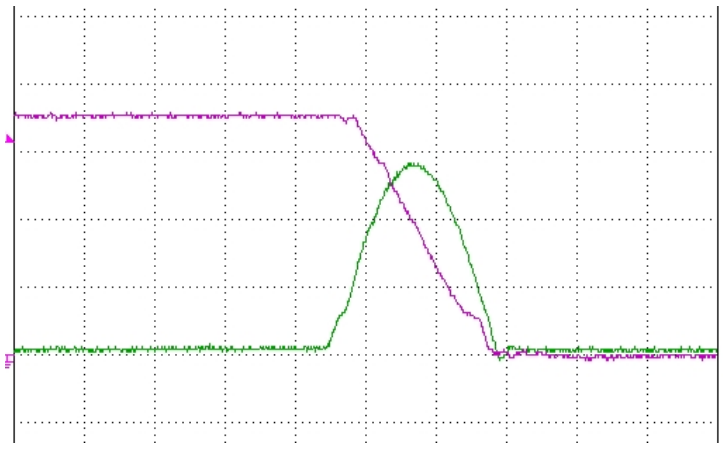


Figure 8. Typical energy recovery current charging the panel.

Immediately after panel capacitance is charged to V_C1, the discharge circuit is activated. The panel capacitance is further charged to Vsustain causing the gases on the

addressed cells to ionize, release UV light and ignite the phosphor that produces visible light. Figure 9 shows discharge current path of the panel. Ionized gases can be represented as non-linear resistor and therefore the peak current during this period is higher than that during energy recovery.

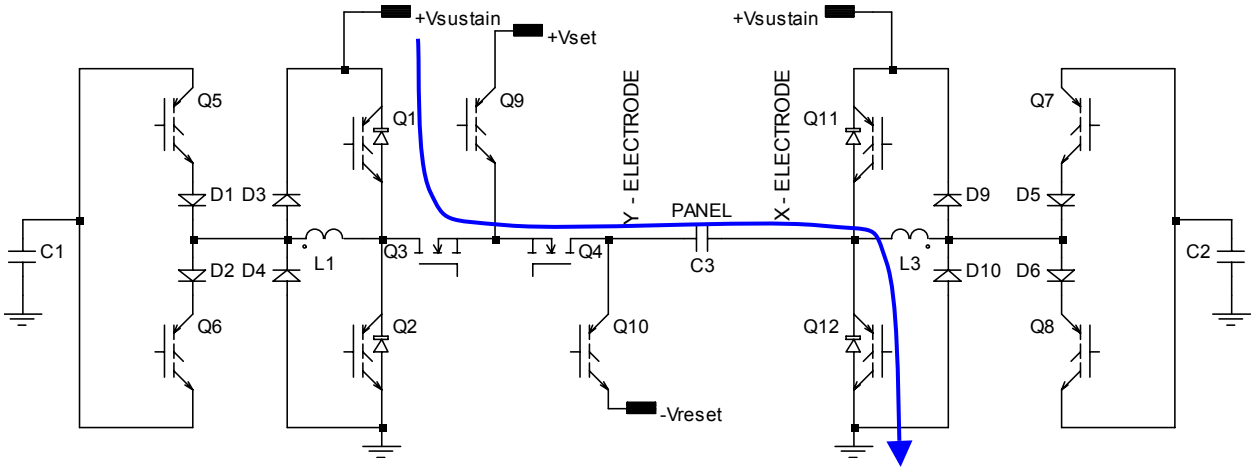


Figure 9. Positive discharge. Q1, Q3, Q4 and Q12 are turned on.

The current during discharge period also has a sinusoidal profile. Once the panel is charged to Vsustain and visible light is emitted, current will cease to flow and the gases will stop to ionize. A tank circuit is formed between the panel capacitance C3, L3 and the bus capacitance. Depending on the quality factor (Q) of the circuit, some current might flow back to the bus capacitors. Therefore it is necessary for discharge circuit power devices to have anti-parallel diodes to carry this reverse current. Typical discharge current waveform is shown in Figure 10.

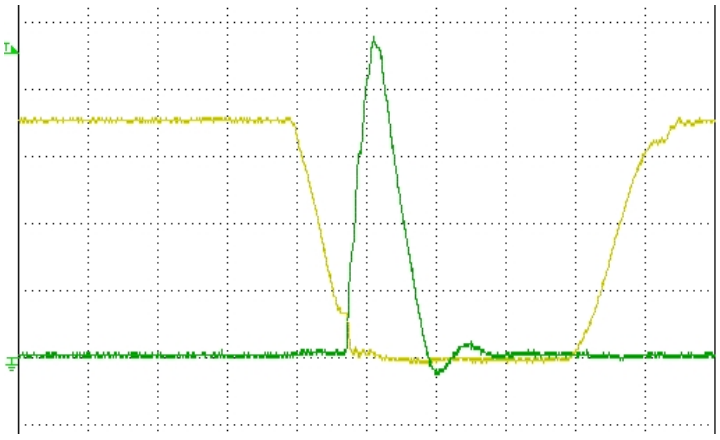


Figure 10. Discharge current profile ionizing gases on the cells.

It is now necessary to reverse the polarity of the voltage across Y – X electrodes. But prior to doing this, the voltage across the panel C3 must be brought back to zero. Dissipating the energy across C3 into a resistor could do this. However, this technique will waste a lot of energy making the panel very inefficient. A better way to do this is by moving the charge on C3 back to the energy recovery capacitor C1. This can be

accomplished by turning on Q6, Q3, Q4 and Q12. The current flow is shown in Figure 11. This current will cease to flow when the voltage across the panel capacitance and C1 are the same which is equal to half of Vsustain. The profile of this current is also half sinusoidal similar to that of Figure 8, except that the current direction is from the panel back to C1. This technique is very effective in increasing the efficiency of a plasma display panel.

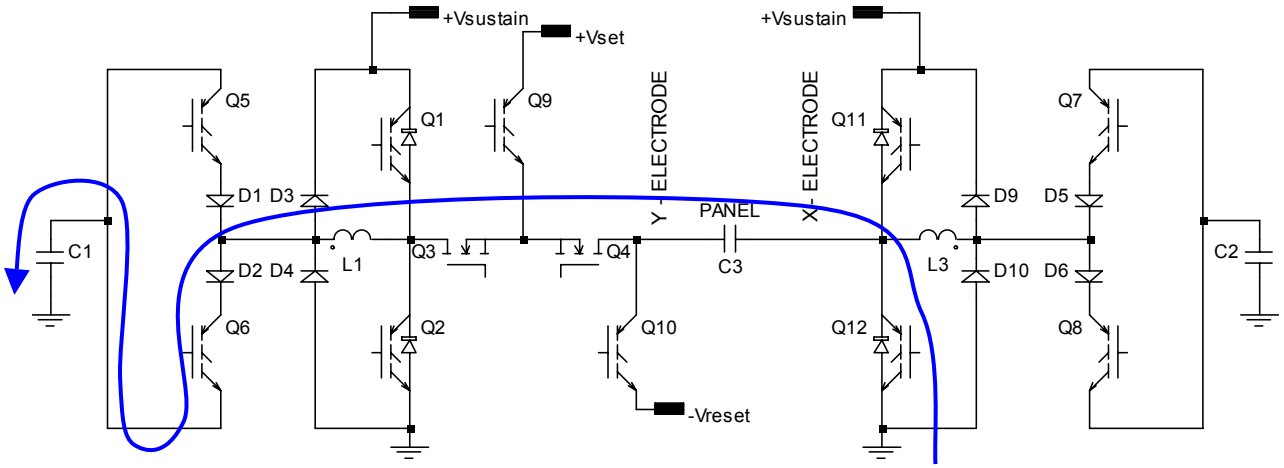


Figure 11. Recovering energy from panel capacitance C3 back to C1.

Finally to completely bring panel capacitance voltage back to zero, Q2, Q3, Q4 and Q12 are turned on. This arrangement creates a discharge path across the panel through the equivalent resistors of the power devices and the parasitic elements of the circuit. The current path is shown in Figure 12.

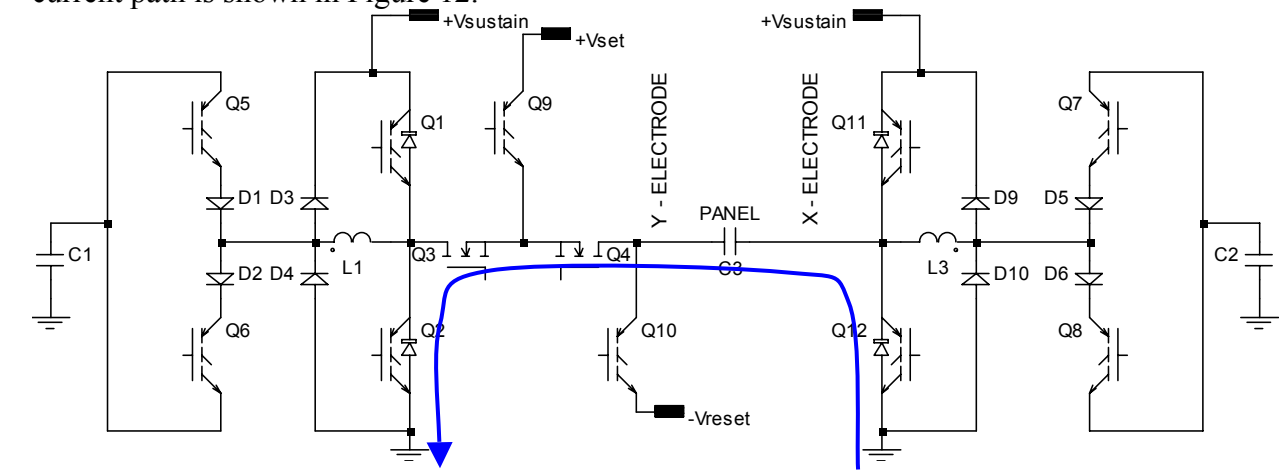


Figure 12. Bringing the voltage across the panel capacitor C3 back to zero.

One can notice that during PDP sustain process, Q3 and Q4 remain on and they will see both energy recovery current and discharge current.

In order to reverse the polarity across Y – X Electrodes. Similar switching sequence as previously discussed is repeated in order to make the X electrode more positive than the Y electrode. For simplicity this switching sequence can be summarized here:

- Energy Recovery = Q7, Q3, Q4 and Q2 are turned on. Current flows from C2 to C3.
- Discharge = Q11, Q3, Q4 and Q2 are turned on. Current flows from Vsustain to C3.
- Energy Recovery = Q8, Q3, Q4 and Q2 are turned on. Current flows from C3 to C2.
- Zero voltage = Q12, Q3, Q4 and Q2 are turned on. C3 voltage is dissipated to zero.

At the end of each subfield, applying positive ramp voltage followed by a negative one resets the cells. The current path is shown in Figure 13.

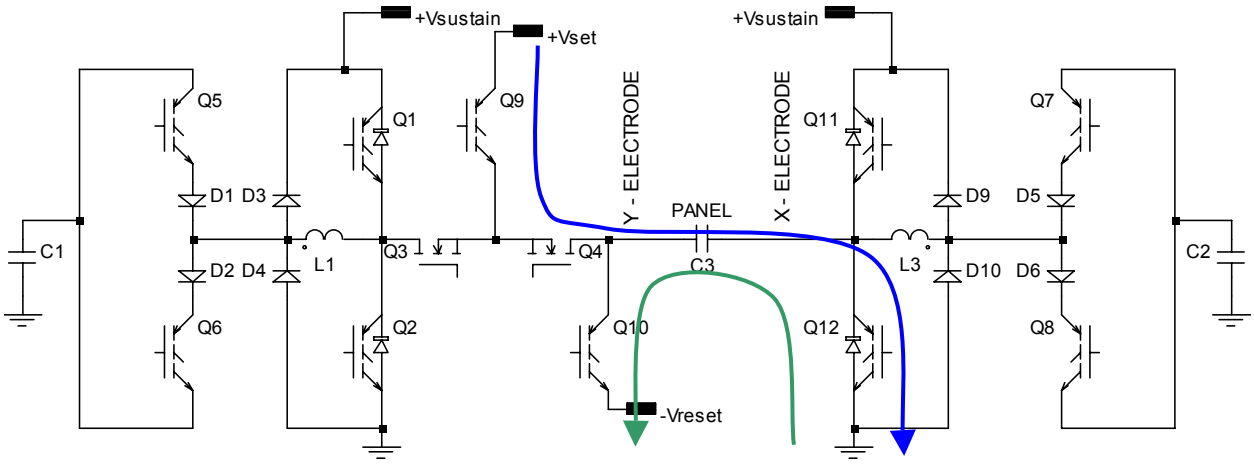


Figure 13. Current path when the panel is reset.

During positive reset, Q9, Q4 and Q12 are turned on. During negative reset only Q10 and Q12 are turned on.

4. PDP Power Devices Characteristics

After studying sustain circuit behavior discussed previously, it can be concluded that the following characteristics applied to the power devices for PDP applications:

- High peak current capability
- Low forward voltage drop
- Fast turn on capability

It can also be seen that for power devices on the ER and Discharge circuits, the current follows a half sinusoidal pattern. Since the circuit can be considered as a series resonant LCR circuit, the current at turn on is zero (zero current switching) and the voltage at turn off is zero (zero voltage switching). These switching behaviors are characteristics of a soft switching converter. For ER and discharge circuits, MOSFETs or IGBTs can be chosen for power devices. If IGBTs are selected for discharge circuit, an anti-parallel diode must be connected across each IGBT to carry any reverse current that might occur. A MOSFET has an intrinsic body diode across it. Therefore, a MOSFET does not require an anti-parallel diode when selected as power devices on the discharge circuit. For ER circuit, IGBTs do not require an anti-parallel diode since reverse current will be blocked by the diodes in series with the devices. These are diodes D1, D2, D5 and D6. MOSFETs can also be used as power devices on the ER circuit.

Additional protection to clamp the voltage on the inductors is provided by D3, D4, D9 and D10. These diodes are used to shunt over voltages on these nodes that might damage devices on the ER circuit.

Pass circuit has to carry both ER and Discharge currents. It can be seen that during ER and discharge cycles, the pass circuit remains on. The circuit switches on and off only during reset period which occurs at the end of each subfield. It is required for pass circuit to have very low voltage drop. In addition, pass circuit has to carry current in both directions. MOSFETs can carry current in both directions and are used for this circuit.

5. PDP Power Devices From International Rectifier

International Rectifier has released a family of trench gate MOSFETs and trench gate IGBTs that are suitable for PDP applications. For ER and discharge circuits, new devices that have very fast turn on and low voltage drop were developed. In order to compare the characteristics of PDP power devices with devices not optimized for PDP application a test circuit was created. This circuit is shown in Figure 14. Q1 is the device under test (DUT), L1 is circuit inductance and C1 is panel capacitance. Gate voltages used to drive the power devices are also shown in this Figure.

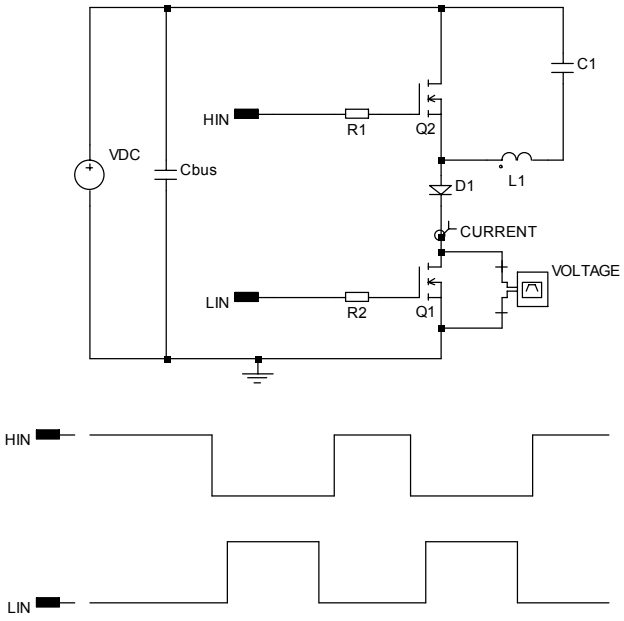


Figure 14. Epulse™ Test Circuit. Q1 is device under test, L1 = load inductor, C1 = panel capacitance.

Using this circuit, current into the DUT is half sinusoidal, simulating actual current in the panel. A new parameter called Epulse™ is defined. Epulse™ is a measurement quantity combining turn on energy loss and conduction loss for one current pulse on the ER or discharge circuits. The unit is in Joules and the equation can be written as:

$$Epulse^{TM} = \int_0^{tpulse} Vdevice \times Idevice\, dt \quad \text{.....(4)}$$

Typical current waveform from this circuit is shown in Figure 15. Due to the reactive nature of the load, the voltage across the DUT falls rapidly followed by a rapid rise in the current. Once the panel, represented by C1 is charged, current will decay to zero. Instantaneous power across the device is also shown which is used to calculate the energy per current pulse or Epulse™ according to Equation (4).

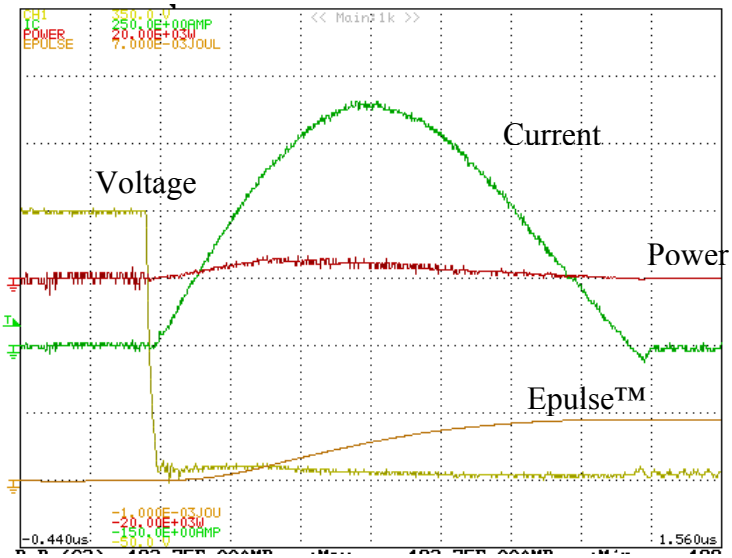


Figure 15. Typical Epulse™ voltage, current, power and energy waveforms.

By using Epulse™ , power dissipation of the power device can be estimated. Power dissipation can be calculated by multiplying Epulse™ with the number of current pulses per second.

Pdissipation = Epulse™ x number of current pulses/second (Watts)…… (5)

For instance, if there are 10,000 pulses at 160 Ampere, power dissipation for IRGB4055PbF PDP IGBT can be calculated as:

Epulse ™ = 380 uJoule/pulse x 10,000 pulses/second = 3.8 Watts

Typical Epulse™ versus collector current for IRGB4055PbF trench gate IGBT is shown in Figure 16. By using this graph and knowing the number of current pulses per second, power dissipation calculation can be easily done.

Comparisons between devices not optimized for PDP and the ones designed for PDP applications are presented in **Figure 17**. It can be seen that the device not optimized for PDP application has large voltage drop compare to the device that is optimized for one.

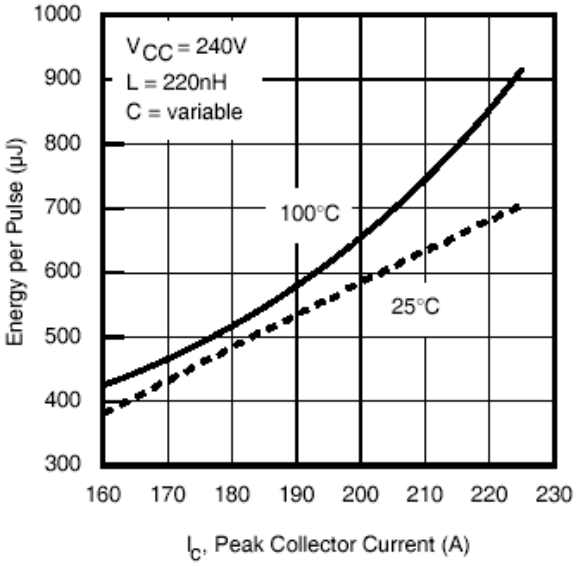
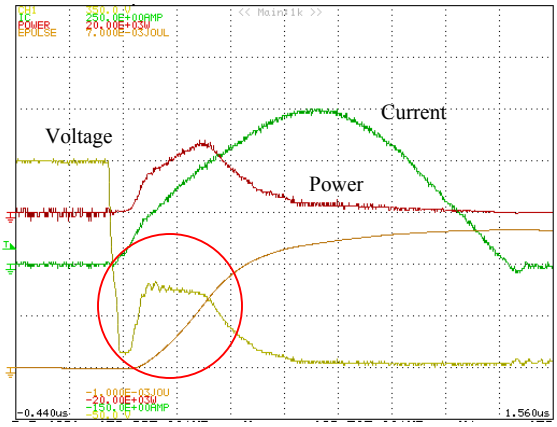
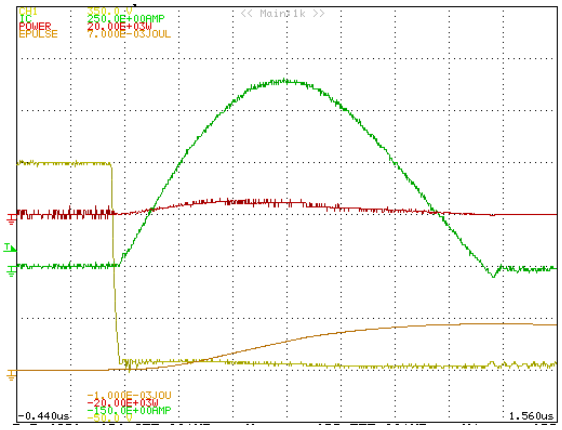


Figure 16. Epulse™ versus collector current for IRGB4055PbF trench gate IGBT.



(a) Non PDP optimized device with large voltage drop



(b) PDP optimized device

Figure 17. Comparisons between non PDP and PDP optimized devices

Another important parameter for PDP power devices is the ability for the device to remain off when current falls to zero and the complementary device is turned on. As can be seen from the schematic in Figure 14, if both Q1 and Q2 are accidentally turned on, a large current will flow through the devices causing shoot through failure. This failure can be avoided by proper circuit layout and by selecting devices that are immune to it. International Rectifier PDP power devices were designed to handle a minimum of 100 nsec dead time between the high side and low side gate signals without causing shoot through conditions.

The ability to handle large repetitive peak current (Irp) for PDP power devices is also important. International Rectifier PDP devices were designed with repetitive large peak current handling capability given that the junction temperature of the device was maintained below the maximum allowable by the datasheet.

The values of repetitive peak current is calculated using the formula:

$$Tj = Tcase + Zth \times Vdevice\ x\ Idevice\ (at\ Tj) \text{ .....(6)}$$

Where:
Tj = Device junction temperature
Tcase = Case temperature
Zth = Thermal resistance at a specific pulse width and duty cycle
Idevice = Device current
Vdevice = Voltage drop across the device at junction temperature

The datasheet of PDP power devices from International Rectifier includes a graph of repetitive peak current versus case temperature for half sine wave current pulse with width equals to 1 usecond and duty cycle equals to 25%. As an example, the typical repetitive peak current versus case temperature for IRGB4055PbF is presented in Figure 18.

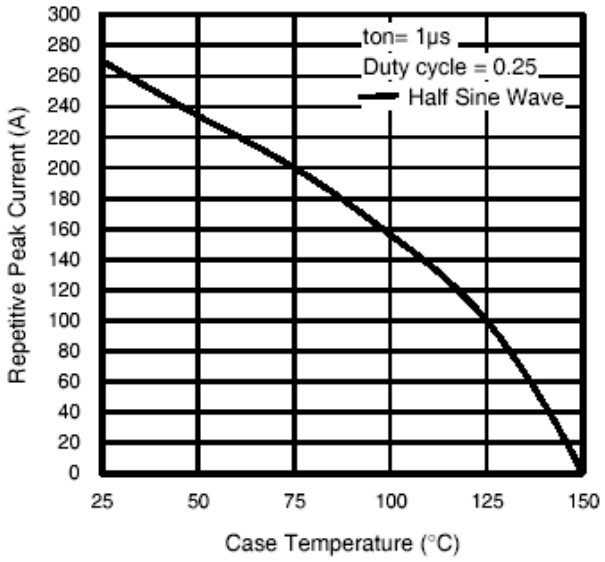


Figure 18. Repetitive peak current versus case temperature for IRGB4055PbF trench gate IGBT.

For pass circuit, MOSFETs are the device of choice since this circuit is required to conduct current in both directions. Although the switching frequency is relatively low, the RMS current through this circuit is very large since it has to conduct both ER and discharge currents. The latest trench gate MOSFETs from International Rectifier are ideal for this application since this technology allow the die to have very high current density and therefore reduce the number of paralleled devices required to maintain very low voltage drop. In addition, these PDP MOSFETs were designed to have both

repetitive and single pulse avalanche capabilities that make them very rugged [5]. These avalanche ratings are necessary in order to guarantee that the MOSFETs will not fail when subjected to voltage spikes. Although PDP application is soft switching and devices are not subject to avalanche, having this rating allow lower voltage MOSFETs to be used and still maintain acceptable voltage margin required by the design. In general the lower the voltage rating of the MOSETs the lower the voltage drop across them. It can be seen in Figure 19, avalanche characteristics of IRFP4232PbF MOSFET. This MOSFET is a 250V rated device with minimum avalanche voltage rating of 300V. This Figure also shows single pulse and repetitive avalanche energy that the device can handle.

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	220	mJ
E_{AR}	Repetitive Avalanche Energy ①	—	43	mJ
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	300	—	V
I_{AS}	Avalanche Current ②	—	42	A

Figure 19. PDP MOSFETs avalanche characteristics of IRFP4232PbF Trench Gate MOSFET.

The last circuit to be discussed is the Set and Reset circuit. This circuit applies asymmetrical AC voltage across the panel in order to purge the cells of any remaining surface charge. This is done at the end of each subfield (or the beginning of the next subfield). Since a slow ramping voltage is required, the power devices on this circuit operate in the linear mode. This means that the current through the device is relatively low but the voltage drop is very large. The devices operate similar to a variable resistor in the Set and Reset circuit.

Figure 20 shows PDP MOSFETs from International Rectifier based on trench gate technology. This table also shows possible circuit use for the devices based on their break down voltage capability. It can also be noted that these MOSFETs are designed with ±30V gate rating capability.

PDP Trench Gate MOSFETs

P/N	BVdss/Irp	Vds(avalanche)	Vgs	Package	Circuit
IRFx4227PbF	200V/185A	240V	±30V	TO220FP, D2PAK, TO220	ER, Pass
IRFB4233PbF	230V/160A	276V	±30V	TO220	ER, Discharge, Pass
IRFP4232PbF	250V/160A	300V	±30V	TO247	Discharge, Pass
IRFP4242PbF	300V/130A	360V	±30V	TO247	Discharge, Pass

x: B=TO220, I=TO220FP, S=D2PAK, P=TO247

Figure 20. International Rectifier PDP Trench Gate MOSFET ratings and possible circuit use.

Figure 21 shows PDP IGBTs from International Rectifier based on trench gate technology. This Figure also shows possible circuit use for the device. It can also be noted that these IGBTs are designed with ±30V gate rating capability.

Power devices in the Set and Reset circuits operate in the linear mode and will have to block up to 600V due to the requirement of asymmetrical Set and Reset voltages. Typical voltage values for Set and Reset voltages are +400V and -150V, respectively. International Rectifier older generation planar IGBTs are the best choice for this circuit due to its ruggedness for linear application. Example devices are IRG4BC20S (TO220) or IRG4BC30S-S (D2PAK).

PDP Trench Gate IGBTs

P/N	BVdss/Irp	Vgs	Package	Circuit
IRGx4065PbF	300V/205A	±30V	TO220FP, TO220, TO247	ER and Discharge
IRGP4065DPbF	300V/205A	±30V	TO247- copack	Discharge
IRGB4055PbF	300V/270A	±30V	TO220, TO247	ER and Discharge
IRGP4055DPbF	300V/270A	±30V	TO247- copack	Discharge

x: B=TO220, I=TO220FP, S=D2PAK, P=TO247

Figure 21. International Rectifier PDP Trench Gate IGBT ratings and possible circuit use.

6. Soft Switching in PDP Application

It is discussed previously; PDP panel can be represented as a three-electrode capacitor. The current in the sustain circuit is sinusoidal as shown in Figure 8 and Figure 10. Once panel capacitance is charged, voltage will fall to zero at turn off (Zero Voltage Switching). In addition, current will be at zero at turn on (Zero Current Switching). Therefore it can be seen that during switching events, high current and high voltage will not happen at the same time as shown in Figure 22.

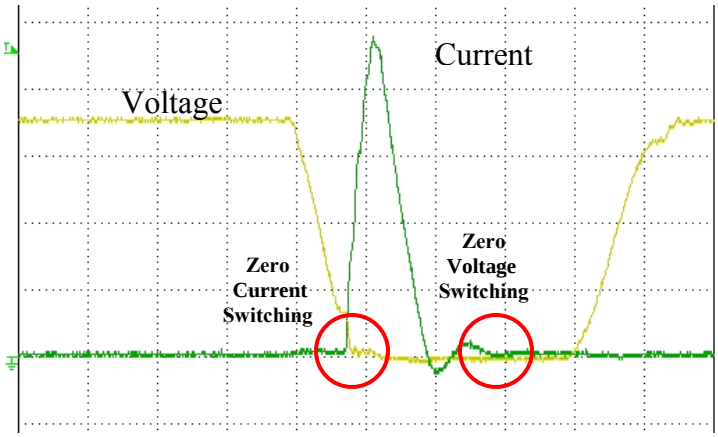


Figure 22. Soft switching in PDP application. Zero voltage switching at turn-off and zero current switching at turn-on.

From the above Figure, it can be concluded that typical switching parameters such as td(on), tr, td(off) and tf for hard switching applications do not apply for power devices designed for PDP application.

For clarity, typical hard switching waveforms are shown in Figure 23 and Figure 24. As it can be seen from these Figures, high voltage and high current always occur at the same

time contributing to device power dissipation. These waveforms are typical of switch mode power supply (SMPS) or motor drive applications.

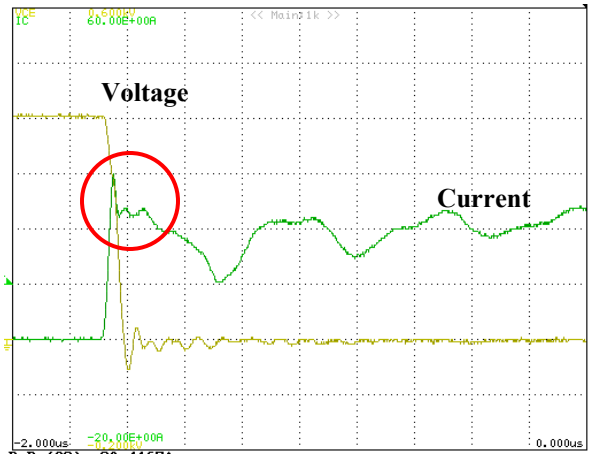


Figure 23. Typical hard switching turn-on waveforms. High voltage and high current occur at the same time

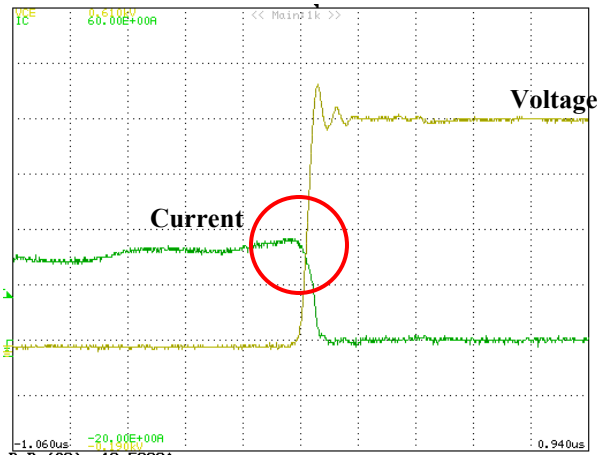


Figure 24. Typical hard switching turn-off waveforms. High voltage and high current occur at the same time.

7. Paralleling PDP Power Devices

In order to increase current density, multiple power devices can be used in parallel. The following guidelines should be applied when paralleling power devices:

- Use individual gate resistor for each device to eliminate risk of oscillation.
- Equalize common source or emitter inductance by proper circuit layout.
- Ensure that each device is driven by a gate drive with sufficient current handling capability with as little impedance as possible.

- Do not place zener diode directly across gate to emitter/source to control over voltage. This will cause oscillation in the gate of the device. Instead place the diode on the driver side and use a gate isolation resistor when necessary.
- Do not place capacitor directly across gate to emitter/source to control switching time. Adjust gate resistor value instead.

In addition, parameter variations on the power devices will also effect current sharing performance among the devices. Parameters that will affect current sharing performance are threshold voltage, gate capacitance, voltage drop and device gains. It is recommended that when paralleling devices, device parameters are matched. International Rectifier provides device matching services for package parts and also for individual die. In the event that the parameters cannot be matched, ensure that the junction temperature of each device is kept below the maximum allowable junction temperature.

8. Design Example

Assume the following requirements for a PDP
Vsustain = 185V
Vset = 400V
Vreset = -150V
ER current = 80A
Sustain discharge current = 120A
8 bit ADS method
Tsink = 55°C
Tj(max) = 100°C

Analysis:
For ER circuit, maximum voltage stress is Vsustain / 2 = 92.5V
For discharge circuit, maximum voltage stress is Vsustain = 185V
For pass circuit Q3, maximum voltage stress is (Vsustain + Vset)/2 = 292.5V
For pass circuit Q4, maximum voltage stress is (Vset + abs(Vreset))/2 = 275V
For set circuit Q9, maximum voltage stress is (Vsustain + Vset) = 585V
For reset circuit Q10, maximum voltage stress is Vset + abs(Vreset) = 550V

Based on the above voltage stress analysis, the following devices are selected:

Circuit	Voltage Stress	Device	Type
ER	92.5V	IRGB4065PbF	IGBT
Sustain	185V	IRGB4055PbF	IGBT
Pass1	292.5V	IRFP4242PbF	Mosfet
Pass2	275V	IRFP4242PbF	Mosfet
Set	585V	IRG4BC20S	IGBT
Reset	550V	IRG4BC20S	IGBT

Figure 25. Device selection based on voltage stress analysis

IRGB4065PbF is selected for ER circuit based on the following calculations. From IRGB4065PbF datasheet, Epulse™ at 80A is 200uJ and Irp = 120A at 100°C.
Pdissipation = 200 uJ/pulse x 256 pulses/field x 60 fields/second = 3.07 W.

Similar calculation can be performed to determine power devices for the other circuit sections.

9. Conclusions

Based on Figure 5, PDP sustain circuit can be grouped into the following functions:

- ER circuit which consists of Q5, Q6, Q7, Q8, D1, D2, D5, D6
- Discharge circuit which consists of Q1, Q2, Q11 and Q12
- Pass circuit which consists of Q3 and Q4
- Set and Reset circuit which consists of Q9 and Q10

International Rectifier had developed power devices suitable for PDP application with the following characteristics:

- High peak current capability
- Low forward voltage drop
- Fast turn on capability

In addition, new parameters are defined for PDP power devices that include Epulse™, and repetitive peak current (Irp). Epulse™ is a combined measurement of turn on and conduction energy losses that allow easy power dissipation calculation. Repetitive peak current (Irp) determines how much current device can safely carry based on device case temperature. Finally, Vds(avalanche) voltage is also specified for PDP MOSFETs in order to provide ruggedness and necessary voltage margin on the device required by the design.

PDP power devices based on trench gate MOSFETs and IGBTs are presented in Figures 20 and 21, respectively. They show electrical characteristics of the devices and their possible use in PDP sustain circuit application.

10. References

[1] H. Van der Broeck, "Application and Integration Opportunities in Switched Mode Power Supplies", MICRO.tec2000 Conference, Hanover, Germany 2000

[2] T. Shinoda, "Fabrication Technologies of Plasma Display Panels", IEEE Industrial Application Society Conference 2003.

[3]K.Yoshikawa, et al, "A Full Color AC Plasma Display with 256 Gray Scales", Proceedings of IDRC, 1992.

[4] L.F. Weber and R.C. Younce, "Independent Sustain and Address Plasma Display Panel", U.S Patent 4924218, May 1990.

[5] T. McDonald, et al, "Power Mosfets Avalanche Design Guidelines", International Rectifier Application Note AN-1005, Rev. 1.0.