Application Characterization of IGBTs

Topics Covered:

Gate drive for IGBTs
Safe Operating Area
Conduction losses
Switching losses
Device selection and optimization
Thermal design
How to replace a power MOSFET
Paralleling
How to select devices for paralleling

SCOPE

This application note covers some of the major issues normally encountered in the design of an IGBT power conditioning circuit. It is the companion to AN-983, "IGBT Characteristics," which covers the details of the device, rather than its application (http://www.irf.com/technical-info/appnotes/an-983.pdf).

I. GATE DRIVE REQUIREMENTS

A. Impact of the impedance of the gate drive circuit on switching losses

The gate drive circuit controls directly the MOSFET channel of the IGBT and, through the drain current of the MOSFET, the base current of its bipolar portion. Since the turn-on characteristics of an IGBT are determined, to a large extent, by its MOSFET portion, the turn-on losses will be significantly affected by the gate drive impedance. Turn-off characteristics, on the other hand, are chiefly determined by the minority carrier recombination mechanism, which is only indirectly affected by the MOSFET turn-off. An increase in gate drive impedance prolongs the Miller effect and causes a delay in the current fall. This delay is emphasized in Figure 1 with the addition of a 47Ω gate resistor.
The impact of the gate drive impedance on total switching losses depends on the basic design of the IGBT and its speed. The impact on *turn-on losses* is appreciable for all IGBTs from International Rectifier, regardless of speed. The impact on *turn-off* losses depends on the speed of the device: the faster the IGBT the greater its sensitivity to the gate drive impedance. In any event, *additional* gate drive impedance has a lower *marginal* impact, i.e. the same amount of additional drive impedance will have a lower effect if the gate drive impedance is already high.

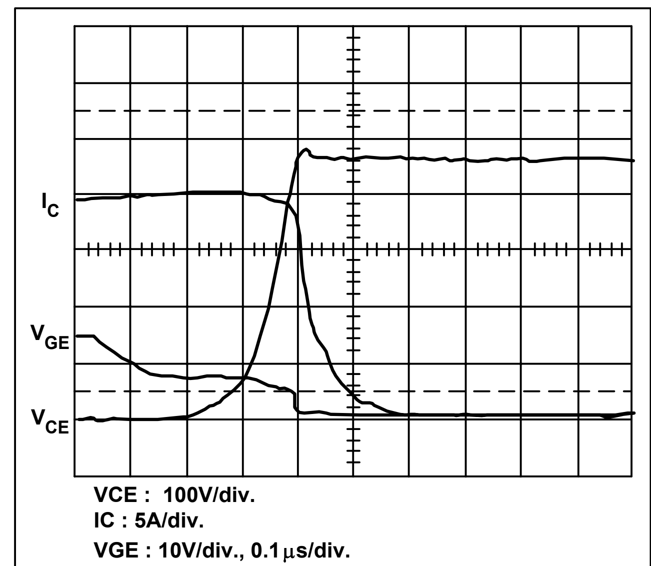

Figure 1. Turn-off waveform of an IRGBC40F with a 47W gate resistor. Notice the turn-off delay of the current waveform during the Miller effect.

It follows that the *total switching losses* of Fast IGBTs will be less affected by the characteristics of the gate drive circuit than that of Ultrafast IGBTs. These last ones are more sensitive to it and stand to benefit the most from a low impedance gate drive. The specific dependence of the switching energy on gate drive resistance is shown in the data sheet.

B. Impact of the gate drive impedance on noise sensitivity

In an IGBT, any dv/dt that appears on the collector is coupled to the gate through a capacitive divider consisting of the Miller capacitance and the gate-to-emitter capacitance. If the gate is not solidly clamped to the emitter, a large enough dv/dt will take the gate voltage beyond the gate threshold and the IGBT will conduct. As it goes into conduction it clamps the dv/dt that is causing it to conduct so that the gate voltage never goes much beyond the threshold voltage. The end result is a limited amount of "shoot-through" current, with an increase in power dissipation. To reduce noise sensitivity and the risk of this dv/dt-induced turn-on, the gate drive impedance must be very low when the device is in the off-state and the gate voltage is close to zero. Frequently a negative gate bias is used to improve noise immunity. This requires additional isolated supplies. An effective alternative is to design a layout that minimizes the inductance of the gate charge/discharge loops with parallel PCB tracks or twisted wires for the gate drive. In some cases the effects of a contained amount of dv/dt induced turn-on, i.e. a small increase in power dissipation, can be an appealing alternative to the added complexity of the negative gate bias.

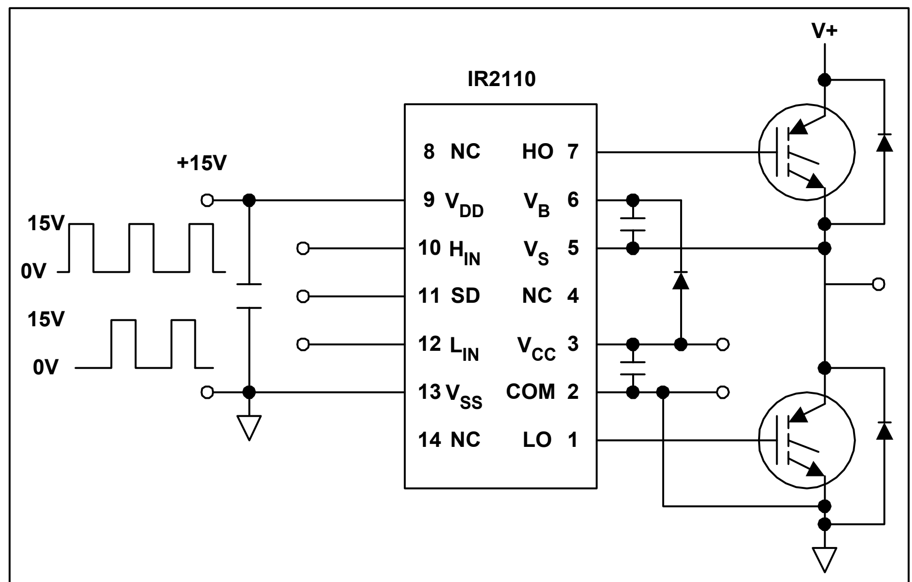

Figure 2. The IR2110 provides a simple, high performance, low cost solution to the problem of driving a Half-Bridge.

Gate drive impedance is frequently increased for a practical reason: to reduce the current spike and ringing at turn-on caused by the reverse recovery of the diode. This resistance can be safely bypassed with an anti-parallel diode to reduce the turn-off losses, as explained in AN-978, Section 3.b (http://www.irf.com/technical-info/appnotes/an-978.pdf). For most applications, the circuit shown in Figure 2 provides a simple, low cost, high performance solution to the gate drive requirements of most applications.

MOS-Gate Driver integrated circuits are available to perform the current limiting and short circuit protection function by means of the gate voltage. One such example is shown in Figure 3.

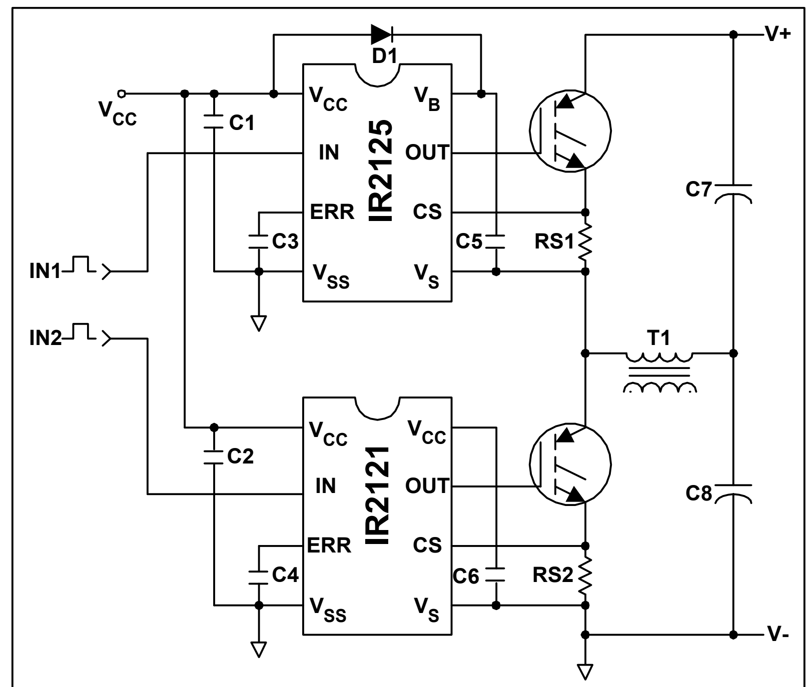

Figure 3. Short circuit protection performed with MOS gate driver ICs

C. Contribution of "common emitter inductance" to the impedance of the gate drive circuit

The "common emitter inductance" is the inductance that is common to the collector circuit and the gate circuit (Figure 4a). This inductance establishes a feedback from the collector circuit to the gate circuit that is proportional to Ldi_C/dt. The voltage developed across this inductance subtracts from the applied gate voltage during the turn-on transient and adds to it during turn-off. In so doing, it slows down the switching.

This phenomenon is similar to the Miller effect, except that it is proportional to the di/dt of the collector current rather than the dv/dt of its voltage. In both cases the feedback is proportional to the transconductance of the IGBT, which is much larger than that of a MOSFET of the same die size. A di_C/dt of 1A/ns is quite common in IGBT circuits and voltages in the order of 10V could be expected in 10 nH of common emitter inductance, except that the feedback mechanism slows down the turn-on process and limits the di_C/dt.

Simple layout precautions can reduce the common emitter inductance to the bare minimum that is already in the package. Separate wires to the emitter pin should be provided for the emitter and the gate return, as shown in Figure 4b. The gate lead and the gate return lead should be twisted or run on parallel PCB tracks to minimize inductance in the gate drive path. This improves immunity to dv/dt induced turn-on and reduces ringing in the gate.

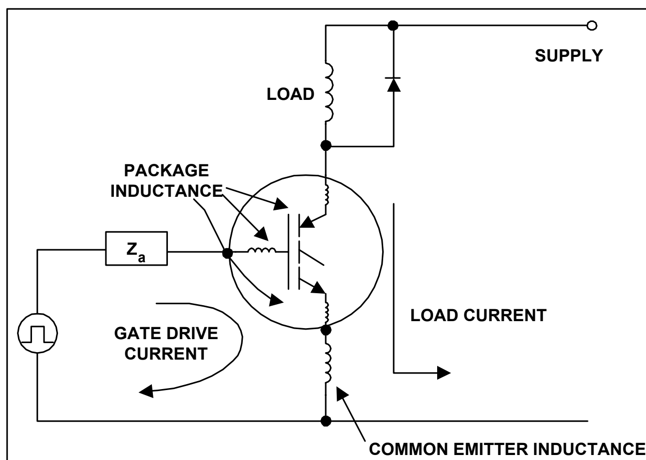

Figure 4a. " Common Emitter Inductance" is the inductance that is common to the collector current and the gate drive current

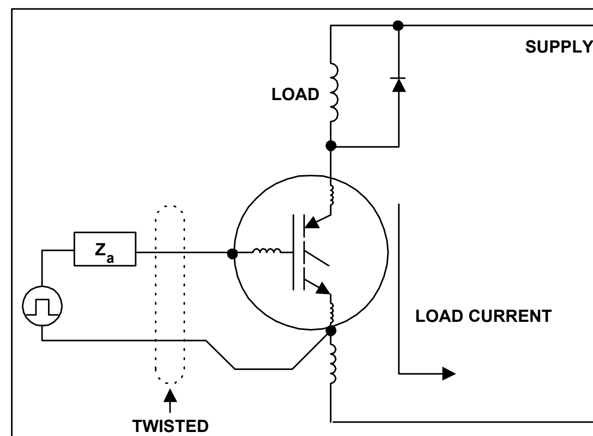

Figure 4b. " Common Emitter Inductance" can be eliminated by running separate wires to the emitter pin, one for the emitter, the other for the gate drive return.

D. Gate charge vs. input capacitance

The difference between gate capacitance and gate charge is covered in AN-944 (http://www.irf.com/technical-info/appnotes/an-944.pdf). Designers that are familiar with the limited usefulness of the input capacitance concept can safely skip this section.

Input capacitance is frequently used for two purposes:

- as a figure of merit of switching performance;
- as a reference point to design a gate drive circuit.

On both counts, the use of data sheet capacitance tabular information gives results that are not useful.

As shown in Figure 5, IGBT capacitances change significantly with collector voltage to the point that no capacitance number is meaningful by itself, unless a voltage is associated with it.

Even disregarding the voltage dependence, input capacitance is not a good figure of merit of switching performance, neither for MOSFETs, nor for IGBTs. As far as MOSFETs go, a device with lower input capacitance can be slower than one with higher input capacitance, depending on threshold, transconductance and total gate charge (see Figure 6 of AN-944). A conspicuous example of this is the fact that logic level devices are faster than their standard gate counterparts, in spite of a larger input capacitance [1].

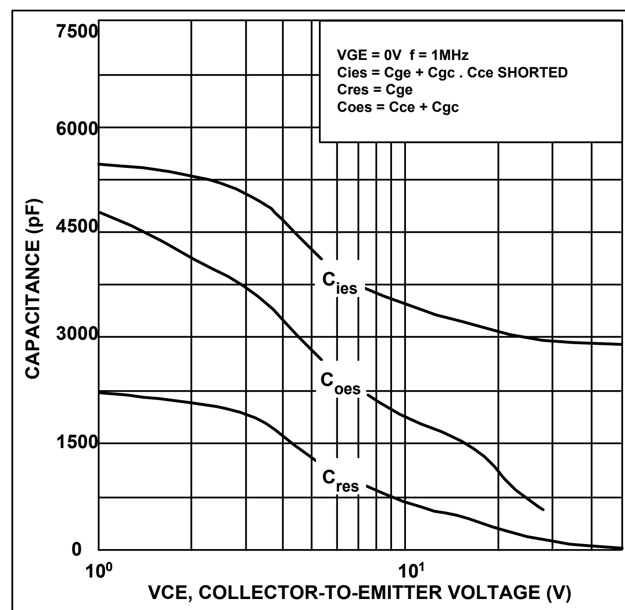

Figure 5. Typical capacitance vs VCE, IRGPC50U. The variation of Cres and Cies with collector voltage makes the concept of capacitance virtually useless.

In the specific case of IGBTs, which are minority carrier devices, the switching behavior is dominated by injection and recombination phenomena and only the turn-on behavior is affected by gate drive conditions in a significant way.

As a guideline to design the gate drive circuit, the input capacitance underestimates the gate drive requirements. Normally the charge required by the gate for one switching operation corresponds to an input capacitance that is two to three times larger than the data sheet value. As explained in AN-944, this is due to the Miller component of the input capacitance. Thus, gate drive circuits designed on the basis of input capacitance are generally inadequate and result in poor switching operation and noise susceptibility. The sizing of the gate drive circuit is more appropriately done using the gate charge specified in the data sheet.

II. SWITCHING TRAJECTORIES AND SAFE OPERATING AREA CONSIDERATIONS

Minority carrier devices, when subjected to high levels of voltage and current, can experience uneven current distributions within the die that, taken beyond safe limits, can cause device failure. The current distribution takes different forms, depending on the sign of the di/dt associated with it. Hence, the Safe Operating Area curve, which was devised as a convenient representation of this limitation, is frequently differentiated into "Forward Biased SOA" and "Reverse-Biased SOA".

The Forward Biased SOA curve applies to linear operation in Class A or Class B or during short circuit, which can be considered an extreme case of Class B operation. Thermal limitations for pulsed operation are frequently included in this curve, even though the Transient Thermal Response curve provides this same information in a more comprehensive and accurate way. Due to the limited use of these devices in linear operation, the FBSOA curve is frequently omitted from the data sheet. The Reverse Biased SOA applies when switching off a clamped inductive load, including the turn-off from a short circuit condition.

Figure 6 shows the importance of the Reverse Biased SOA. During the turn off of a clamped inductive load, the voltage across the transistor goes from the low value of $V_{CE(sat)}$ to the full supply voltage while the collector current stays constant. After the collector voltage exceeds the supply voltage by a diode drop, the diode starts to conduct, thereby taking over the inductor current from the transistor. Thus the trajectory of the operating point moves along a constant current line until it intercepts the supply voltage, at which point a voltage overshoot normally occurs, whose magnitude depends on the amount of stray inductance L_S and the turn-off speed. A more detailed explanation of the switching trajectories can be found in Ref. [2].

It will be appreciated that, for a safe commutation of the load current, the entire trajectory must lay within the turn-off SOA and that any limitation in the RBSOA will translate into a limitation of turn-off capability of inductive loads. Load-shaping snubbers have been used in conjunction with bipolar transistors to lower the trajectory below the second breakdown limit.

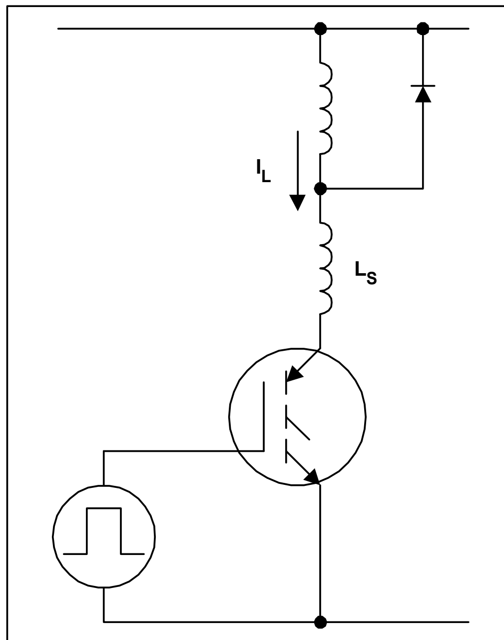

Figure 6a. Typical clamped inductive load

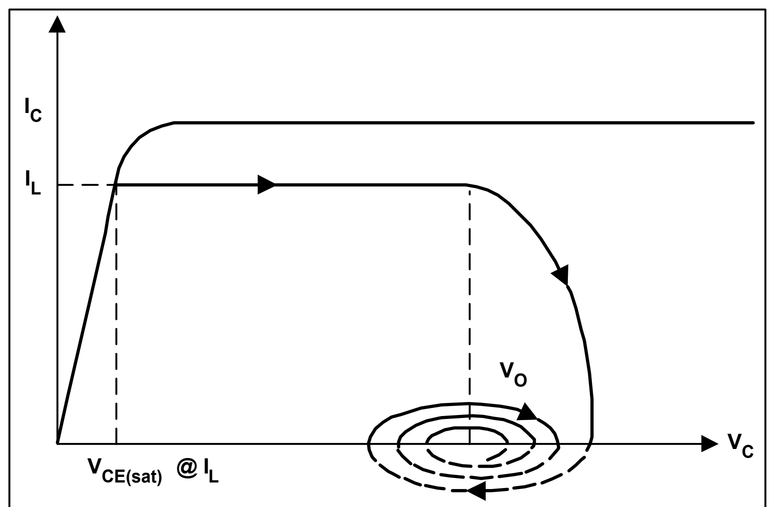

Figure 6b. During a turn-off transient, the trajectory of the operating point traverses the SOA curve. Second breakdown would place limits to the free evolution of the trajectory.

Due to the wide base and, hence, low gain of its bipolar portion, the second breakdown of International Rectifier's IGBTs occur at current and voltage levels that are significantly higher than what is normally encountered in a practical application, as shown in the data sheets. Notice that the values therein contained apply at high temperature and that load-shaping snubbers are not necessary, as long as the switching trajectory is confined within the turn-off SOA. In addition to load shaping, snubbers can be used to limit overshoots and/or reduce EMI. This function is not related to SOA and is covered in many publications.

III. CONDUCTION LOSSES

At any given time, the energy dissipated in the IGBT can be obtained with the following expression:

$$E = \int_0^t V_{CE}(i)\, i(t)\, dt$$

where t is the length of the pulse. Power is obtained by multiplying energy by frequency, if applicable. When the transistor is off $i(t) \cong 0$ and losses are negligible. Unfortunately, no simple expression can be found for the voltage and current functions during a switching transient. Hence, for analytical expediency, we resort to a somewhat artificial distinction between conduction and switching losses.

We define conduction losses the losses that occur between the end of the turn-on interval and the beginning of the turn-off interval, as defined for the switching losses characterization. Since the turn-on energy is measured from 5% of the test current to 5% of the test voltage and the turn-off energy is measured starting from 5% of the test voltage, conduction losses occur when the voltage across the IGBT is less than 5% of the test, or supply, voltage (see AN-983, Section 8.5). The function $V_{CE}(i)$ in the formula above characterizes the conduction behavior of the IGBT. This information is provided in the data sheet with graphs and specific values.

The tabular information in the data sheet provides a few limit points that, with the help of the graphs, can be used to generate the information necessary to calculate the conduction losses. To obtain the max voltage drop at any current and temperature, from the data sheet values, a two step procedure can be followed

1. Obtain a typical value for the collector voltage by interpolating a curve in the Collector Voltage v. Collector current figure of the data sheet at the desired current level and the appropriate junction temperature.
2. To obtain a maximum value, the voltage drop read from this curve at the appropriate junction temperature is multiplied by the ratio between maximum and typical from the Table of Electrical Characteristics.

Finally, conduction losses must be multiplied by conduction time (if the desired result is energy) or duty cycle (if the desired result is power).

If the current waveform is not constant during the conduction interval, it should be broken up into smaller intervals, calculating the losses for each sub-interval and summing the results, rather than averaging or taking its RMS value. An appealing alternative would be to generate a simple function by means of a curve-fitting algorithm. This function could be easily integrated by mathematical routines.

IV. LOSSES IN HARD SWITCHING

Losses in hard switching have been separated into two components that will be analyzed separately: turn-on losses and turn-off losses.

Like conduction losses, "hard switching" operation is characterized with tabular information and with graphs in the data sheet.

As explained in AN-983, Section 8.5, the Switching Energy reported in the data sheet makes specific reference to a test circuit that simulates a clamped inductive load. Switching energy data are in millijoules. These numbers must be multiplied by frequency to obtain power losses.

It is important to remember that switching energy changes significantly with temperature and all calculations should be carried out with numbers that are appropriate for the worst case operating temperature.

Like conduction losses, switching losses can be handled with relatively simple analytical algorithms.

A. Turn-off losses

Turn-off losses can be calculated with the same two-step technique described in the previous section, complemented by two additional corrections:
1. The energy loss thus obtained must be scaled with voltage. Data sheet measurements have been taken with a defined supply voltage that may or may not be the same as the supply voltage of the specific application.
2. Similarly, the gate drive resistance of the test circuit in the data sheet may be different from what is used in the actual application. Most data sheets have a figure that correlates switching energy with gate drive impedance.

B. Turn-on losses

The turn-on transient of a clamped inductive load is complicated by the reverse recovery of the anti-parallel diode of the complementary device. When the IGBT turns it will take over the entire load current ***plus*** the reverse recovery current of the diode that was carrying the current when the IGBT turns on.
Switching energy data in recent data sheets include the "diode induced" losses. Thus, the turn-on losses can be calculated with the same procedure described above for the turn-off losses.
Earlier data sheets used a different test circuit described in AN-983, Section 8.5. This test circuit measures turn-on energy without the diode induced losses. It follows that, to obtain the total turn-on losses two components have to be calculated:

- turn-on or total losses with an ideal diode
- the additional turn-on losses in the IGBT due to the reverse recovery of the freewheeling diode.

The following sections show how to calculate these two components. It should be kept in mind that there are topologies where the switches do not normally have turn-on losses, nor are they subject to recovery transients. This is true for flybacks as well as other ZVS topologies.

C. Contribution of the diode reverse recovery

In a typical clamped inductive load in continuous current mode, the turn-on of a switch causes a reverse recovery in the freewheeling diode and a large current spike in the device that is being turned on (Figure 7). This increases the turn-on losses in the IGBT with respect to the data sheet characterization done with the "ideal diode" test circuit of the older data sheets.

No simple expression can be provided for these additional losses, as they depend on a number of factors: turn-on speed, di/dt, stray inductance and diode characteristics. Several have been proposed, based on simplifying assumptions. The following assumes that the voltage across the diode stays close to 0V during the length of t_a, rising to the supply voltage during t_b.

$$E = VI_L[(1+\frac{1}{2}\frac{I_{rr}}{I_L})t_a + \frac{1}{4}\frac{I_{rr}}{I_L}t_b]$$

$$= V(I_L t_a + Q_a + \frac{1}{2}Q_b)$$

where V and I_L are supply voltage and load current, I_{rr} is the peak reverse recovery current, t_a and t_b are the two components of t_{rr} and Q_a and Q_b the charges associated with them. The first two terms represent the losses during t_a, one due to the load current, the other due to the reverse recovery current. The third term represents the losses during t_b, which are partly in the IGBT, partly in the diode.

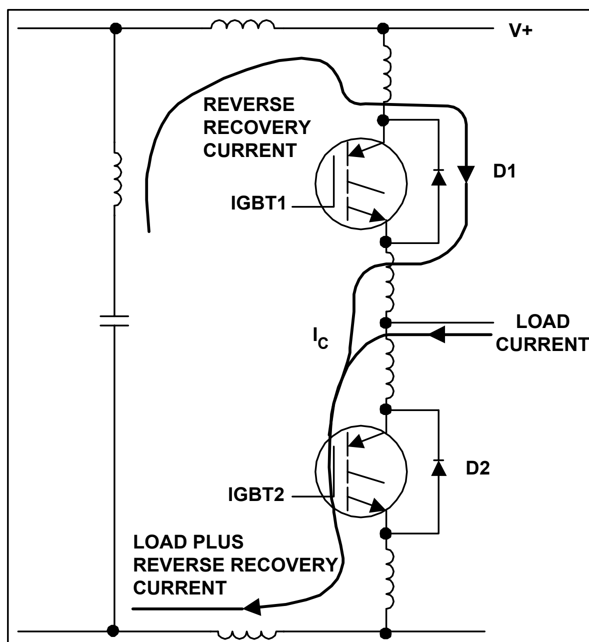

Figure 7a. Typical clamped inductive load showing stray circuit inductances. Load current was flowing in D1 previous to IGBT2 turning on. At turn-on IGBT2 takes over load current and reverse recovery current of D1

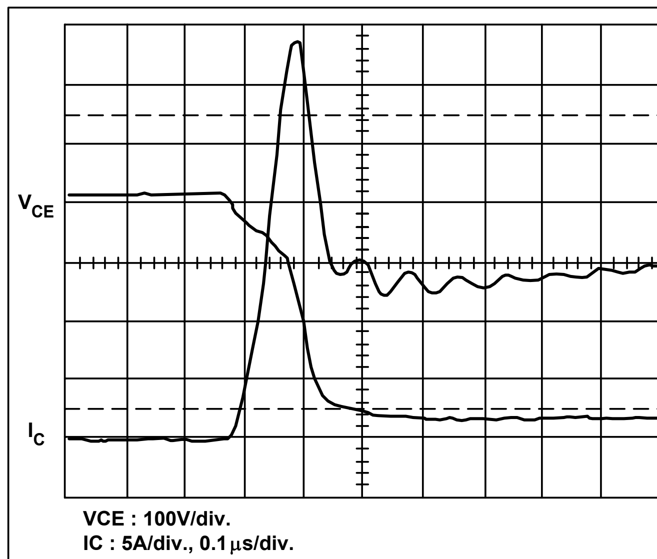

Figure 7b. Turn-on current in IGBT2.

V. TRADE-OFF BETWEEN CONDUCTION AND SWITCHING LOSSES: DEVICE OPTIMIZATION

To compare different devices or technologies, silicon designers often resort to curves of voltage drop vs. current density like those shown in Figure 8. These curves ignore the dynamic behavior of the device and, since in a typical switchmode application a significant portion of the temperature rise is due to the switching losses, they are not useful in the device selection.

Furthermore, it is frequently inferred, from those curves, that a technology is superior if it is capable of operating at higher current densities. In a specific application, operation at higher current densities means smaller die sizes and, consequently, higher thermal resistances. If total losses stay the same, this implies higher operating junction temperature, with all its negative connotations.

It follows that, for a given thermal design, operation at higher current densities will be advantageous only if the higher thermal resistance is compensated by lower total losses.

To quantify these considerations a simple method has been developed comparing different power devices in a typical Switchmode environment. This method takes all critical aspects into account: thermal constraints, conduction and switching losses.

The popular half-bridge operated with a clamped inductive load was chosen as the benchmark circuit to compare the Performance of different IGBTs. Operating conditions are listed in Figure 9 and they can all be changed to suit a specific application. Flyback or resonant circuits could be used in place of the half-bridge to obtain

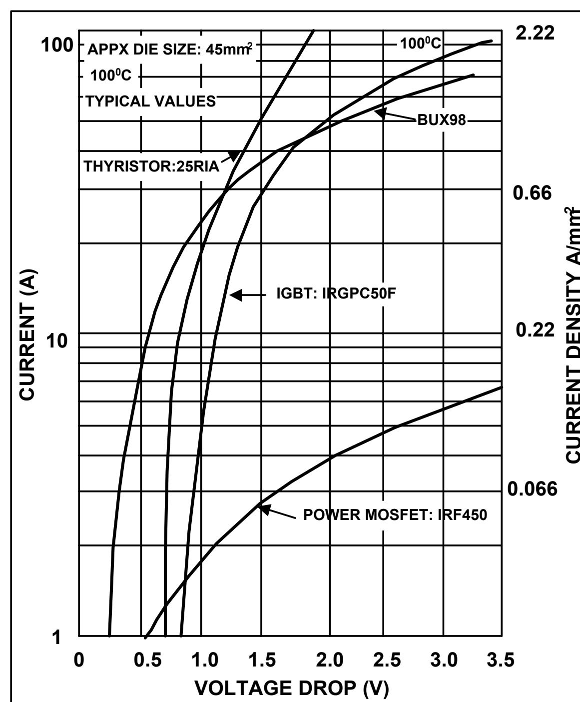

Figure 8. Conduction characteristics for devices of similar die size implemented in different technologies.

results that are specifically tailored to a given application. This figure shows in a clear and concise way to what extent higher switching frequencies impact the current output of the pair.

It also provides a simple way of selecting the optimum device for the application, which is the one that gives the highest output current at the specific operating frequency.

Once the thermal constraints are properly factored into the operating conditions, the graph carries important application information. In a motor control, the RMS component of the fundamental is directly related to torque. In a power supply, on the other hand, the total RMS content of the square wave contributes to power. The ratio between the two is 1.11.

The graph shown in Figure 9 can be generated with a relatively simple test circuit or with device models and analytical tools. It is present in most data sheets as Figure 1.

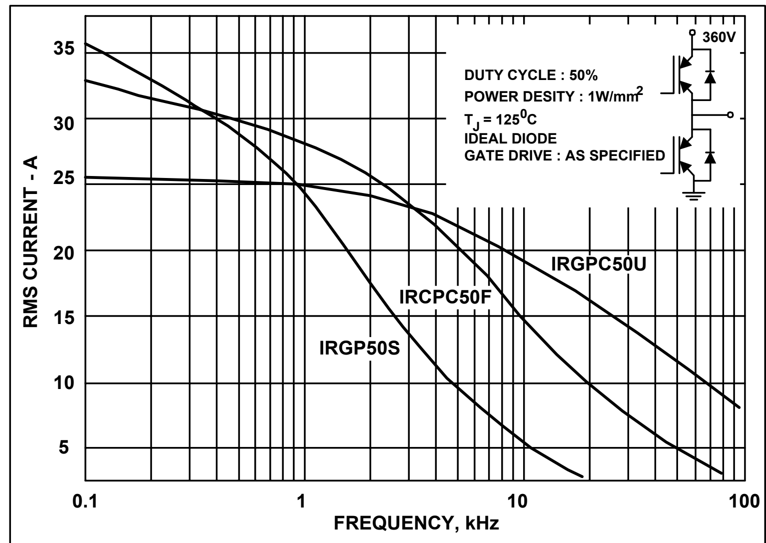

Figure 9. RMS current vs. frequency for a Half Bridge with two IGBTs of same die size, same package, different speed, operated in the conditions indicated in the inset.

VI. THERMAL DESIGN

IGBTs, like power MOSFETs and thyristors, are thermally limited. Hence, a good thermal design is the key to their cost effective utilization. When the objective of the thermal design is just the selection of the heatsink to keep the junction at, or below, a given temperature, the following expression provides the answer.

$$R_{\theta S-A} = \frac{\Delta T}{P_D} - R_{\theta J-C} - R_{\theta C-S}$$

ΔT is the temperature rise from ambient to junction. The power dissipation can be calculated as indicated in the previous chapter.

In general, the objective of the thermal design is the selection of the best device-heatsink combination. This may require a number of calculations. The entire selection process would be speeded-up significantly with the help of simple device models plugged into an application-specific spreadsheet.

In order to obtain a thermal resistance case-to-sink that is close to the data sheet value, the mounting torque should be approximately the value specified in the data sheet. An excessive mounting torque causes the package to bow and may crack the die. An inadequate mounting torque, on the other hand, results in poor thermal performance.

The temperature rise due to pulses of short duration can be calculated with the transient thermal response curve in the data sheet. The section "Peak Current Rating" in AN-949 describes the procedure in detail (http://www.irf.com/technical-info/appnotes/an-949.pdf).

For short pulses (5ms or less) the temperature rise calculated with the transient thermal response curve tends to be too conservative. A more accurate method to calculate temperature rise requires a FEA tools.

VII. REPLACING MOSFETS WITH IGBTS

The new generation of IGBTs has switching characteristics that are very close to those of power MOSFETs, without sacrificing the superior conduction characteristics of IGBTs. They offer advantages over MOSFETs in high voltage, hard-switching

applications. These advantages include lower conduction losses and smaller die area for the same output power. The smaller die area results in lower input capacitance, simpler gate drive and lower cost. Because the package style and the pinout of MOSFETs and IGBTs are identical, no mechanical or layout changes are required.

The gate drive requirement for IGBTs is similar to MOSFETs. A gate voltage between 12V and 15V is sufficient for turn-on, and no negative voltage required at turn-off. The value of the series gate resistor may have to be increased to avoid ringing at the gate of IGBT due to the lower input capacitances.

In high voltage MOSFETs, the power dissipation is mostly due to conduction losses; the switching losses being negligible up to 50kHz. On the other hand, the conduction losses in the IGBT are less than in the MOSFET, but the switching losses become significant above 10kHz. The following design example illustrates the point.

Switched DC Current	=	7.5A
Duty cycle	=	0.5
Bus voltage	=	310V
Junction temperature	=	125°C
MOSFET used	=	IRFP450
$R_{DS(on)}$ (25 °C)	=	0.4Ω
Operating frequency	=	50kHz
Current waveform	=	square wave

The on-resistance of the IRFP450 MOSFET at 125°C is (from the data sheet):

$R_{DS(on)}(125°C) = 0.816\Omega.$

The conduction loss in the MOSFET at 125°C:

$P_D = R_{DS(On)}(125°C) * I^2 * D = 23W$

Assuming 75ns switching times and 50kHz switching frequency, the switching losses in the MOSFET at 7.5A are approximately:

$P_{SW} = 6.5\ W$

The total power loss in the MOSFET is:

$P_{tot} = 29.5W$

Replacing the MOSFET with a IRGP430U IGBT, the conduction loss in the IGBT is:

$P_c = V_{CE}(125°C) * I_c * D$

The on-state collector-emitter voltage at 125°C and 7.5 A is from Figure 5 on the data sheet:

$V_{CE\ @\ 125°C} = 2.03V.$

The conduction loss in the IGBT is:

$P_c = 2.03V * 7.5A * 0.5 = 7.62W$

Due to the IGBTs higher usable current density, the same power dissipation in the IGBT and MOSFET results higher junction temperature for the IGBT because of higher junction to case thermal resistance.

To maintain the junction temperature parity, the power dissipation in the IGBT needs to be reduced to:

$P_{DIGBT} = P_D * (R_{\theta SA} + R_{\theta CSM} + R_{\theta JCM}) / (R_{\theta SA} + R_{\theta SI} + R_{\theta JCI})$

Where:

$R_{\theta SA}$ Heatsink to ambient thermal resistance.
$R_{\theta CSM}$ MOSFET case to sink thermal resistance.
$R_{\theta JCM}$ MOSFET junction to case thermal resistance.
$R_{\theta SI}$ IGBT case to sink thermal resistance.
$R_{\theta JCI}$ IGBT, junction to case thermal resistance.

The total power dissipation is composed of both conduction and switching losses. Conduction losses were calculated above. Using the formula above yields $P_{DIGBT} = 23.2W$.

The maximum allowable power loss due to switching losses:

$$P_{SW} = P_{TOT} - P_{COND}$$
$$P_{SW} = 23.2W - 7.6W = 15.6W$$

The maximum switching frequency for same junction temperature in same thermal environment:

$$f_{max} = 10.3W/0.226mJ = 56.4kHz$$

The switching energy number comes from data sheet information. It will be appreciated that, being operated with lower losses, the IGBT design is more efficient.
The sources of power dissipation in the IRFP450 MOSFET and IRGP430U IGBT are shown in Figure 10.

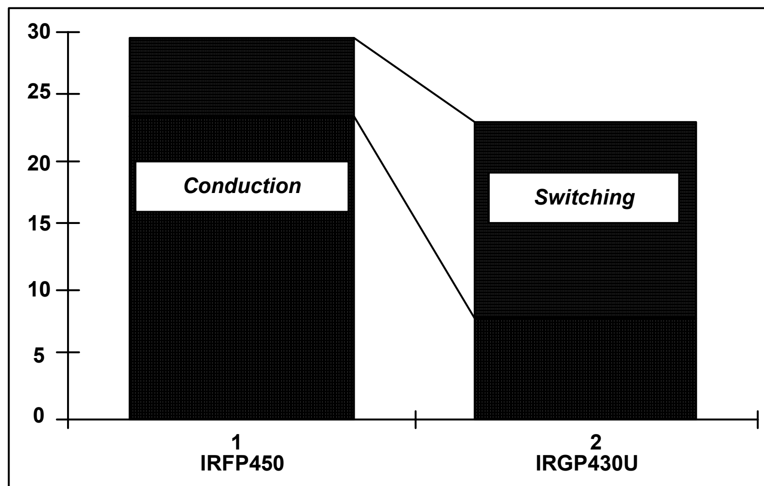

Figure 10. Power losses in an IRGPC450 MOSFET and a IRGP430U IGBT at 7.5A current both switching at 50kHz.

The smaller die size and input capacitance of the IGBT may result in faster switching speed than the MOSFET replaced. A larger value gate resistor slows down the turn-on speed, but has little effect on turn-off. Unlike the MOSFET, the turn-off speed of the IGBT cannot be controlled with the series gate resistor.

In applications where the body diode of the MOSFET is used, IGBT-diode co-packs improve performance and efficiency, while reducing current spikes. This is due to better diode performance.

VIII. GUIDELINES ON PARALLELING

Whenever devices are operated in parallel, due consideration should be given to the sharing between devices to ensure that the individual units are operated within their limits. To operate IGBTs in parallel, the following factors should be considered: gate circuitry, layout considerations, current unbalance, and temperature unbalance between devices.

Paralleling helps to reduce conduction losses and junction to case thermal resistance. However, switching losses remain the same, or may even increase. If they are the dominant losses, only a thermal resistance improvement will be achieved by paralleling. Experimental results should be obtained at the extremes of the manufacturing tolerances.

Power MOSFETs parallel relatively well due to their positive temperature coefficient. The IGBT, being a combination of a power MOSFET and BJT, cannot be simply described as having either a negative or positive temperature coefficient. The temperature coefficient is dependent on the technology used in the IGBT design; even within the same technology, it changes with current density.

The three most important parameters from this point of view are: voltage, current and junction temperature. The effects of current and temperature unbalances will be analyzed in detail in the following sections, while voltage unbalances will be briefly examined in a qualitative way in the next section.

A. General paralleling guidelines

Generally speaking, voltage equality is ensured by the fact that the devices are in parallel. However, under transient conditions, voltage differentials can appear across devices, due to di/dt effects in unequalized stray inductances.

The stray inductances of a typical power circuit, like the one shown in Figure 11, have different effects, depending on where they are situated.

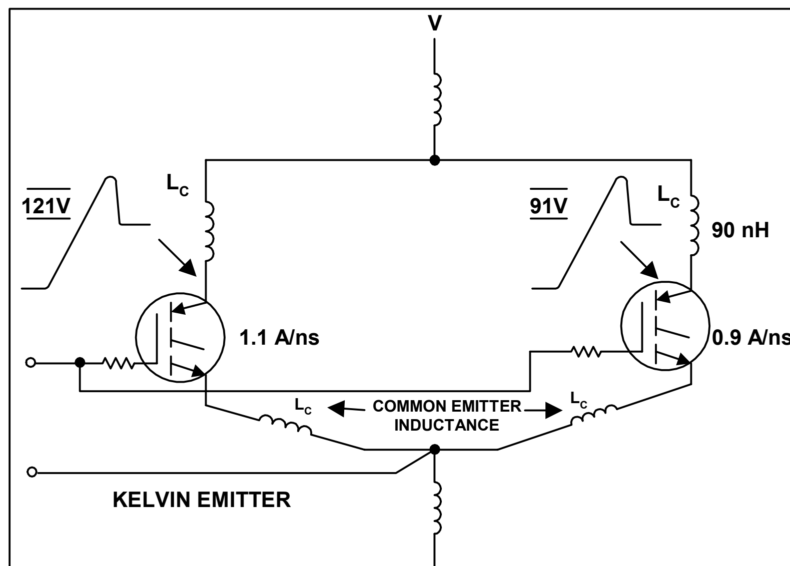

Figure 11. The effect of different di/dt and stray inductances on collector voltages.

An unbalance of 10% in the stray inductances that are in series with each collector, combined with a di/dt unbalance of 10% translates in an unbalance of 20% in the overshoot seen at turn-off (81 vs. 121V). To minimize these differentials both di/dt's and stray inductances have to be matched. However, if the overshoot does not violate the ratings of the IGBT, the differential in the turn-off losses may be negligible.

The impact of the common emitter inductance on switching energy, on the other hand, is far from negligible, as explained in Section I C. Furthermore, the IGBT with lower common source inductance turns off before the other, which is left to shoulder the entire load current during the turn-off transient, as described in AN-941 (http://www.irf.com/technical-info/appnotes/an-941.pdf). It follows that Switchmode operation of paralleled IGBTs should not be undertaken unless the common emitter inductances are matched in value.

Finally, like power MOSFETs, parasitic oscillation have been observed on paralleled IGBTs without individual gate resistors. It is assumed that the cause for this oscillation is the same as that reported in AN-941.

In summary, the following general guidelines should be followed when paralleling IGBTs:

- Use individual gate resistors to eliminate the risk of parasitic oscillation;
- Equalize common emitter inductance and reduce it to a value that does not greatly impact the total switching losses at the frequency of operation;
- Reduce stray inductance to values that give acceptable overshoots at the maximum operating current.
- Ensure that the gate of the IGBT is looking into a stiff (voltage) source with as little impedance as practical..
- Zener diodes in gate drive circuits may cause oscillations. Do not place them directly gate to emitter/source to control gate overvoltage, instead place them on the driver side of the gate isolation resistor(s), if required.
- Gate-to-source capacitors are frequently used to reduce dv/dt induced turn-on. However, they may cause oscillations when IGBTs are paralleled. Capacitors slow down switching, thereby increasing the switching unbalance between devices.

Stray components are minimized by a tight layout and equalized by symmetrical position of components and routing of connections.

These guidelines ensure that the voltage and switching unbalances due to the layout are negligible with respect to those due to the IGBTs themselves, analyzed in the next section.

B. Current and temperature unbalance

In this section we will examine the steady state conduction and temperature unbalance due to the IGBTs themselves and the effects of frequency and duty cycle. When paralleling power semiconductors, the first issue that comes to mind is how well they share the total current. This disregards the fact that semiconductors are more sensitive to temperature than to current, so the real issue is how close are their junction temperatures and whether or not one of the devices approaches the rated junction temperature. This should be of primary concern to the designer, as junction temperature directly correlates to reliability,

Given two different IGBTs, their respective $V_{CE(on)}$ at any given current will be slightly different. When these two IGBTs are operated in parallel, the $V_{CE(on)}$ across both devices is forced to be the same.

Thus, for a given load current, one IGBT will carry more current than the other, resulting in a current unbalance. As long as the current remains below the maximum specified on the data sheet, current unbalance is not critically important. At low currents, it can be 75-100%. Since the voltage drop is the same for both IGBTs, the device that carries more current has a higher junction temperature.

Current unbalance may not be affected significantly by thermal coupling. This is shown in the figures in the following section depicting current unbalance for IGBTs mounted on both separate and common heat sinks. However, the more important criteria, temperature unbalance, is affected significantly. In fact, the figures in the following section show that the maximum current is limited by the hotter device exceeding the stipulated maximum junction temperature of 150°.

The complexity of the algebraic equations does not allow a direct, closed form solution of general applicability. However, with suitable analytical work, we can establish the operating conditions of two paralleled IGBTs in a given application environment. The results, although specific to the application, provide a useful insight into the factors that come into play and their respective effects.

B.1. Selection Criteria for the IGBTs

As far as this analysis goes, two IGBTs (IRGPC50U) have been selected from a population of 15 devices from three different lots. The two IGBTs were at the two extremes of the distribution of voltage drop, one being the highest (IGBT 1), the other being the lowest (IGBT 2). Temperature and current were not a factor since both IGBTs remained, respectively, the highest and the lowest throughout the temperature and current range.

Conduction and switching models were generated for both IGBTs, together with the average parameters for the entire population. Thus, the analysis carried out in the following sections is based on two extreme but real IGBTs, chosen from a given population. As it should be expected, the IGBT with better conduction characteristics has worse switching characteristics.

From that same population we could have constructed the model for two fictitious IGBTs with extreme conduction ***and*** switching behavior. This, however, would have been at odds with the fundamental trade-off between conduction and switching characteristics, typical of the device itself.

B.2. The Thermal System

The heat generated by the two IGBTs is transmitted to a sink and, ultimately, to the ambient. Two cases will be examined: common and separate heatsinks (Figure 12).

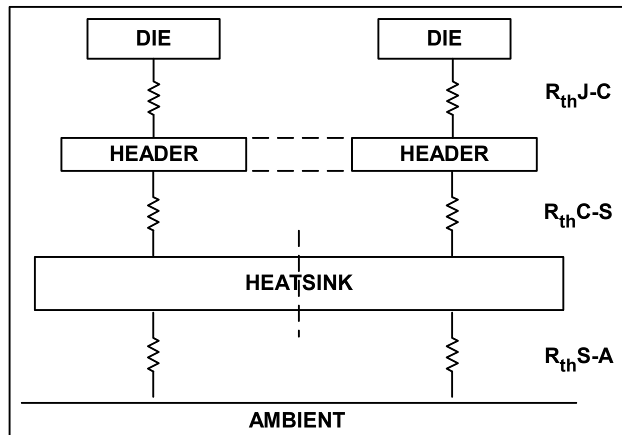

Figure 12. The characteristics of the thermal system of the paralled IGBTs.

A common heatsink establishes a thermal coupling between the two dice that limits their temperature differential. As it will be seen later, if the thermal coupling is tight, as with dice mounted on the same substrate, the temperature differential is in the order of few degrees.

B.3. Steady State Operating Conditions

Being in parallel, the voltage drop across the IGBTs is the same. Hence, the IGBT with better conduction characteristics carries a larger share of the load current to make its voltage drop the same as the other. Its power dissipation and junction temperature are higher by an amount that depends on the thermal design, as shown in Figure 13.

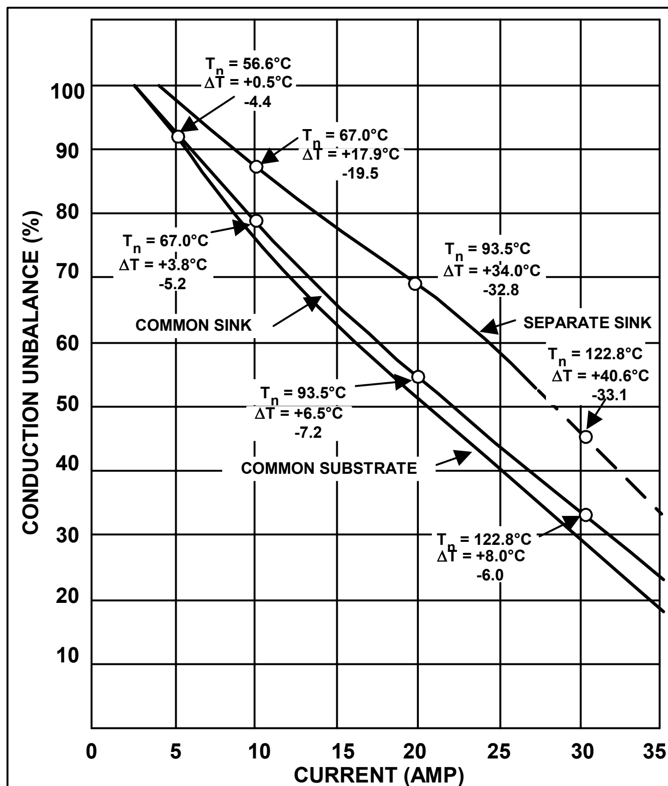

Figure 13. Conduction unbalance for two paralleled IGBTs as a function of current for three different thermal designs.

For low currents the conduction unbalance can be as high as 100%, i.e. one IGBT takes the entire current, operating, however, well within its limits. As the load current increases the current unbalance decreases and, as long as the IGBTs are mounted on a common heatsink, the two temperatures stay within ±10°C. The use of separate heatsinks causes large current unbalances and very significant temperature differentials.

The first factor that keeps the unbalance in check is the thermal feedback between the two junctions. The one with higher power dissipation increases the sink temperature and, consequently, the junction temperature of the other, by an amount that is inversely proportional to the thermal resistance between the junctions.

If the thermal coupling between dice is tight, the temperature differential cannot be significant. The other factor that reduces the current unbalance is the temperature coefficient of the voltage drop. Although they are both negative, the IGBT with lower voltage drop has a lower temperature coefficient. As current and temperature increase, its voltage drop changes little, while the voltage drop of the IGBT that was carrying little current comes down significantly, thereby closing the gap in current, as well as temperature.

There is a third balancing mechanism: as collector current increases, the voltage drop of the two IGBTs converge toward the average of the distribution. This intrinsically reduces the unbalance at higher currents.

B.4. The Effect of Frequency and Duty Cycle

In a practical application the two IGBTs would be operated at some frequency and the losses in both devices would have a switching component.

The IGBT that carries more current will also be switching a higher current. Hence, it has higher conduction, as well as higher switching losses. This unbalance in losses is further compounded by the fact that, as we have mentioned previously, this same IGBT exhibits a worse switching behavior, which further increases its switching losses.

Thus, it would appear that a regenerative process is in place that will quickly take the junction temperature of the IGBT with lower conduction losses beyond its rated limits and that this regenerative process is accelerated by the operating frequency. In practice this does not happen and frequency helps bring about balanced operation, as we are about to see.

Curves of current and temperature unbalance have been generated for the popular "half-bridge" circuit, as shown in Figure 14a. From these curves we observe the following:

1. As the frequency increases the current unbalance decreases. The rate of decrease increases with frequency.

2. As the current increases the amount of unbalance decreases. This result is consistent with the observations made when analyzing steady state operation.

3. As the frequency increases the temperature differential first increases, then it decreases rapidly.

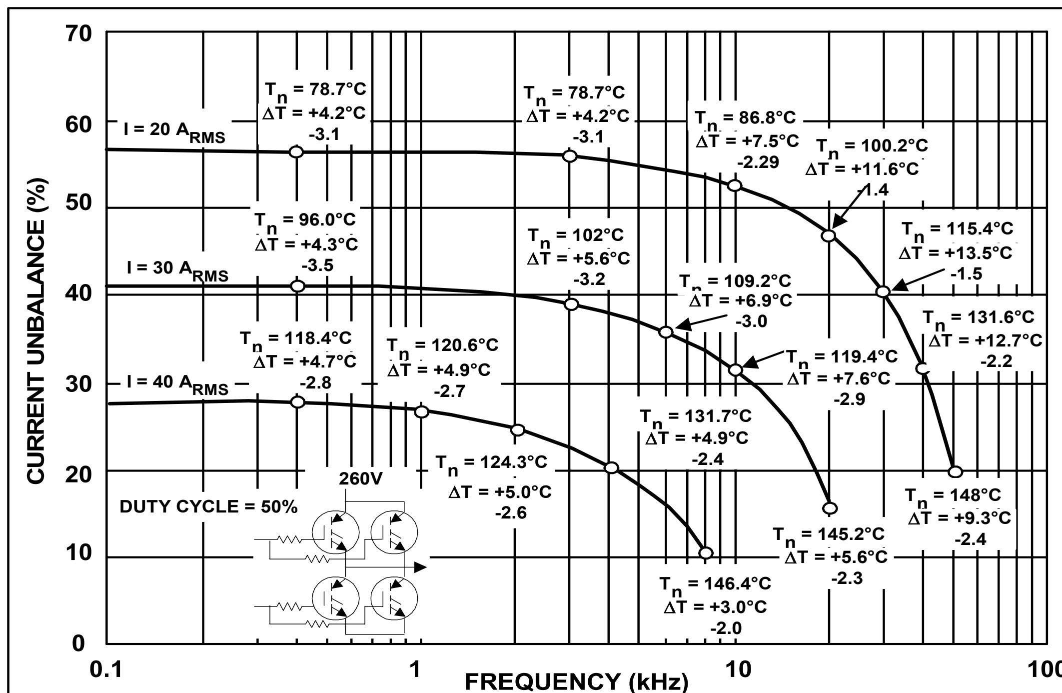

Figure 14a. Duty cycle at 50%

The key balancing mechanism in this, as in the steady state mode of operation, is the different temperature coefficients of the voltage drop. As we have seen in the previous section, an increase in current causes an increase in temperature which, in turn, causes a reduction in voltage drop that is larger for the IGBT with a higher voltage drop. Hence, an increase in temperature results in a reduction in current unbalance.

Switching losses increase junction temperature of both IGBTs and contribute to a reduction of the current unbalance. However, the increase in temperature is higher for the IGBT which carries the higher current, on account of its higher conduction and switching losses. This delays the balancing mechanism and causes the increase in temperature differential noticeable in Figure 21 between 10 and 30 kHz ($I = 20A_{RMS}$). The thermal coupling and the difference in temperature coefficients gradually cause a reduction in the current unbalance.

This, in turn, reduces conduction and switching losses in the IGBT that was carrying more current, thereby bringing about a more balanced operating condition at an exponential rate. For the specific IGBTs we have modeled the point of current balance occurs at a temperature that is somewhat higher than 150°C.

Operation at lower duty cycles is not significantly different from what we have just described (Figure 14b), except that the current unbalance for a given output current is lower.

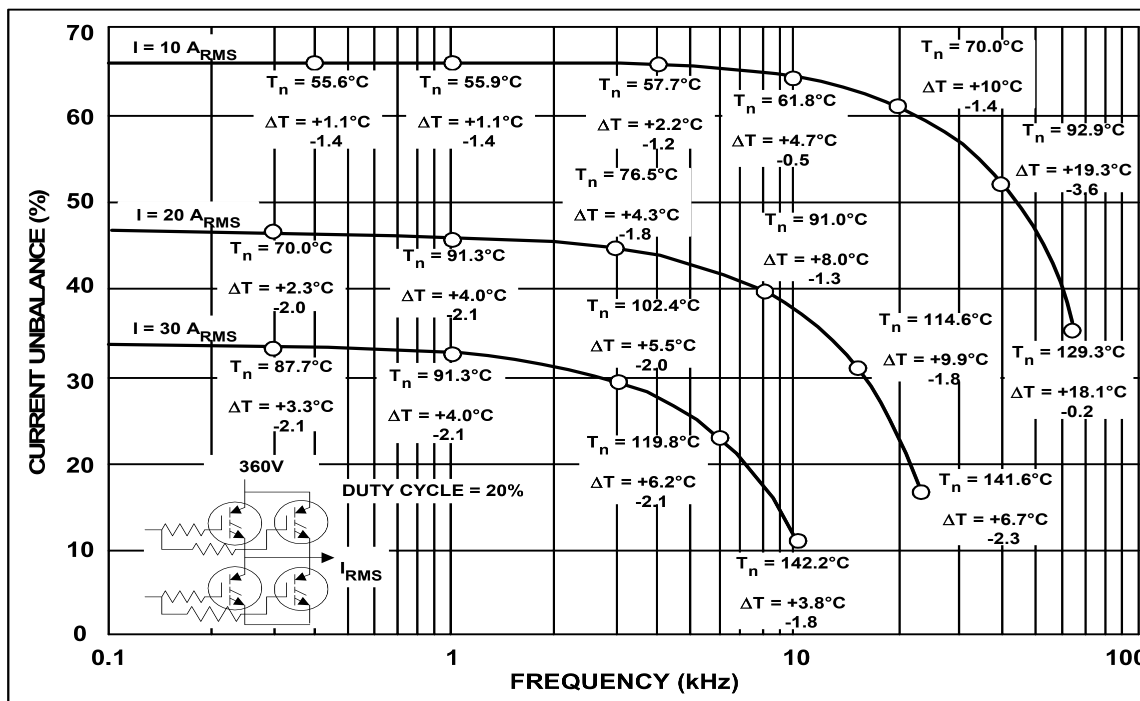

Figure 14b. Current and temperature unbalance as a function of frequency of two IGBTs operated in parallel.

This is due to the third balancing mechanism, whereby the voltage drops converge at higher currents. To generate the same output current with a lower duty cycle a higher peak current is necessary, with intrinsically better current sharing.

One additional unbalancing element, disregarded in the foregoing analysis is the fact that, with a clamped inductive load, the IGBT that goes off last ends up carrying the entire load current. This turn-off unbalance can be disregarded only to the extent that the turn-off times of the devices is short compared to the individual stray inductances, which tends to reduce this source of unbalance.

C. Conclusions

Although the analysis presented in the previous sections is limited to one specific type of IGBTs in a specific operating mode, the results have been found to be equally applicable to the other families of IGBTs available from International Rectifier at the time of writing. They can he summarized as follows:

1. Paralleled IGBTs will operate with a current unbalance that, in a practical application, can be as high as 50 to 70% at low currents. Temperature unbalance, on the other hand, is generally less than 10°C, provided they are on the same heatsink.

2. Three balancing mechanisms tend to reduce the current unbalance:

   * thermal feedback;
   * different temperature coefficients of the voltage drop;
   * converging voltage drop characteristics at higher currents.

3. The tighter the thermal coupling, the lower the unbalance. Operation of paralleled IGBTs on separate heatsinks should be avoided.

4. An increase in junction temperature reduces the unbalance, on account of the different temperature coefficients of the voltage drop. An increase in frequency has the same effect, for the same reason.

5. An increase in current reduces the unbalance, due to converging dynamic resistances. It would also cause an increase in temperature and, consequently, a further reduction in unbalance.

6. For a given output current, a decrease in duty cycle causes an increase in peak current, hence a reduction in unbalance.

IX. SCREENING OF IGBTS FOR PARALLELING

Device selection is an effective method to reduce derating that would normally be required when paralleling IGBTs to ensure that they are operated within data sheet limits. Matching $V_{CE(on)}$ and $V_{G(th)}$ is commonly done. An alternative way is to connect the IGBT in "diode mode", i.e. with the gate connected to the collector as shown in Figure 15. The selection criterion is the voltage across each IGBT at a meaningful current level. This measurement must be done in pulse mode to avoid device self-heating. The voltage required for this amount of current is recorded. This measurement not only takes into account variations in $V_{CE(on)}$, but also threshold and transconductance. Which one of the two screening method is more effective depends on the IGBT technology and speed. Here we report one instance of $V_{CE(on)}$ screening performed on a particular family of IGBTs.

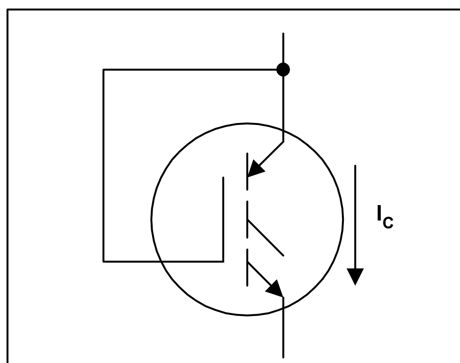

Figure 15. Connection for Measuring "Diode Mode" Voltage, V diode

Five devices from each lot, using three lots, were examined and ranked in order of conduction voltage. This information was used to obtain the operating point of each IGBT in parallel operation.

Figure 16 depicts the percent current unbalance at different current levels for the two IRGPC50Us at both ends of the spectrum: lowest and highest $V_{CE(on)}$s of the entire population of 15 devices from three lots. The $\Delta V_{CE(on)}$ for these was 0.55 volts measured at 30 amps. The operating conditions were: two devices mounted on a common heat sink with an $R_{\theta SA}$ of 2°C/W with an ambient temperature of 45°C.

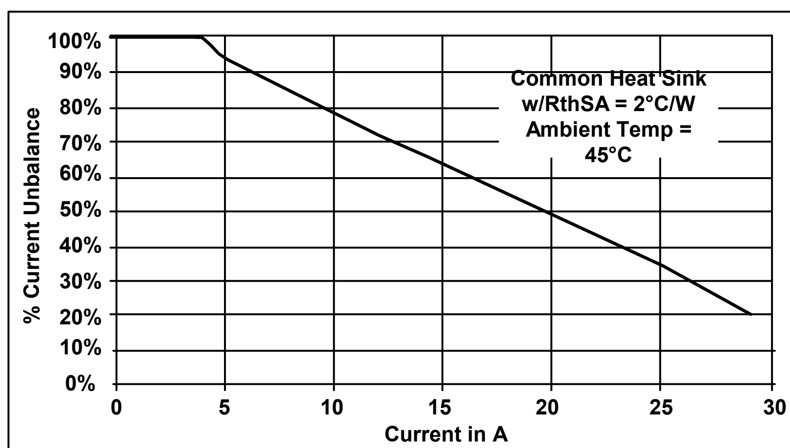

Figure 16. Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.55V

As it is apparent from Figure 16, the current unbalance can be as high as 100%. This means that the entire current flows in one device. This may appear to be unacceptable except that the total amount of current is very low and definitely within the capability of a single device. Also, as discussed in the previous section, the more important factor is the junction temperature, which is

shown in Figure 17. The upper curve in Figure 17 is for the same operating conditions as Figure 16 (extreme devices), while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$ is zero). For any current the penalty resulting from totally mismatched devices is only a few degrees Celsius. This is true if, and only if, the devices are mounted on the same sink in a tight thermal coupling (no insulation).

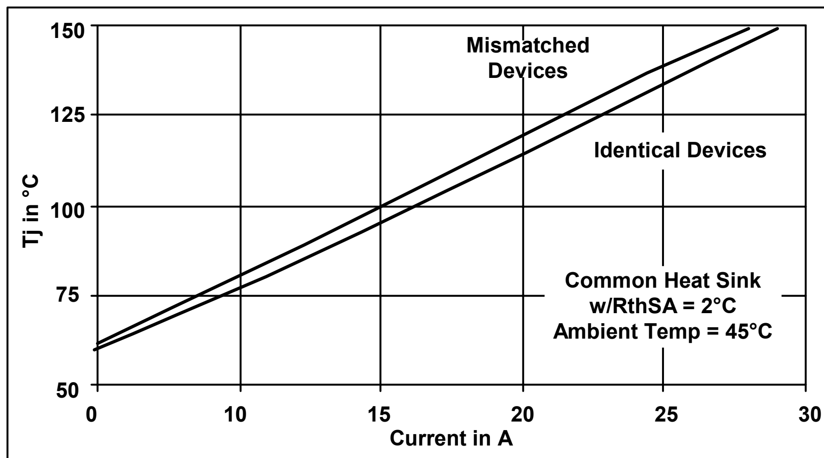

Figure 17. Junction Temperature versus Total Current, IRGPC50U with ΔVCE(on) = 0.55V

To compare closer matched devices, the same measurements were repeated using two devices with a $\Delta V_{CE(on)}$ = 0.36V in the same operating conditions. Figure 18 and 19 show the corresponding results. Notice how the current unbalance has decreased significantly with respect to what is shown in Figure 16 for a $\Delta V_{CE(on)}$=0.55V.

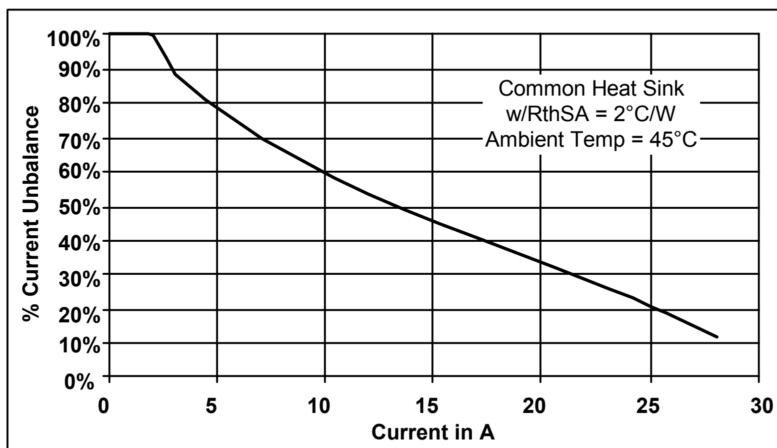

Figure 18. Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

Figure 19 shows the junction temperature versus current. The upper curve in Figure 19 is for the devices in Figure 18, while the lower curve is for two identical devices (i.e., $\Delta V_{CE(on)}$ is zero). Comparing this with the temperature unbalance shown in Figure 17 it will be noticed that the unbalance has reduced further from an already small value.

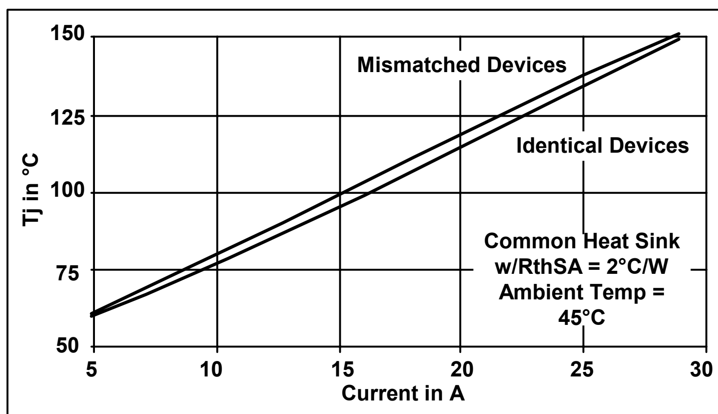

Figure 19. Junction Temperate versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

Figure 20 shows the higher of the two junction temperatures for the parallel combination of several different pairs of IRGPC50Us with increasing $\Delta V_{CE(on)}$s. This graph shows that screening is of marginal value compared with a tight thermal feedback obtained by mounting the paralleled IGBTs on the same sink or substrate, without interface material.

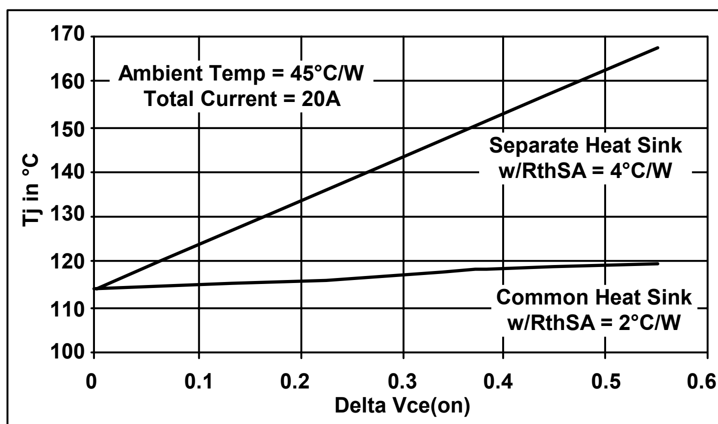

Figure 20. Junction Temperature versus ΔVCE(on), for IRGPC50Us

The final graph, Figure 21, depicts the RMS current versus switching frequency for a parallel pair of IRGPC50Us operated in a typical half-bridge configuration with 50% fixed duty cycle. The devices are mounted on a common heat sink with a thermal resistance of 2°C/W with an ambient temperature of 45°C. Neither IGBT is allowed to exceed a junction temperature of 125°C. The upper curve is for identical devices, the next curve is for the devices characterized in Figures 16 and 17 ($\Delta V_{CE(on)}$=0.55V), while the lower curve is for the devices described in Figures 18 and 19 ($\Delta V_{CE(on)}$=0.36V).

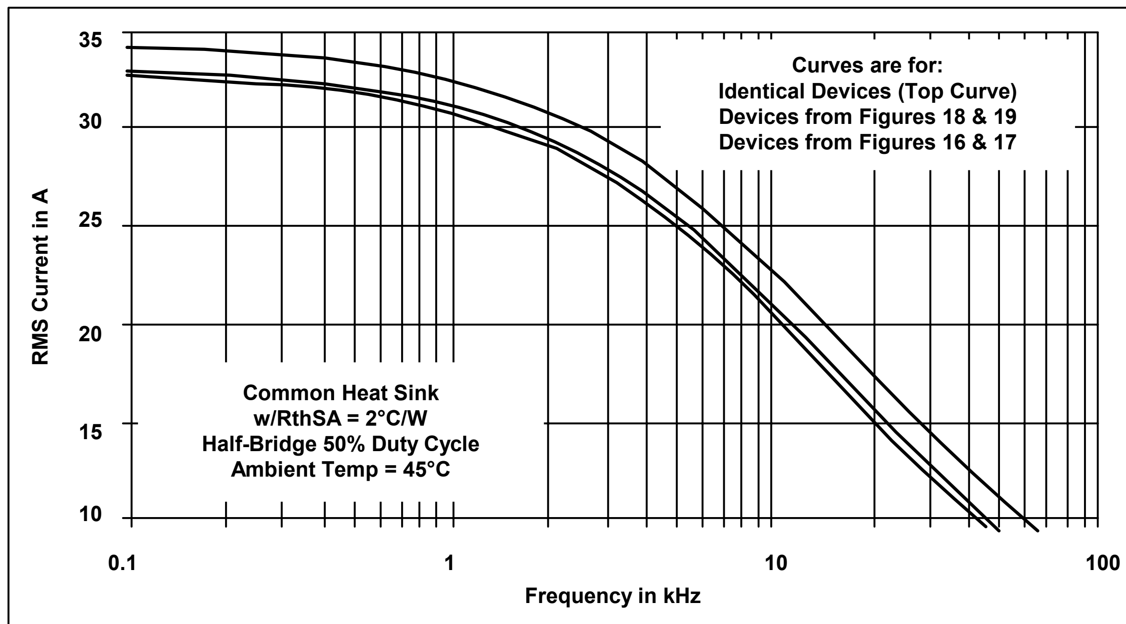

Figure 21. Current versus Frequency Graph for Three Pairs of IRGPC50Us with ΔVdiode = 0.00, 0.36, & 0.55V

The previous discussions have been limited to two paralleled devices, the only case that can be treated with simple analytical tools. This does not limit the generality of the conclusions, however, as in any group of paralleled devices, there will be two with extreme voltage drops. As explained in Section IX.B.1., these two are also likely to have extreme switching characteristics. The selection criteria, would apply to these two extreme devices, with all others falling in between.

References:

[1] Switching Waveforms of the L^2FET, by C.F. Wheatley and H.R. Ronan IEEE Transactions on Power Electronics. April 1987 p. 81

[2] Analysis and characterization of power MOSFET switching performance, by S.M. Clemente, A. Isidori, B.R. Pelly. Proceedings of Powercon 8, 1981, H2.