Transient Suppression Techniques for *TOPSwitch*® Power Supplies

Application Note AN-20

Introduction

AC power mains occasionally have transient surge voltages. Lightning strikes and AC mains load switching are just two examples of many possible conditions causing transient voltages. Consequently, all off-line power supplies must provide some level of protection to suppress the effects of such transient voltages.

This application note presents design techniques which improve *TOPSwitch* power supply operation through most AC mains transient surge voltages. Properly designed transformers, PC boards, and EMI filters not only suppress the effects from transient voltages but also reduce both conducted and radiated EMI emissions as well. These techniques can also be used in applications with DC input voltages such as Telecom and Television Cable Communication (or Cablecom).

The ST202A Reference Design Board using the TOP202YAI *TOPSwitch* will be used as an example throughout this application note. Refer to the ST202A data sheet as well as AN-14 and AN-15 for additional information.

Typical Transient Test Voltages

Figure 1 shows a typical surge voltage waveform specified by IEC 1000-4-5 (formerly IEC 801-4-5). Peak test voltages (U) of 3kV are common but in some applications higher peak voltages are specified. The surge voltage waveform has a 1.2µS front time T_1 and 50µS time to half value T_2 as shown.

Figure 2 shows a typical ring wave voltage waveform specified by IEEE-587. Peak test voltages (V_{peak}) of 3kV are common but in some applications higher voltages are specified. The open circuit ring wave voltage waveform has a 0.5µS rise time to 90% of peak value and exponentially decays while oscillating at 100 kHz with each peak being 60% of the preceding peak.

The transient test voltage may be applied both in common mode and differential mode configurations. The common mode configuration shown in Figure 3 applies the transient test voltage first to one AC mains conductor and then the other with respect to earth ground. The *TOPSwitch* power supply output should be connected either directly to earth ground or AC coupled through a capacitor to earth ground. This transient test voltage causes high peak transient ringing currents to flow between the *TOPSwitch* power supply primary and secondary. Without proper attention to EMI filter design, transformer design, and PC layout design, transient currents couple into signal traces and generate voltage spikes capable of setting the *TOPSwitch* shutdown latch.

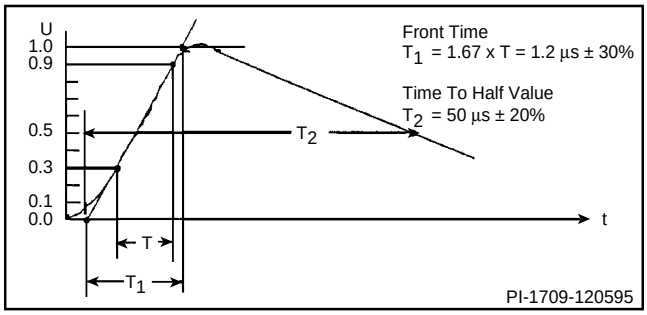

Figure 1. Waveshape of Open Circuit Voltage (1.2/50 µS) From IEC-1000-4-5.

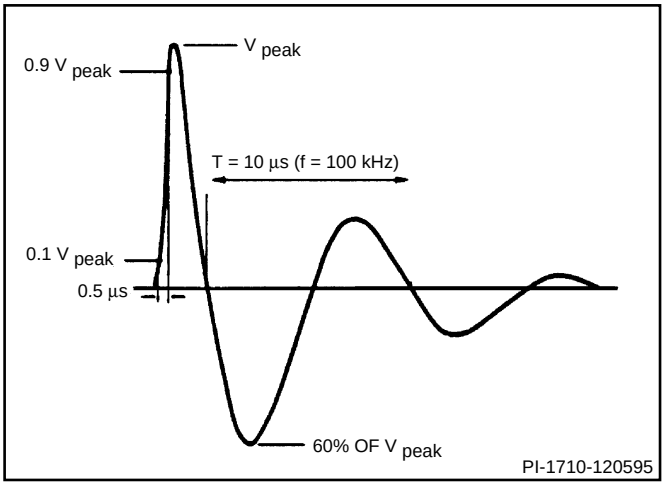

Figure 2. 0.5 µs-100 kHz Ring Wave (Open-Circuit Voltage) From IEEE-587.

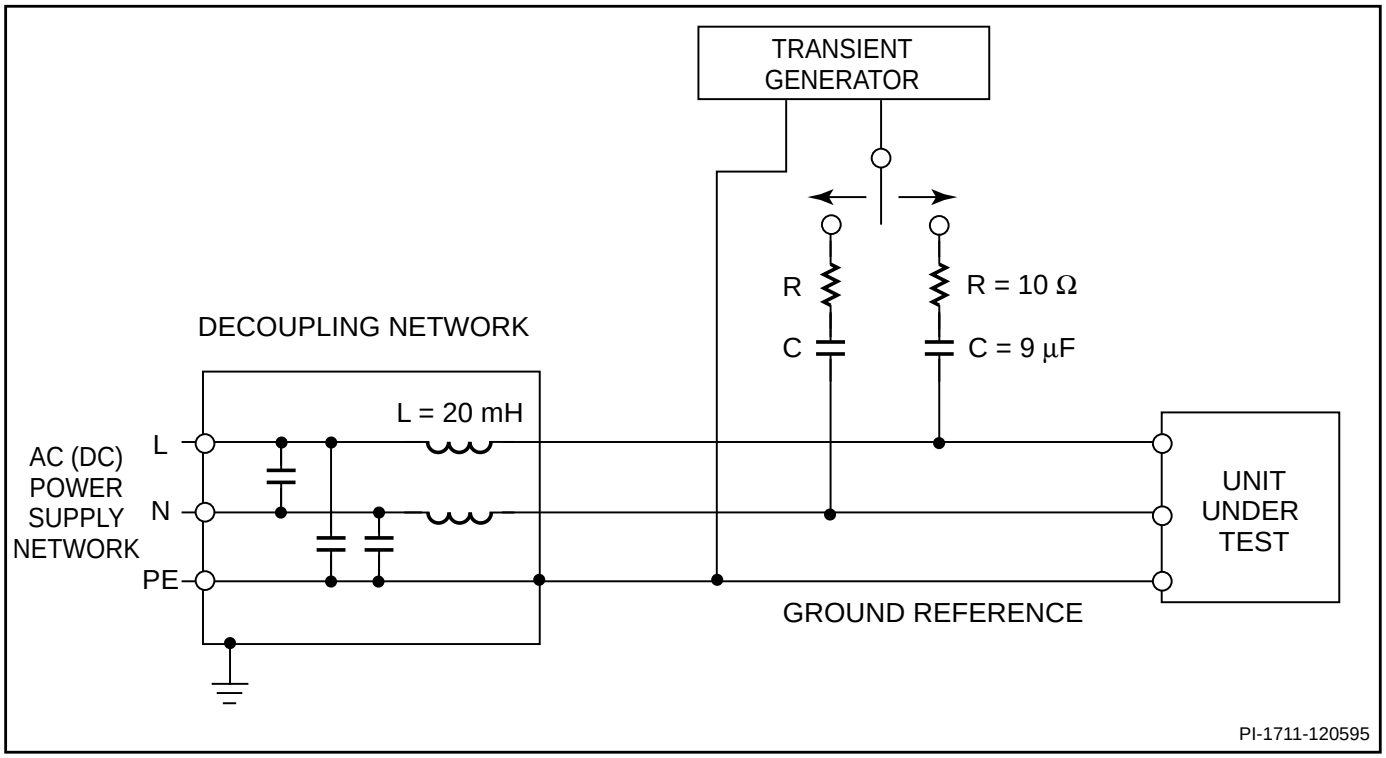

Figure 3. Typical Test Set-Up for Capacitive Coupling on AC Lines; Common Mode or Line to Ground Coupling.

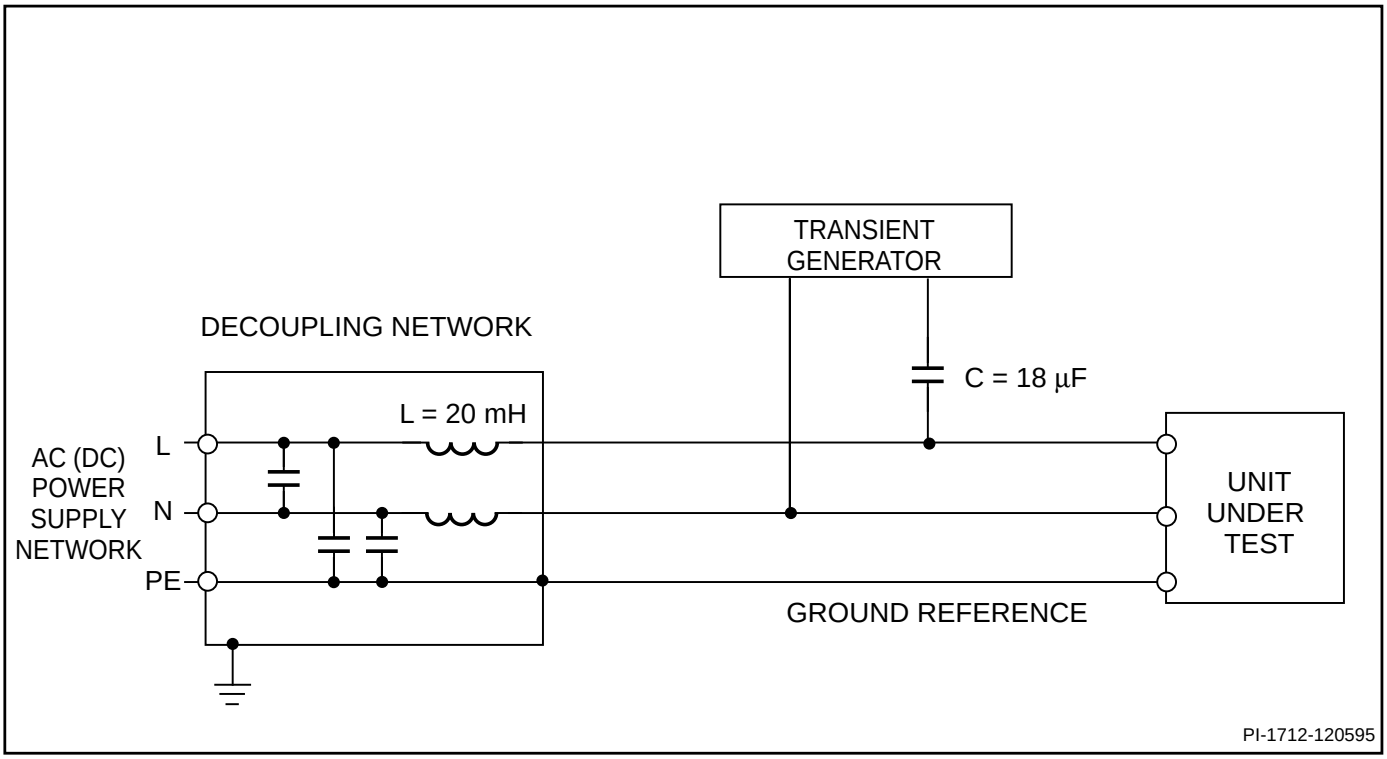

Figure 4. Typical Test Set-up for Capacitive Coupling on AC Lines; Differential Mode or Line to Line Coupling.

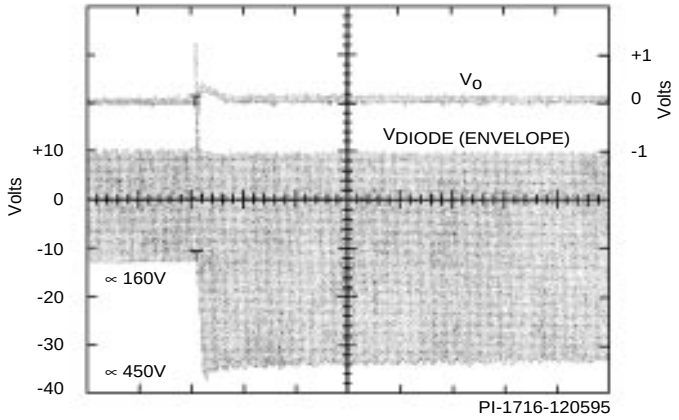

Figure 5. Output Voltage and Envelope of Diode Voltage Waveform During Normal Mode Transient Surge.

The differential mode configuration shown in Figure 4 applies the transient test voltage across both AC mains conductors. The *TOPSwitch* power supply output should be connected either directly to earth ground or AC coupled through a capacitor to earth ground. This transient test voltage causes high differential mode transient currents which can overcharge the power supply bulk energy storage capacitor (C1 in Figure 7) or high voltage DC bus (V+) to a high value. During transient testing, directly measuring the V+ high voltage DC bus is dangerous and can lead to equipment damage. Fortunately, the V+ high voltage DC bus can be measured indirectly on the secondary side of the power supply. Figure 5 shows the ST202A power supply output voltage and the envelope of the output rectifier (D2 in Figure 7) anode voltage during a differential mode test. The anode voltage is useful because the envelope above reference is proportional to power supply output voltage V_O and the envelope below reference is proportional to the V+ high voltage DC bus. During the transient test, input capacitor C1 and the V+ high voltage DC bus is charged from 160 VDC up to 450 VDC but the *TOPSwitch* simply operates through with just a minor output voltage correction.

Some differential mode transient test voltages are capable of charging input capacitor C1 up to a voltage sufficient to cause the bridge rectifier diodes to enter avalanche breakdown which essentially clamps the high voltage DC bus (V+). Sometimes the fuse opens, sometimes the bridge rectifier fails and then the fuse opens. In the worst case scenario, the transient test voltage charges up input capacitor C1 to a sufficiently high DC bus voltage (V+) that *TOPSwitch* Drain voltage rating is exceeded.

Circuit Countermeasures

The following circuit countermeasures have been shown to improve *TOPSwitch* power supply operation under transient spike or surge voltage conditions. *TOPSwitch* ST202A power supplies have been demonstrated to successfully operate through both ring wave and 1.2µS/50µS surge voltages with peak voltages up to 3 kV with the following circuit modifications. All common mode countermeasures apply to differential mode transient test conditions as well.

Common Mode Countermeasures

Eliminate all PC Board arcing! Dim the lights and closely examine the PC board during testing for signs of arcing between PC traces or conductors. Change the PC layout temporarily with trace cuts and jumpers to increase the spacing and make permanent changes on the PC board artwork. Slots in the PC board can be used to increase effective clearance.

Replace common mode choke with wider bandwidth style. One example of a wide bandwidth common mode choke is shown in Figure 6. Note that each common mode inductor is wound in two series connected sections to reduce capacitance. Two section construction also divides or splits the transient test voltage to reduce voltage stress and prevent arcing between common mode choke windings. Use 10 mH to 33 mH common mode chokes such as the Panasonic ELF-18D290X series for output power under 20 Watts and ELF-18D2XX series for output power over 20 Watts. (Toroidal common mode chokes are not recommended.)

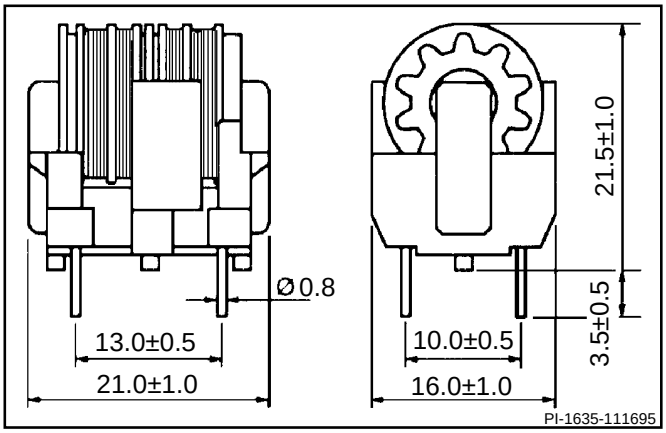

Figure 6. Spool Wound Common Mode Choke (Dimensions in mm).

Figure 7 shows a typical 2-wire input *TOPSwitch* ST202A power supply modified with Y2-safety capacitors C7, C8, and C11. The schematic is drawn to emphasize that C7, C8, and C11 should connect directly to the transformer pins. This capacitor connection keeps peak transient currents flowing through known paths and out of sensitive PC traces. Note that C11 connects to the high voltage DC bus (V+), C7 connects to the high voltage DC bus return (V-), and C8 connects directly to secondary return. C7, C8, and C11 must have very short leads and be connected with short, wide traces.

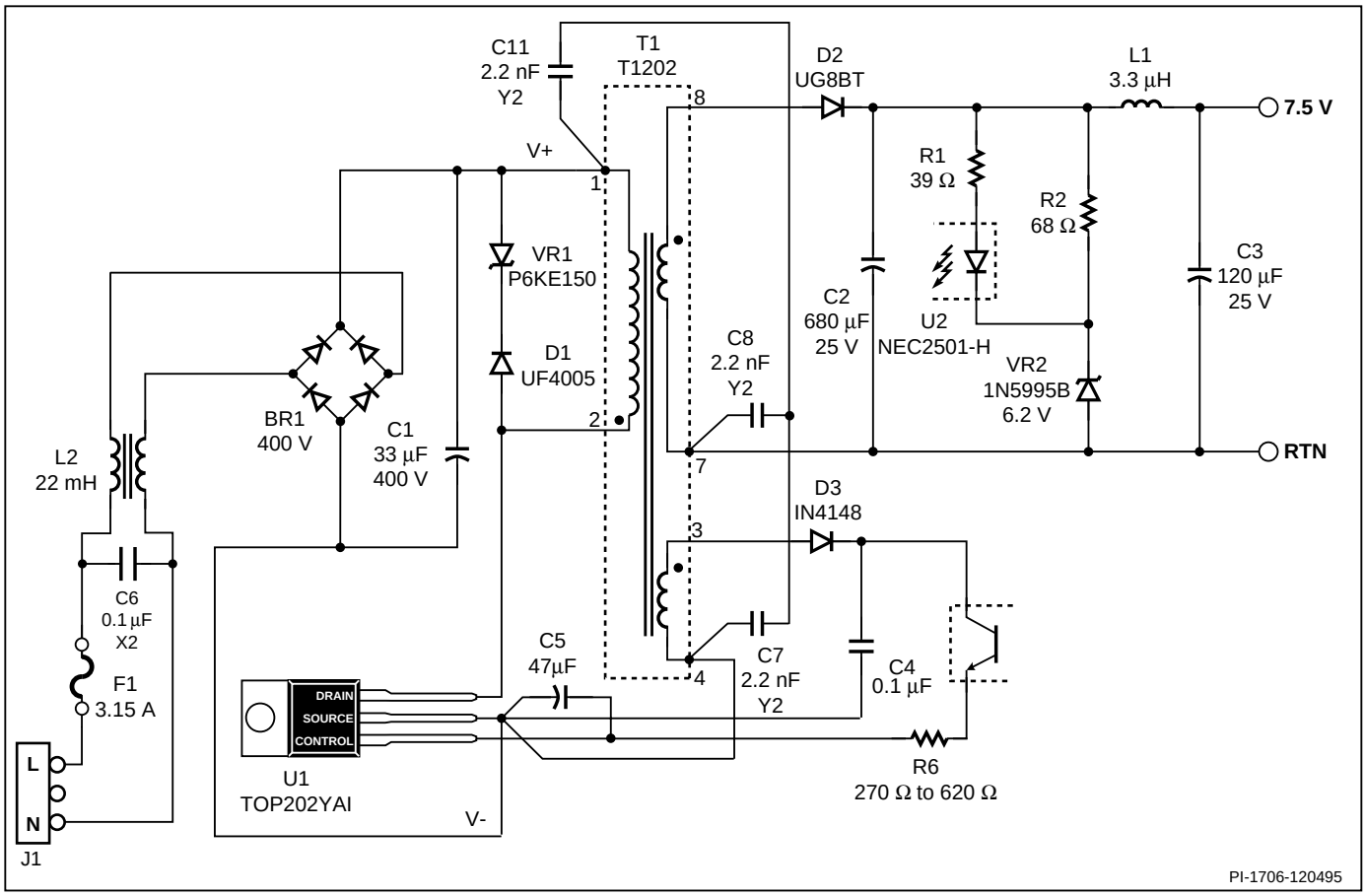

Figure 7. Modified ST202A Power Supply, 2-Wire Input.

Figure 8 shows a typical 3-wire modification to the ST202A *TOPSwitch* power supply. The earth ground wire is threaded through a ferrite bead or toroid to damp power cord resonances (see AN-15). Because of the connection to earth ground, C8 no longer needs to be a Y-capacitor but can be replaced with a simple, general purpose and low cost ceramic 0.1 uF capacitor. C7, C8, and C11 must have very short leads and be connected with short, wide traces.

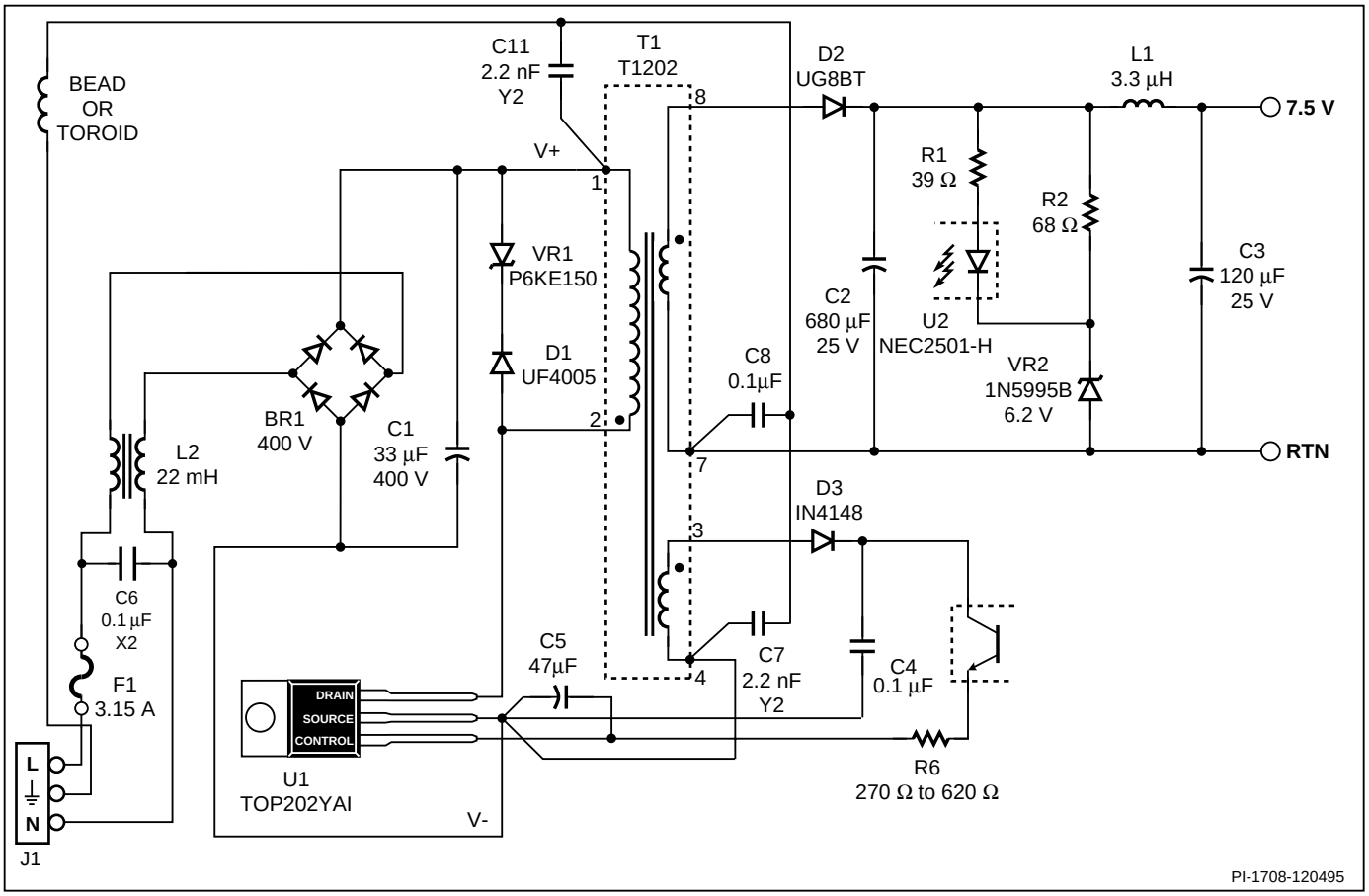

Figure 8. Modified ST202A Power Supply, 3-Wire Input.

Figure 9 shows a typical 3-wire input power supply with cascaded LC EMI filters. The sum of common mode inductance L2 and L3 should be 10 mH or less and L3 should be at least twice the value of L2 to prevent superposition of filter resonant frequencies. L2 will tend to have higher bandwidth and effectively filters higher frequency common mode currents close to the input power connection.

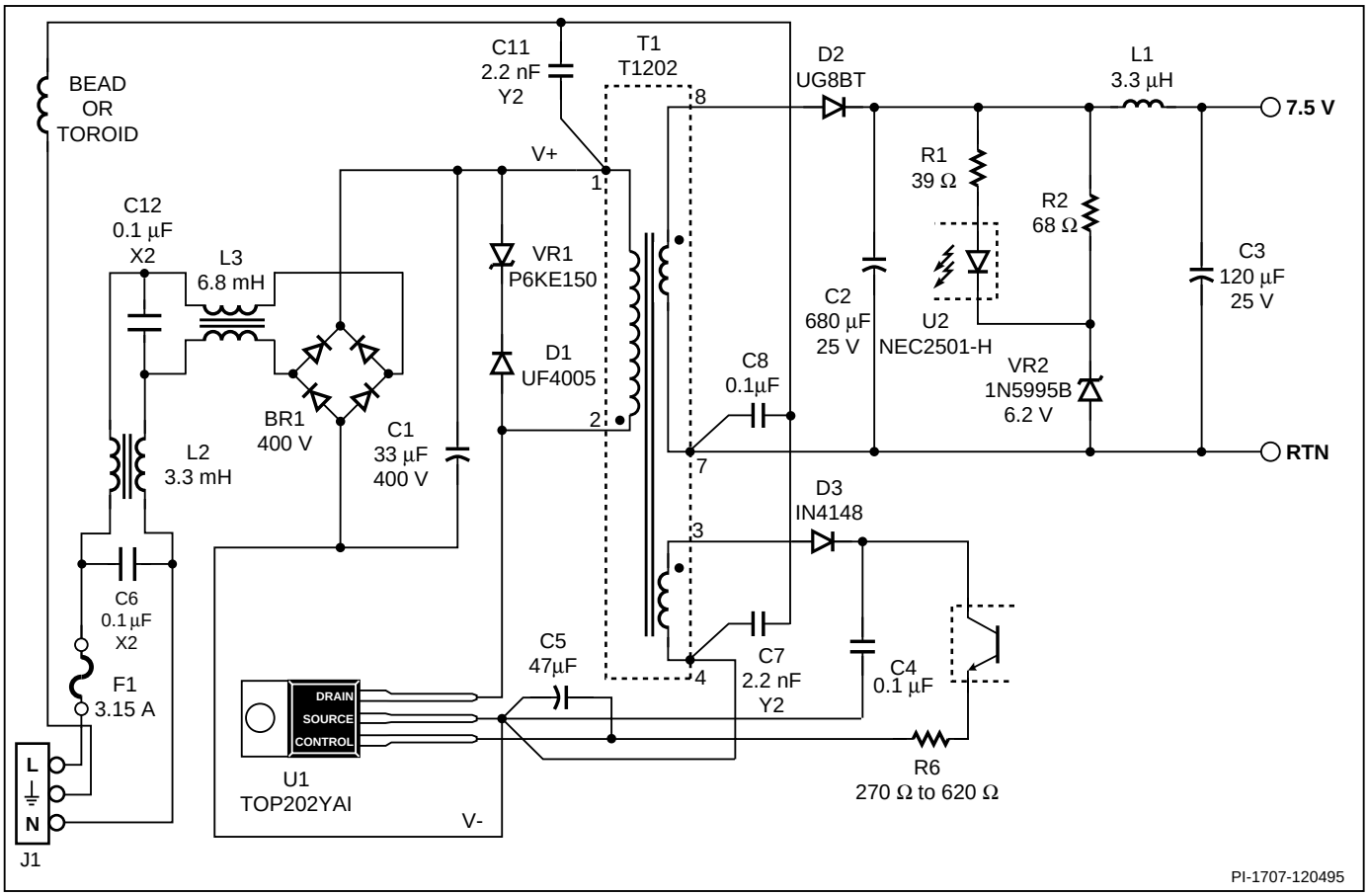

Figure 9. Modified ST202A Power Supply, 3-Wire Input with Two Cascaded LC EMI Filters.

The primary bias winding should be connected directly with a single trace to the *TOPSwitch* Source pin as shown in Figures 7, 8, and 9. Bias filter capacitor C4 should also connect directly to the *TOPSwitch* Source pin with a single trace.

Auto-restart capacitor C5 should be connected directly across *TOPSwitch* Control and Source pins to reduce noise voltages on the Control pin.

Reducing transformer capacitance reduces the peak transient currents. To reduce transformer capacitance, the primary must be properly located relative to the other windings. 3 to 5 layers of 2 mil thick polyester film tape should also be used between the secondary and all primary referenced windings. Three typical transformer design examples are given below:

Figure 10 shows a transformer with single primary layer, single tape layer and bias winding layer. To reduce capacitance, 3 to 5 tape layers are added before the secondary is wound.

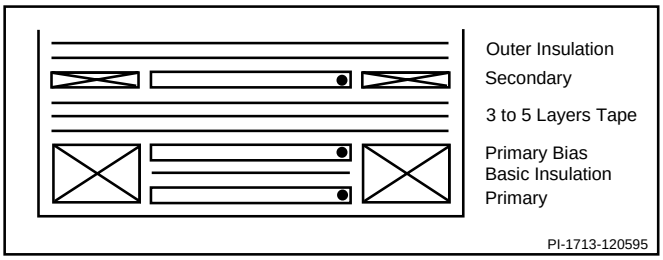

Figure 10. Single Layer Primary Transformer Cross Section.

Figure 11 shows a two layer primary transformer with the "noisy" or *TOPSwitch* connected half of the primary buried or shielded beneath the "quiet" or V+ connected half of the primary. To reduce transformer capacitance, 3 to 5 tape layers are placed before the secondary is wound. 3 to 5 more tape layers are placed over the secondary before the primary bias winding is wound.

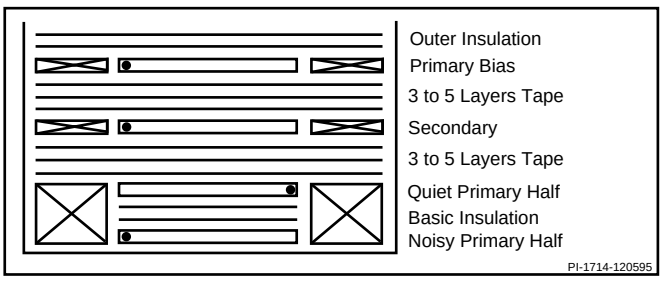

Figure 11. Two-Layer Primary Transformer Cross Section.

Figure 12 shows a split sandwich primary transformer. The "noisy" or *TOPSwitch* connected half of the primary is wound followed by 1 or 2 tape layers and the bias winding. To reduce transformer capacitance, 3 to 5 tape layers are placed followed by the secondary. 3 to 5 more tape layers are placed before winding the "quiet" or V+ connected half of the primary.

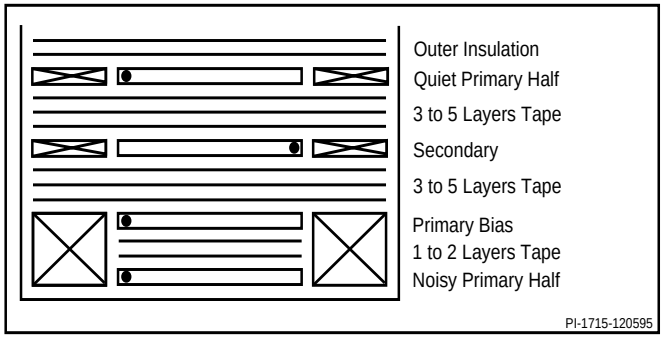

Figure 12. Split Sandwich Primary Transformer Cross Section.

When using triple insulated wire secondaries, the number of tape layers can be reduced to 1 or 2 layers due to the inherent spacing and reduced capacitance provided by the insulated wire.

The highest transformer secondary resistance (smallest wire diameter) should be used which is still consistent with power supply efficiency requirements. Slightly higher secondary resistance helps limit peak transient currents.

Heat sinks should be either connected only to *TOPSwitch* tab or completely isolated from both *TOPSwitch* tab and circuit. If the heat sink is connected elsewhere in circuit but isolated from *TOPSwitch* tab, capacitance between *TOPSwitch* tab and heat sink can resonate with circuit inductance causing high frequency ringing currents which may trigger *TOPSwitch* shutdown latch.

Additional Countermeasures for Differential Mode

Add resistor R6 (approximately 270 to 620 Ohms) in series with the optocoupler (U2) phototransistor emitter as shown in Figures 7, 8, and 9. R6 limits peak current flow below the latched shutdown trigger current threshold during output voltage and control loop overshoot.

Select larger input capacitor C1 to control the final DC bus voltage.

Carefully select bridge rectifier BR1 (or discrete diodes) for avalanche and voltage clamping capability.

Select a common mode choke to withstand some excessive normal mode current levels (occurring when bridge diodes

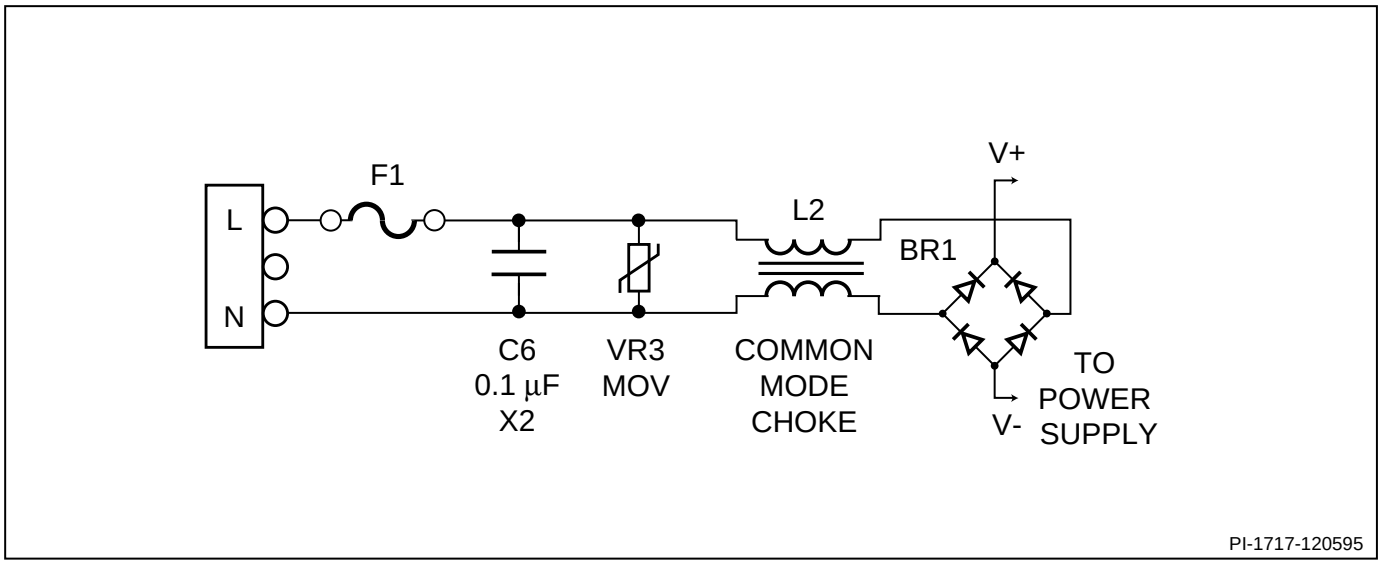

Figure 13. MOV VR3 Position Relative to X-Capacitor C6, Common Mode Choke L2 and Bridge Rectifier BR1.

avalanche and clamp the V+ high voltage DC bus) without causing sufficient coil magnetostriction to stress and crack the ferrite core.

For lower power 100 to 115 VAC applications, use higher voltage TOP2XX *TOPSwitch* for improved voltage breakdown margin relative to peak DC bus voltage V+ (across C1) which occurs following application of the transient test voltage.

Select MOV or metal-oxide-varistor transient suppressor to "clip" the peak off the higher transient test voltages. Connect varistor VR3 between fuse F1 and common mode choke L2 as shown in Figure 13. Long term reliability of VR3 should be high because VR3 absorbs only a portion of the energy associated with the highest peak transient test voltages. Lower peak transient test voltages can be safely tolerated without VR3 absorbing significant energy.

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