Clock Generation and Distribution for High-Performance Processors

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Outline

• Clock Distribution Trends
• Distribution Networks
• De-skew Circuits
• Jitter Reduction Techniques
• Clock Power Dissipation
• Future Directions
• Summary
Clock Definition and Parameters

- The **clock** is a periodic synchronization signal used as a time reference for data transfers in synchronous digital systems.

- **Skew**
  - Spatial variation of the clock signal as distributed through the chip
  - Global vs. local skew

- **Clock jitter**
  - Temporal variation of the clock with respect to a reference edge
  - Long-term vs. cycle-to-cycle jitter

- **Duty cycle variation**
  - 50/50 design target
Processor Frequency Trend

- 386
- 486
- Pentium®
- Pentium Pro®
- Pentium® II
- Pentium® III
- Pentium® IV

Frequency [MHz]

Clock Skew Trend

Source: ISSCC and JSSC papers
• Clock skew accounts in average for ~5% of the cycle time

Source: ISSCC and JSSC papers
Sources of Clock Skew

- With a perfectly balanced distribution, device mismatch is the largest contributor to the clock skew

![Bar chart showing sources of clock skew: Temperature Mismatch, Load Mismatch, Supply Mismatch, Device Mismatch (Le).]

Geannopoulos, ISSCC-1998
Clock Jitter Trend

Source: ISSCC and JSSC papers
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Clock Distribution Networks

- Tree
- Mesh
- Grid
- H-Tree
- X-Tree
- Tapered H-Tree
Inductance Effect

Xanthopoulos, ISSCC-2001
Itanium® Processor Clock Hierarchy

Reference Clock

Main Clock

Global Distribution

Regional Distribution

Local Distribution

Rusu, ISSCC-2000
Local Clock Distribution

- Local clock distribution enables flexible skew management to support:
  - Intentional clock skew insertion for timing optimization
  - Clock gating for power reduction
Itanium® 2 Processor Clock Distribution

- **First level**: Pseudo-differential, impedance matched branching, balanced h-tree
- **Second level**: balanced, width and length tuned binary h-tree
- **Second Level Clock Buffers**: adjustable delay buffer
- **Gaters**: all constant input loading with load-tuned drive strength

Anderson, ISSCC-2002
Optical Skew Probing

- Clock edge generates infrared photon emission
- Emission peak indicates clock transition edge

Tam, VLSI Symposium, 2003
Optical Probing Results

Tam, VLSI Symposium, 2003

20ps per division

24ps
130nm Itanium® 2 Skew Profile

Tam, VLSI Symposium, 2003
Pentium® 4 Processor Clock Network

- 2GHz triple-spine clock distribution (180nm)

Kurd, JSSC-2001
90nm Clock Distribution

- Sub-10ps clock skew demonstrated in a 90nm processor using clock tree averaging

Bindal, ISSCC 2003
Pentium® 4 Processor Clock Skew

- 90nm design has 3x lower clock skew than the 130nm

Schutz, ISSCC 2004
## Alpha* Processors Clocking

<table>
<thead>
<tr>
<th>Product</th>
<th>21064</th>
<th>21164</th>
<th>21264</th>
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<tbody>
<tr>
<td>Frequency</td>
<td>166MHz</td>
<td>300MHz</td>
<td>600MHz</td>
</tr>
<tr>
<td>Transistors</td>
<td>1.7M</td>
<td>9.3M</td>
<td>9.3M</td>
</tr>
<tr>
<td>Process</td>
<td>0.75um 4ML</td>
<td>0.5um, 4ML</td>
<td>0.35um, 6ML</td>
</tr>
<tr>
<td>Power</td>
<td>25W</td>
<td>50W</td>
<td>72W</td>
</tr>
<tr>
<td>Clock load</td>
<td>2.75nF</td>
<td>3.75nF</td>
<td>2.8nF</td>
</tr>
</tbody>
</table>

* Other names and brands may be claimed as the property of others

Gronowski, JSSC 1998
Power4* Clock Distribution

- Dual core, SOI process, 174M transistors
- Measured clock skew below 25ps

* Other names and brands may be claimed as the property of others

Restle, ISSCC-2002
Power4* - 3D Skew Visualization

- grid
- Tuned sector trees
- Sector buffers level 4
- buffer level 3
- buffer level 2
- buffer level 1

Delay (ps)

800
700
600
500
400
300
200
100

Restle, ISSCC-2002

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Dual-Zone Clock Deskew

Geannopoulos, ISSCC-1998
Itanium® Processor Clock Deskew

- Distributed array of deskew buffers to reduce process related skew
- 8 deskew clusters each holding up to 4 buffers
- 30 deskew zones

DSK = Cluster of 4 deskew buffers
CDC = Central Deskew Controller

Rusu, ISSCC-2000
Itanium® Processor Deskew Buffer

- Small step size enables fine skew control over a wide range
- TAP read / write access to Control Register enables faster timing debug and performance tuning

Rusu, ISSCC-2000
Pentium® 4 Processor Deskew

Logical diagram of the skew optimization circuit

Phase detector network

Kurd, JSSC-2001
Deskew Techniques Summary

<table>
<thead>
<tr>
<th>Author</th>
<th>Source</th>
<th>Clock Zones</th>
<th>Skew Before</th>
<th>Skew After</th>
<th>Step Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Geannopoulous</td>
<td>ISSCC-98</td>
<td>2</td>
<td>60ps</td>
<td>15ps</td>
<td>12ps</td>
</tr>
<tr>
<td>Rusu</td>
<td>ISSCC-00</td>
<td>30</td>
<td>110ps</td>
<td>28ps</td>
<td>8ps</td>
</tr>
<tr>
<td>Kurd</td>
<td>ISSCC-01</td>
<td>47</td>
<td>64ps</td>
<td>16ps</td>
<td>8ps</td>
</tr>
<tr>
<td>Stinson</td>
<td>ISSCC-03</td>
<td>23</td>
<td>60ps</td>
<td>7ps</td>
<td>7ps</td>
</tr>
</tbody>
</table>

- Clock deskew techniques compensate for device and interconnect within-die variations
- Deskew circuits cut clock skew to less than a quarter of the original value
Useful Clock Skew

- Use de-skew buffers to insert intentional skew to maximize the processor operating frequency
- Larger benefit achieved in early steppings

Tam, VLSI Symposium, 2003
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Pentium® 4 Processor Jitter Reduction

- RC-filtered power supply for clock drivers reduces clock distribution jitter

Kurd, JSSC-2001
Alpha* Processor Voltage Regulator

- Voltage regulator ensures optimum DLL tracking
- Supply noise frequencies over 1MHz are attenuated by more than 15dB

Xanthopoulos, ISSCC-2001

* Other names and brands may be claimed as the property of others
On-Die Clock Jitter Detector

Kuppuswamy, VLSI Symposium 2001
Array Phase Detector

- 7 elements above and below center, with increasing positive and negative built-in offset away from center
- Phase offset created by progressively delaying data wrt clock
Histogram Mode Operation

- Array Phase Detector
- XOR Logic
- Error Detection Logic

jitter error

count

bins

SoC 2004 – Stefan Rusu
Graph Mode Operation

- Array Phase Detector
- XOR Logic
- Error Detection Logic

- jitter error
- encoded bins

- time
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Clock Power Breakdown Example

- 30% of the total power is attributed to clock
- Most of the clock power is used in the final clock buffers and flip-flops

Anderson, ISSCC-2002
Clock Power Reduction

- Reduce clock frequency
  - Multiple frequency domains
  - Dual edge triggered flip-flops

- Reduce voltage swing
  - Low swing clocks

Clock Power = f * C * V^2

- Reduce clock loading
  - Clock gating
  - Clock-on-demand flip-flop
  - Optimized routing
Half Swing Clocking

• Requires four clock signals
  - Two clock phases with a swing between Vdd and Vdd/2 drive the PMOS devices
  - The other two phases with a swing between Gnd and Vdd/2 drive the NMOS transistors

• Experimental savings of 67% were demonstrated on a 0.5µm CMOS test chip with only 0.5ns speed degradation

• Requires additional area for the special clock drivers and suffers from skew problems between the four phases

Kojima, JSSC 1995
Clock-on-demand Flip-Flop

- Activates internal clock only when the input data will change the output - equivalent to single bit clock gating
- Longer setup time and sensitive to hold time violations

Hamada, ISSCC 1999
XScale Processor Clock Gating

- Three hierarchical clock gating levels
  - Top level – stop clock
  - Unit level – 83 enables
  - Local clock buffers – 400 unique enables

Clark, JSSC 11/2001
Dual Edge Triggered Flip-Flop

- Operates at half the clock frequency
- Requires tight control of the clock duty cycle

Nedovic, ESSCIRC 2002
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Rotary Clock Distribution

• Transmission line based, self-regenerating rotary clock generator

Wood, ISSCC-2001
Standing Wave Oscillator

O’Mahony, ISSCC-2003
10GHz Clock Grid Test Chip

- Fabricated in a 0.18µm 1.8V 6M CMOS process

- Very low clock skew and power consumption
- Attractive alternative for 10GHz clocking and beyond

<table>
<thead>
<tr>
<th></th>
<th>9.8 GHz – 10.5 GHz (6.4% range)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Locking range</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Skew</strong></td>
<td>0.6ps</td>
</tr>
<tr>
<td><strong>Jitter (added to external source)</strong></td>
<td>0.5ps rms</td>
</tr>
<tr>
<td></td>
<td>(1.4ps rms external source)</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>430mW</td>
</tr>
</tbody>
</table>
Optical Clock Distribution

• Board-level guided-wave H-tree distribution
• Monolithic silicon-based detection
• Couplers provide tolerance for horizontal and vertical misalignment of the flip-chip assembly
• Optical transmission is immune to process variations, power-grid noise and temperature

J.D. Meindl, Georgia Institute of Technology, 2000
Summary

• High performance processors require a low skew and jitter clock distribution network
• Clock distribution techniques are optimized to achieve the best skew and jitter with reduced area and power consumption
• Deskew techniques are demonstrated to cut the skew to $\frac{1}{4}$ of its original value
• On-die supply filters are used to reduce jitter
• Intensive research focuses on novel clock distribution techniques