Capacitive Position Sense Circuits

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Gyroscope Example

\[ x(t) = X_0 \sin \omega_x t \]

\[ \ddot{y}_{coriolis} = 2\Omega_z \times \dot{x}(t) \]

\[ = 2\Omega_z X_0 \omega_x \cos \omega_x t \]

\[ = 4.4 \times 10^{-3} \begin{bmatrix} m \\ s^2 \end{bmatrix} \times \cos \omega_x t \]

\[ m\ddot{y} = k_y y \]

\[ y = \frac{\ddot{y}}{\omega_y^2} \]

\[ = 0.003 \AA \times \cos \omega_x t \]

with \( \Omega_z = 1 \text{deg/s}, X_0 = 1 \mu\text{m}, \omega_x = \omega_y = 2\pi \times 20\text{krad/s}, Q = 1 \)

Outline

- Capacitive Sensor Interface
  - Bootstrapping
  - Offset & Drift Reduction
  - Charge Sensing
  - Correlated Double Sampling
  - Noise
Capacitive Interface

\[ C_{s1} = C_0 + \Delta C \]
\[ C_{s2} = C_0 - \Delta C \]
\[ V_x = V_0 \frac{\Delta C}{C} \]
Output Signal

\[ C_{s1} = C_0 + \Delta C \]
\[ C_{s2} = C_0 - \Delta C \]
\[ V_x = V_0 \frac{\Delta C}{C_0} \]

for \( C_0 = 100 \text{ fF} \)
\( \frac{dC}{dy} = 10 \text{ aF/Å} \)
\( y = 0.003 \text{ Å} \)
\( V_0 = 5 \text{ V} \)

\[ \Delta C = 10 \text{ aF/Å} \times 0.003 \text{ Å} = 0.03 \text{ aF} \]
\[ V_x = 5 \text{ V} \times 0.03 \text{ aF} / 100 \text{ fF} = 0.3 \mu\text{V} \]
Electrical Interface

Parasitic Capacitors

substrate

shield
Electrical Interface Model
Impact of Parasitics

\[ V_x = \frac{\text{signal}}{2\Delta CV_0 + C_{p1} V_{\text{sub}} + C_{p2} V_{\text{shield}}} \]

\[ C_T = 2C_0 + C_{p1} + C_{p2} \]
Impact of Parasitics (cont.)

1) signal attenuation by

$$\frac{1}{1 + \frac{C_{p1} + C_{p2}}{2C_0}} = \frac{1}{3}$$

2) couple $V_{\text{shield}}$ & $V_{\text{sub}}$ to $V_x$

   e.g. $V_{\text{sub}} = 1\text{mV}$
   
   $V_x = 250\mu\text{V} >> 0.3\mu\text{V}$

   keep substrate quiet!

3) parasitic electrostatic forces
   
   check voltage across all capacitors!
Parasitic Electrostatic Force

Example:

\[ F = \frac{CV_x^2}{2d} \]
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Bootstrapping

![Diagram showing bootstrapping circuit]

- $V_{\text{shield}} = V_{\text{out}} = V_x$  --->  voltage across $C_{p2}$ is always zero

$$V_x = \frac{2\Delta C V_0 + C_{p1} V_{\text{sub}}}{2C_0 + C_{p1}}$$

$C_{p2}$ effectively removed

- **Caveats**: instability if buffer gain $> 1$, increased noise
Unity Gain Buffer Circuits

Breadboard Setup:

\[ V_{in} \rightarrow \text{OpAmp} \rightarrow V_{out} = V_{in} \]

JFET inputs (negligible input current)
e.g. LF356 or LH0022

Integrated Circuit:

\[ V_{DD} = +2.5V \]

\[ V_{in} \rightarrow M3 \rightarrow M4 \rightarrow V_{out} \]

\[ M1 \rightarrow M2 \rightarrow 50\mu A \]

\[ M5 \rightarrow M6 \rightarrow 50\mu A \]

\[ V_{SS} = -2.5V \]

\[ V_{out} \approx 0.98 \cdot V_{in} \]
Improved Buffer

\[ V_{in} \rightarrow \text{Buffer} \rightarrow V_{out} \approx 0.999 \, V_{in} \]

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Offset & Drift Reduction

EMI (Electromagnetic Interference)
substrate coupling
carrier generation
amplifier offset & drift
flicker noise (1/f noise)

\[ +V_0 \]
\[ C_{s1} 100fF \]
\[ C_{s2} 100fF \]
\[ -V_0 \]
\[ C_{p1} 100fF \]
\[ C_{p2} 300fF \]
\[ V_{x} \]
\[ V_{out} \]
\[ V_{shield} \]

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Modulation & Demodulation

\[ \Delta C \]

\[ +V_0 \quad -V_0 \]

\[ C_{s1} \]

\[ V_x \]

\[ C_{s2} \]

\[ +1 \quad -1 \]

\[ f_{clk} \]

\[ V_y \]

\[ f_{clk} \]

\[ V_z \]

\[ \text{Demodulator (multiplier)} \]

\[ \text{lowpass filter} \]

\[ V_{out} \sim \Delta C \]
Frequency Domain Interpretation

\[ \Delta C \sim \Delta x \sim \text{input} \]

\[ V_x \quad V_y \quad V_z \quad V_{out} \]
Modulation (cont.)

• like AM radio
  different name: “chopper stabilization”

• modulation frequency
  \( f_{\text{clk}} = 100\text{kHz} \ldots 10\text{MHz} \) (typical)

• wave-form:
  sinusoidal or
  square-wave (avoid distortion!)
Demodulator Circuit

Gilbert Multiplier:

\[ V_{\text{out}} \sim V_1 \times V_2 \]

![Gilbert Multiplier Diagram](image)

(MOS circuit identical)
DC Potential

Dimensioning $R_{dc}$:

$$|i_{signal}| >> |i_{dc}| \quad \rightarrow \quad 2\pi f_{clk} C_{s1} V_x >> \frac{V_x}{R_{dc}} \quad \rightarrow \quad R_{dc} >> \frac{1}{2\pi f_{clk} C_{s1}} = 1.6M\Omega$$

for $f_{clk} = 1\text{MHz}$ and $C_{s1} = 100\text{fF}$
Realizing $R_{dc}$

- physical resistor
  - low-doped polysilicon
  - thin-film resistor
  - avoid large parasitic capacitance (e.g. diffusion)
- back-to-back diodes
  - nonlinear distortion
- MOSFET in weak inversion
  - poor control
- Switched Capacitors
Example: ADXL-50

- full-scale input: 50 g
- noise floor: 6.6 mG/rt-Hz
- linearity: 0.2 % of F.S.
- bandwidth: 1 kHz
- power dissipation: 50 mW

Ref.: Analog Devices ADXL-50
ADXL 50 Layout
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Charge Sensing Concept

\[ V_x = 0 \]

\[ q = \Delta C \frac{V_0}{2} \]

\[ V_{\text{out}} = -V_0 \frac{\Delta C}{C_{\text{int}}} \]

\[ C_{s1} = C_0 + \Delta C \]

\[ C_{s2} = C_0 - \Delta C \]

\[ V_x \text{ is virtual ground} \]
Charge Sensing: Parasitics

\[ V_{out} = -V_0 \frac{\Delta C}{C_{int}} \]
Charge Sensing: Parasitics

- virtual ground shorts $C_p$
- no need to drive shield

CAVEATS:

- $V_{\text{sub}}$ still couples to $V_{\text{out}}$
- avoid undesired electrostatic forces
- $C_p$ increases electronic noise
Choosing $C_{\text{int}}$

$$V_{x} = 0$$

$$V_{\text{out}} = -V_{0} \frac{\Delta C}{C_{\text{int}}}$$

Time constant $\tau$
Choosing $C_{\text{int}}$ (cont.)

- **Gain:**
  \[ V_{\text{out}} \propto \frac{1}{C_{\text{int}}} \quad \rightarrow \]
  \[ C_{\text{int}} \rightarrow 0 \iff V_{\text{out}} \rightarrow \infty \]

- **Time-constant (settling time):**
  \[ \tau \propto \frac{1}{C_{\text{int}}} \quad \rightarrow \]
  \[ C_{\text{int}} \rightarrow 0 \iff \tau \rightarrow \infty \]

- **Gain-Speed Tradeoff:**
  \textit{typical:} $C_{\text{int}} \approx 2C_0$
Offset & Drift Reduction

• Chopper Stabilization

• Correlated Double Sampling (CDS)
  – no low-pass filter (increased bandwidth)
  – no need for leak resistor ($R_{dc}$)
  – disadvantage: needs clocks
Chopper Stabilization
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CDS Problem

\[ V_{x} = V_{\text{offset}} \]

\[ V_{out} = V_{0} \frac{\Delta C}{C_{\text{int}}} + V_{os} \left( 1 + \frac{C_{s1} + C_{s2}}{C_{\text{int}}} \right) \]
CDS Concept

Two Phase Operation:

1) measure and cancel offset
2) measure signal
CDS Phase 1a: Measure Offset

\[ V_{out} = A_v V_{os} \]

should be zero
CDS Phase 1b: Cancel Offset

\[ V_{out,off} = V_{os1} \frac{A_{v1}}{A_{v2} + 1} + V_{os2} \frac{A_{v2}}{A_{v2} + 1} \ll 1 \]

input referred amplifier offset:

\[ V_{in,off} = \frac{V_{out,off}}{A_{v1}} \approx \frac{V_{os1}}{A_{v2}} + \frac{V_{os2}}{A_{v1}} \ll V_{os1} \]
CDS Phase 2: Measure Signal

\[ V_{out} = V_0 \frac{\Delta C}{C_{int}} \]

\[ + \left( 1 + \frac{C_{s1} + C_{s2}}{C_{int}} \right) \frac{V_{in,off}}{A_{v1}} \]

\[ \approx V_0 \frac{\Delta C}{C_{int}} \text{signal} \]

\[ + \left( 1 + \frac{C_{s1} + C_{s2}}{C_{int}} \right) \frac{V_{os1}}{A_{v2}} + \frac{V_{os2}}{A_{v1}} \]
Complete CDS Circuit
CDS References

• General Principle
  M. Degrauwe et al, “A Micropower CMOS-Instrumentation Amplifier”,

• Capacitive Sensor Interfaces with CDS
  T. Smith et al, “A 15b Electromechanical Sigma-Delta Converter for
  Acceleration Measurements”, in Digest ISSCC 94, pp. 160-161,
  February 1994.
  C. Lu et al, “A Monolithic Surface Micromachined Accelerometer with
  Digital Output”, IEEE J. Solid-State Circuits, pp. 1367-1373,
  December 1995.
  M. Lemkin et al, “A Micromachined Fully Differential Lateral
  Accelerometer”, in Digest CICC 96, pp. 315-318, May 1996.
Example 1: CDS Z-Axis Accelerometer

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size</td>
<td>3 x 3 mm²</td>
</tr>
<tr>
<td>Mass</td>
<td>0.5 µgram</td>
</tr>
<tr>
<td>Resonant frequency</td>
<td>4.7 kHz</td>
</tr>
<tr>
<td>Air gap</td>
<td>1.6 µm</td>
</tr>
<tr>
<td>Sense capacitance</td>
<td>500 fF</td>
</tr>
<tr>
<td>Feedback capacitance</td>
<td>300 fF</td>
</tr>
<tr>
<td>Noise floor</td>
<td>1.6 mG/rt-Hz</td>
</tr>
</tbody>
</table>

Example 1: CDS Position Sensor
Example 1: CDS Amplifier
Example 2: Differential CDS Accelerometer

Process: 3 μm BiCMOS
Power: 3.7 mA @ 5V
Sampling rate: 500 kHz
Full scale: ±3.5 G
Noise floor: 500 μG/rt-Hz
Resonant freq.: 8.1 kHz
Proof mass: 0.2 μgram
Sense cap.: 84 fF per side
Sensitivity: 64 fF/μm

Example 2: Differential Position Sense Amp

Differential interface improves power supply and EMI rejection, and achieves first-order cancellation of switch charge injection errors.
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• Correlated Double Sampling

微量 Noise
Noise Sources

• “man-made”, e.g.
  – power supply coupling
  – clock feed-through
  – electromagnetic interference (EMI)
  → make arbitrarily small

• “correlated”, e.g.
  – offset
  – 1/f noise
  → low frequency: measure and cancel

• “thermal” (synonyms: Johnson, Brownian, …)
  – from thermodynamics
  – sets ultimate performance limit
Device Thermal Noise Models

Resistor

\[
\overline{v_n^2} = 4k_B TR \Delta f
\]

MOSFET

\[
\overline{v_n^2} = 4k_B T \frac{2}{3g_m} \Delta f
\]

\(k_B = 1.38 \times 10^{-23} \text{ J/K}\) (Boltzmann's constant)

\(k_B T = 4.1 \times 10^{-21} \text{ J}\) at room temperature \((T = 300^0 \text{ K})\)

\(e.g.\ R = 1M\Omega, \ \Delta f = 1\text{kHz} \quad \rightarrow \quad \sqrt{\overline{v_n^2}} = 2\mu\text{V}\)
Noise Bandwidth

Typical sensor application:

Noise power is proportional to sensor bandwidth (assuming flat spectrum).
MOS Amplifier Noise

input transistors
transconductance $g_m$
gate capacitance $C_{gs} = 2/3 WLC_{ox}$
MOS Amplifier Noise Model

\[
\bar{v}_n^2 \approx 4k_B T \frac{2}{3g_m} \Delta f (1 + F)
\]

with \( F > 0 \)

(typical: \( F = 2 \ldots 5 \))

\[
C_{in} = C_{gs1} = C_{gs2}
\]

(assumption: transconductance amplifier - high impedance output)
Noise Calculation

\[
\overline{v^2_{o,n}} = 2\overline{v^2_n}\left[1 + \frac{C_T + C_{in}}{C_{int}}\right]^2
\]

with \( C_T = C_{s1} + C_{s2} + C_p \)
Input Transistor Sizing

- increasing $g_m$ reduces amplifier noise
  \[ \overline{v_n^2} \approx \frac{1}{g_m} \]

- **CAVEAT:**
  \[ C_{in} \approx C_{gs} = \frac{g_m}{\omega_T} \quad \text{typical } \omega_T = 2\pi [1 \ldots 10 \text{ Grad/sec}] \]

  implies $C_{in}$ and hence noise increase with $g_m$

  \[ \textbf{OPTIMUM} \]
Noise Optimum

- shallow optimum for $C_{in} = C_T$
- $C_{in}$ (transistor size) also affects speed: in practice often choose $C_{in} > C_T$
Minimum Detectable Signal (MDS)

- Definition: signal power = noise power

\[
\sqrt{\left(\frac{\Delta C}{C_0}\right)^2} \approx \frac{8}{V_0} \sqrt{\frac{2k_B T}{3\omega_T C_0 \left(1+\frac{C_p}{C_0}\right)}}
\]

Assumption: \(C_m = C_T\) (optimal transistor sizing)

Example: Accelerometer

- proof-mass displacement
  \[ x = \frac{a_{in}}{\omega^2} \quad \omega_r = 2\pi f_r = \text{ resonant frequency} \]

- parallel plate capacitor
  \[ \frac{dC}{dx} = \frac{C_0}{x_0} \]

- acceleration noise floor
  \[ \sqrt{\frac{a_{in}^2}{\Delta f}} \approx \frac{32\pi f_r^2 x_0}{V_0} \sqrt{\frac{2k_BT}{3\omega_r C_0} \left(1 + \frac{C_p}{C_0}\right)} \]

E.g. \( C_0 = 500\text{fF}, \quad \omega_T = 2\pi \times 500\text{MHz}, \quad V_0 = 500\text{mV}, \quad f_r = 5\text{kHz}, \quad x_0 = 1\mu\text{m} \)

\[ \sqrt{\frac{a_{in}^2}{\Delta f}} \approx 1\mu\text{G} / \sqrt{\text{Hz}} \]
Summary

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